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LARGE-SCALE DIGITIZER SYSTEM, ANALOG CONVERTERS

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LARGE-SCALE DIGITIZER SYSTEM, ANALOG CONVERTERS*

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Abstract

Analog to digital converter circuits that are based on the sharing of common resources, including those which are critical to the linearity and stability of the individual channels, are described. Simplicity of circuit composition is valued over other more costly approaches. These are intended to be applied in a large-scale processing and digitizing system for use with high-energy physics detectors such as drift-chambers or phototube-scintillator arrays. Signal distribution techniques are of paramount importance in maintaining adequate signal-to-noise ratio. Noise in both amplitude and time-jitter senses is held sufficiently low so that conversions with 10-bit charge resolution and 12-bit time resolution are achieved.

Introduction

As high-energy physics experiments tend toward the need to digitize larger numbers of analog quantities, the need for an economical analog converter system has become increasingly evident. Such a system, called the LARGE-SCALE DIGITIZER SYSTEM,[1] has been developed. Much of the economy of this system is due to the sharing of system resources and controls by many channels of converter. This paper describes the unique character of the converter channels of the Large-Scale Digitizer (LSD). The particular design of these converters is instrumental in achieving the low overall system cost of the complete LSD system.

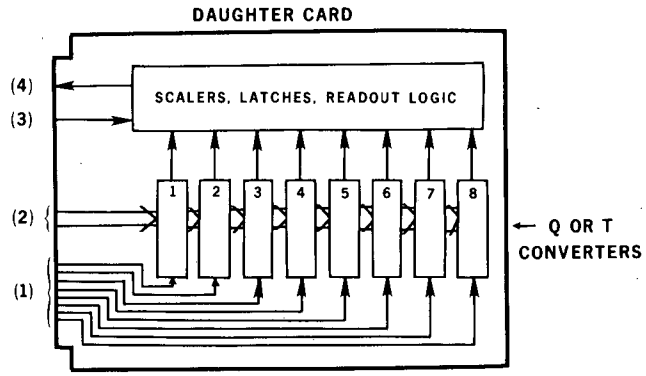
Analog Converter Card

Figure 1 shows diagrammatically the concept of an analog converter daughter card used in the LSD System. Signals (2), (3), and (4) are organized by a control card which is common to 16 such daughter cards in a full LSD bin. It is the sharing of these signals by up to 128 channels per bin that makes these converters practical, in that it results in reasonably low cost. Note particularly that the conversion time-base is one of the shared signals. The digitizing counter and readout circuits are shared by all eight converters on a daughter card.

Charge Converter

Block Diagram

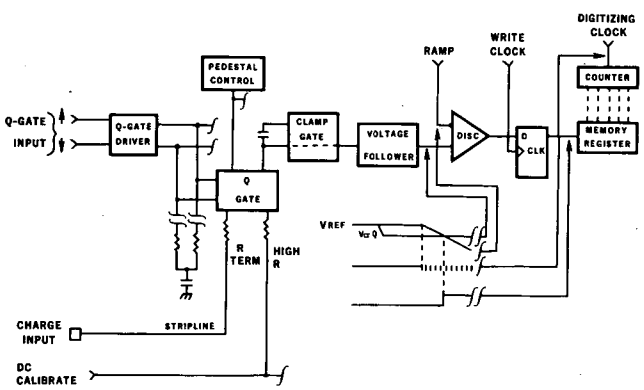
Figure 2 shows a block diagram of the charge converter. A brief overview shows the converter functions as follows: analog voltage at the CHARGE INPUT is converted to a proportional current which is stored on the output capacitor through Q-GATE. The capacitor voltage is reduced from Vref by an amount proportional to input charge; this voltage is buffered by a voltage-follower, and is established as a voltage, VαQ, at the non-inverting input of the comparator discriminator. At some time after completion of charge storage, DIGITIZING CLOCK and



(1) INDIVIDUAL INPUTS (1-8 CONVERTERS)
(2) COMMON SIGNALS: FAST GATES
CONVERSION TIME-BASE
PEDESTAL
CALIBRATION
RESET
(3) READOUT CONTROL
(4) BIT-SERIAL READOUT

ANALOG CONVERTER CARD
(CHARGE OR TIME)
LARGE SCALE DIGITIZER SYSTEM

FIG. 1



CHARGE CONVERTER
LARGE SCALE DIGITIZER
FIG. 2

RAMP are initiated as shown on the timing diagram. As the RAMP voltage transverse VαQ, the comparator output switches a high level to the D input of the latching flip-flop. The next WRITE CLOCK, providing proper phase relative to the DIGITIZING CLOCK, sets the flip-flop and thereby strobes the contents of the counter into the memory registers.

Peripheral circuits include buffer Q-GATE and

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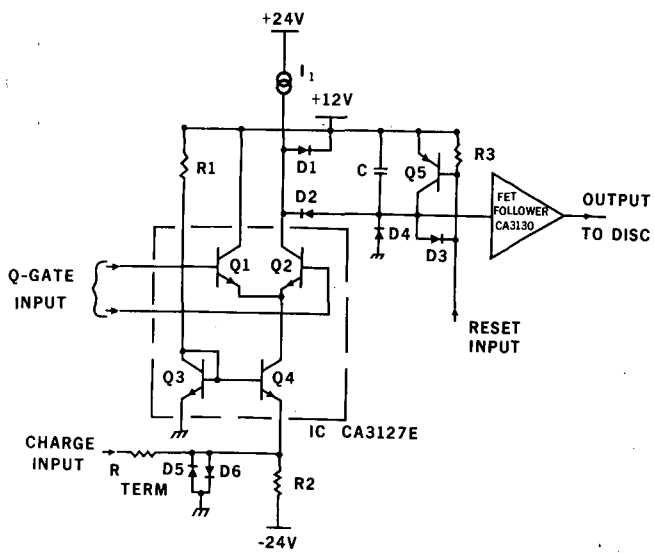
CLAMP-GATE drivers to minimize loading to the common input lines. PEDESTAL CONTROL is a variable current source which is adjusted to uniformly set each ADC channel. Accurate calibration current to each channel is developed through a precision high resistance driven by the common DC CALIBRATE line.

Analog Circuit of Charge Converter

The basic circuit which generates an output voltage proportional to input charge is shown in Figure 3. Circuit simplicity and low cost are largely attributable to the integrated circuits used. A brief description of parameters and operation is given below.



BASIC ANALOG CIRCUIT OF CHARGE-TO-TIME CONVERTER

FIG. 3

Integrate Circuit CA3127E is connected to form a gated voltage-to-current converter. Input R_{TERM} in series with Q4 emitter resistance provide the input terminating impedance. D5 and D6 are protection diodes and high resistance R2 provides the bias current-source. Off-set voltage at the CHARGE INPUT terminal is typically less than 2 mV and is temperature stable. Q4 base voltage is generated by the base-emitter voltage across diode-connected transistor Q3; integrated on the same substrate Q3 and Q4 are identical and self-compensating for temperature variation.

Q1 and Q2 form a fast current-switching pair. These devices have low noise, current gain typically 90, and bandwidth in excess of 1 GHz. Operationally, switching time is in the order of 1 nanosecond.

Prior to the arrival of the input charge, Q2 is switched off and sink-current from Q4 is diverted through Q1. Current I_1 is forced to flow through D1 thereby clamping the collector of Q2 to +12V. At the appropriate time, Q2 is switched on; current through Q4 forces the collector voltage at Q2 to fall below +12V thereby turning on D2, completing the current path from the CHARGE INPUT terminal to the charge-holding capacitor C.

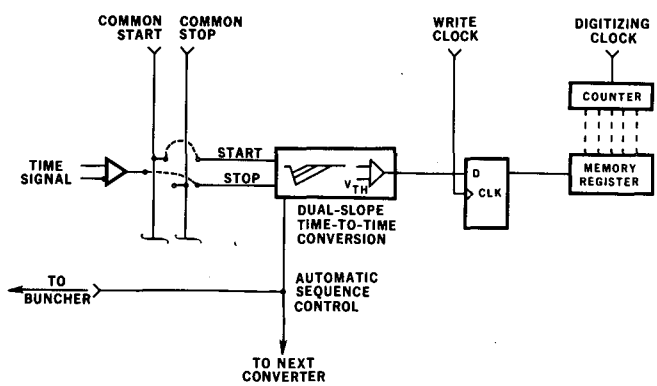
Current I_1 is adjusted during channel setup (PEDESTAL CONTROL) to be less than sink-current from Q4 assuring D2 turn-on and thereby setting a pedestal charge.

The clamp gate circuit (Q5, D3, R3) provides a fast reset and a firm voltage reference. During the inactive period, a constant RESET level is applied which drives transistor Q5 into near saturation. Saturation is avoided by diverting base current through D3 when collector-emitter voltage of Q5 is approximately 0.3V. Turn-off time of Q5 is typically 12 nanoseconds. Thus, resetting a full-scale charge of 256 pico-coulomb to less than one percent of full scale can be accomplished in less than 300 nanoseconds. D4 provides compensation current to null circuit leakage current, resulting in a typical net charge through leakage of 0.5 pC over a 50 μs ramp period.

Time Converter

Design Concept

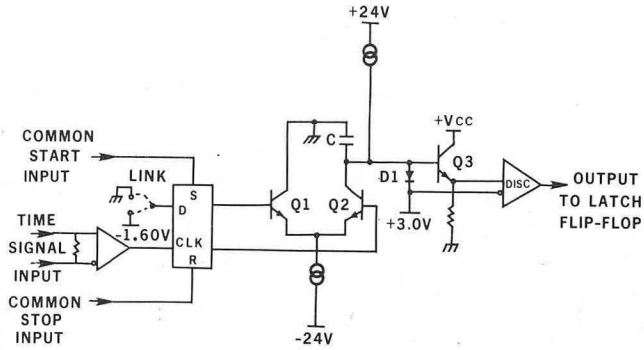
Time digitization is accomplished by means of the dual-slope technique followed by the same digitizer circuitry used in the charge digitizer. The time converters are flexible, allowing for common start or common stop (with self-abort) modes of operation. By means of wire links, four converts can be caused to self-advance for the purpose of accommodating sequential hits on a wire; or on a group of wires when used with the buncher (wire identification[1] register). Figure 4 is a simplified block diagram showing one of eight channels.



TIME CONVERTER
LARGE SCALE DIGITIZER
FIG. 4

Analog Circuit of Time Converter

The basic analog circuitry of the time converter is shown in Figure 5. A brief circuit description for a COMMON START mode is given as follows: in the quiescent state Q2 is switched off allowing storage capacitor C to charge to a reference voltage of approximately +3.6V clamped by D1. The comparator discriminator output is held at a high-voltage level with a small amount of hysteresis. The arrival of a COMMON START pulse sets the flip-flop to switch Q2 on, discharging storage capacitor C toward ground. Within a few millivolts below +3.6V reference the discriminator output switches to a low-voltage level.



BASIC ANALOG CIRCUIT OF TIME-TO-TIME CONVERTER:

FIG. 5

Arrival of a TIME SIGNAL pulse resets the flip-flop thus switching Q2 off. Down-ramping ceases and up-ramping immediately begins and ends when the voltage across C returns to the +3.6V reference level. At this point in time, the discriminator switches a high-voltage level to the D-input of the latching flip-flop. Operation of digital registration into the memory registers is the same as previously described. Time expansion is essentially governed by the ratio of the two current sources shown.

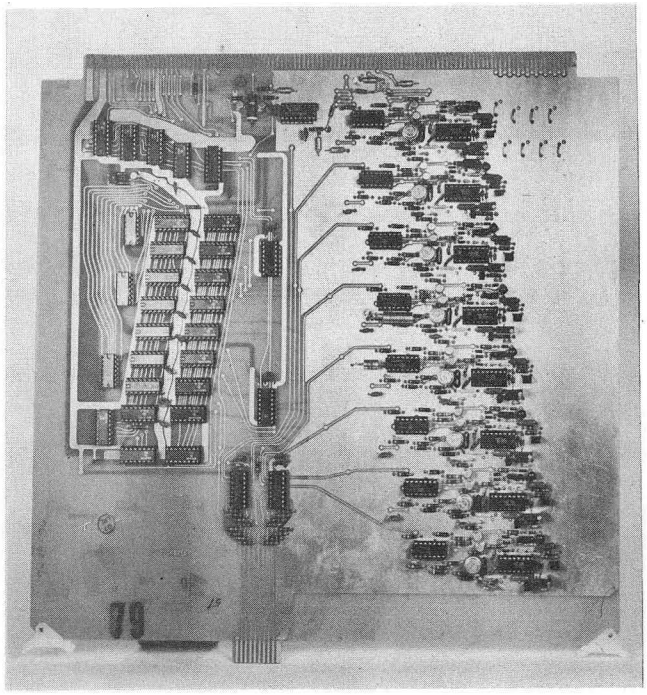
Summary

Figures 6 and 7 show eight-channel daughter cards for Charge and Time Converters, respectively. Identical digital circuitry for the two systems can be seen at the left portion of each board.

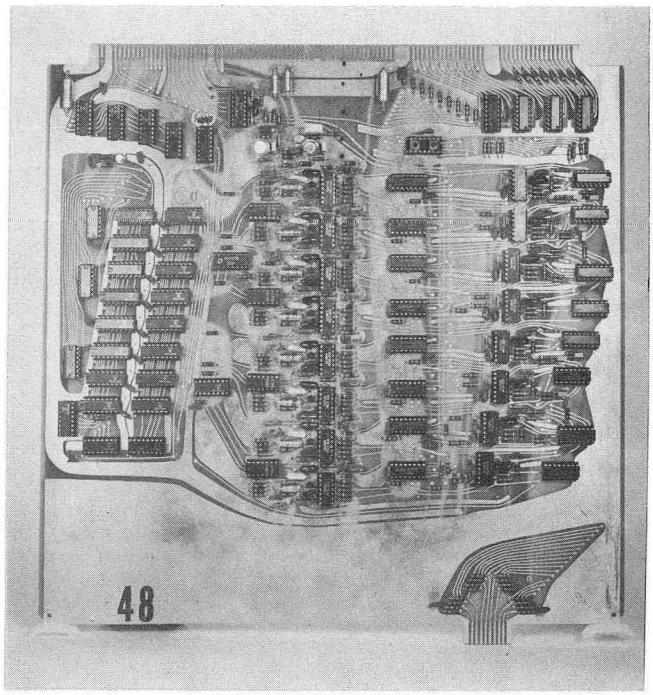
Analog circuits of the ADCs have been designed for high performance with emphasis on circuit simplicity and associated low cost. However, stability of the ADCs is critically dependent upon several of the signals that are bussed between the LSD bin controller and all ADC cards.

The charge ADCs system's sensitivity to Q-gate jitter is 50 ps per least count when calibrated to full scale with 50 ns Q-gate. The time-base ramp must be stable and repeatable within ±1 mV. Standard deviation of 0.7 least count is typically achieved for full-scale calibration signal with 50 ns Q-gate; deviation is proportionately lower for lower amplitudes. Pedestal count varies at the rate of one count per 1/4 μA of pedestial control current for 1 μs charge gates.

ADC calibration is accomplished by distributing ADC calibration voltage (from a computer-controlled DAC, for instance) to all inputs, and "strobing" with a stable Q-gate. For this purpose the Q-gate width is stabilized by the clipping-line technique. The distribution circuitry for the dc calibration voltage is designed to be insensitive to differences in ground potential between different parts of the system and is self-protected against possible short circuits on the converter cards.



CHARGE CONVERTER CARD
FIG. 6



TIME CONVERTER CARD
FIG. 7

Reference

1. R. F. Althaus, et al., "A Large-Scale Digitizer System (LSD) for Charge and Time Digitization in High-Energy Physics Experiments," published in these proceedings.

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