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FAST SUCCESSIVE APPROXIMATION ANALOGUE-TO-DIGITAL CONVERTER

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FAST SUCCESSIVE APPROXIMATION ANALOGUE-TO-DIGITAL CONVERTER*

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ABSTRACT

A new scheme has been developed for a 4096 Channel (12 Bit) Successive Approximation ADC which will allow more rapid coding than schemes commonly used at the present time. The allowable bit setting time for the major bits has been increased without adding to the total coding time. This is accomplished by permitting the initial accuracy of the setting of the major bits to be within eight channels. Towards the end of the coding time, when the major bits have settled, this error is corrected to an accuracy of a fraction of a channel.

Using this scheme a differential nonlinearity of better than 20% has been achieved in the basic encoder with a total coding time of 4 μs. Applying a 6-bit sliding register (the method of Gatti) to the ADC, a differential nonlinearity less than 0.5% results in the complete ADC.

INTRODUCTION

Pulse-height analyzers commonly use run-down ADCs (first proposed by Wilkinson[1]) which give excellent differential linearity, a very important parameter for pulse-height analyzers. Modern run-down ADCs use a 100 MHz clock, but even at this frequency the conversion time is 40 μs for a 12 bit ADC, which is long compared with the cycle time of modern memories.

With the availability of precision resistors and integrated circuits, successive approximation ADCs have become quite attractive for pulse-height analyzers. An early design of 12-bit ADC reported by Robinson, et al[2] achieved a 24 μs conversion time. The required differential linearity can

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be achieved using the Gatti[3] sliding-scale method which subtracts a random level ranging up to a few bits from the analogue signal while adding the equivalent digital code to the digital output. This causes the error in channel widths produced by variations in the components making the digital to analogue comparison to be distributed over several channels thereby improving the differential linearity.

Kandiah, et al[4] report another method (the cycling method) in which a smaller number of precision resistors is used than in the conventional successive approximation method. The stretcher input signal is held in the first sample-and-hold circuit and compared with a potential equivalent to the major bit. If the signal is more than the major bit a voltage equivalent to the bit is subtracted from it and the difference is precisely amplified by a factor of 2. The resulting signal is held in a second sample-and-hold circuit, and the first one is cleared. The signal from the second sample-and-hold circuit is then transferred to the input of the first sample-and-hold circuit and the next bit cycle is initiated. This process continues until all bits are processed. In this method not only the subtracting signal but the transients in the sample-and-hold circuit must settle before the next cycle can start. Time is also wasted during the transfer from one sample-and-hold circuit to the other. The reported conversion time for a 12 bit ADC using this method is 12 μs, and little room is left for reduction of this time.

The present paper describes a method of reducing the coding time while still giving the major bits enough time to settle within the desired accuracy. Figure 1 shows a simplified block diagram of an ADC using this method. The method is characterised by initially subtracting a level from the stretched signal equal to eight channels (bit #3) of current. Then the conversion starts by subtracting a current equal to the bit #11 from the stretched signal. If the current from the bit #11 is less than the current from the stretched signal then the bit #11 is set in a register. If the current is greater than the stretched signal then the bit is not set and the 11th bit current is removed. The accuracy of the comparison between the stretched signal and the current from the bit set need only be within eight channels (2^3) as the comparison will be corrected later to better accuracy. Successive lower bits are processed in a similar way until the bit #4 is compared. At this point the bit #3 pedestal is removed and the #4 bit comparison is repeated. The

setting of this bit and later ones require that the accuracy of comparison be much better than one channel. This is easily possible because minor bits require less time to settle than major bits, where large currents are switched. The scheme permits the most significant bit and other major bits to settle during the period of time until the pedestal is removed. A digital adder is used at the output to allow for the fact that the bit #4 setting is repeated.

The addition of the bit #3 pedestal speeds up the conversion substantially; allowing a bit setting period of 300 ns, the total conversion time is about 4 μs. This can be reduced to 2 μs by use of a scheme whereby two suitably timed pedestals are subtracted from the stretched current. For example, a bit #5 pedestal might be subtracted until the bit #6 is decoded. A bit #0 pedestal then replaces it until the bit #1 has been decoded. The bit #6 comparison and the bit #1 comparison must be repeated and a 12 bit adder is needed.

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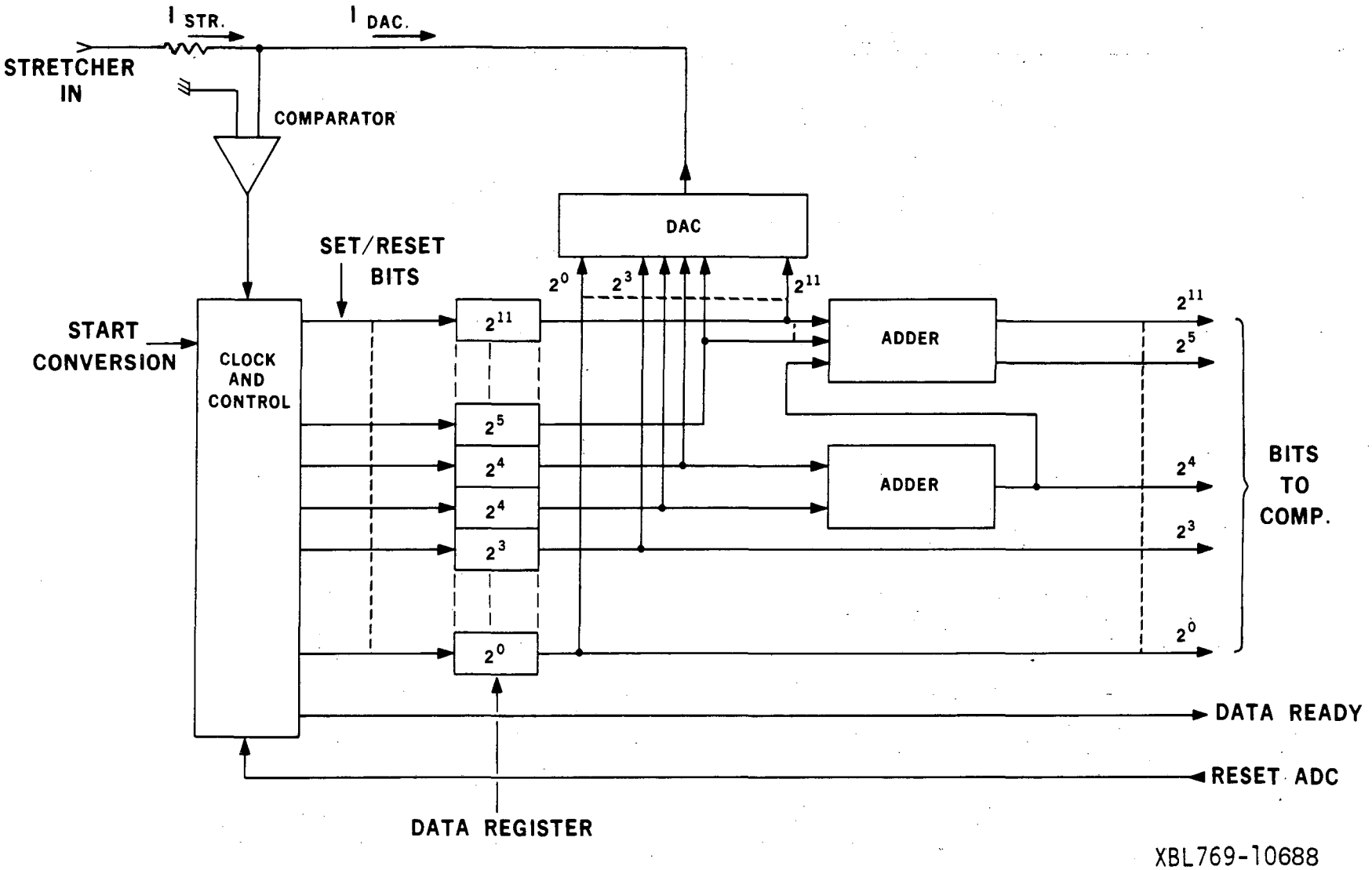

Fig. 1. A simplified block diagram of an ADC

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