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1K DELAY LINE DIGITIZER

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1K DELAY LINE DIGITIZER*

LBL-7215

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INTRODUCTION

The initial External Muon Identifier (EMI) experiment[1-6] at the Fermi National Accelerator Laboratory consisted of 30 Multiwire Proportional Chambers (MWPCs) with an equal number of discriminators and digitizers. Each chamber had seven outputs representing two signals per plane (X, Y and U) and a common signal called "prompt". These chambers were located around a 15-foot diameter bubble chamber that was placed along the neutrino beam line.

At the time an average of five events were expected per 60 μs beam spill. Therefore, the first digitizers had seven independent channels[7] with a maximum capacity of 16 words as shown in Fig. 1. However, the present EMI MWPC has 30 percent better resolution and nine output signals. Further, the event time has been lengthened at the accelerator resulting in additional events per beam spill. In order to take full advantage of these changes, a new digitizer was developed at the Lawrence Berkeley Laboratory (LBL).

This digitizer has nine input channels for accommodating all the signals (2 Xs, 2 Ys, 4 Us and a prompt) from one MWPC (Fig. 2). Also, there is an internal channel that stores a flag for each wrap around of the memory data scaler. By using 1K ECL memories, the digitizer has a capacity of 1024 words and a 33 ns resolution.

Figure 3 is a block diagram illustrating data written into and is read out of the module. For example, data from the MWPC would enter via the front panel (Fig. 4); whereas, data from the computer are transferred into the module from the CAMAC dataway (W1-W22). Lines W1-12 are used for data and lines WT3-22 carry channel numbers (W22 for wrap arounds). On the output lines, R1-12 carry the 12 bits of data; while R13-16 present the channel numbers.

As shown in Fig. 5, data and channel identification are transferred directly into their respective memories, M1-12 and IDO-9. Another important feature of this design is that the memories are constantly updated during a digitizing phase. While such a design greatly simplified the associated logic, it required memories with an access time less than a period of the system's 28 MHz clock (36ns). This problem was solved by the selection of Fairchild's ECL memory 10415A (1024X1)**. A total of 22 such memories are used (one each for the 12 data bits and one for each channel).

WRITE PHASE

A write (digitizing) phase begins when the system's clock transmits to the digitizer the 28 MHz pulse train preceded (120 ns) by a high-to-low level shift in a signal called "Write Permit" (WP). The leading edge of WP initialized the module's address and data counters.

MWPC signals arriving on some or all of the channels causes a '1' to be stored in their respective memories. At the same time, the most recent scaler data is recorded and the address is advanced to the next (one) location. However, in the absence of MWPC signals or wrap around flags, the data memories are still updated while 0's are written into the channel memories. For this situation, the address is not advanced. When no MWPC signals are received but a wrap around occurs, a '1' is stored in the flag memory with all zeros loaded into the other memories (Fig. 6).

READOUT

The readout process from this module is the same whether the data comes from MWPCs or a computer (Fig. 7). Multiword read is employed in a "Last-in/First-out" manner with each word being read on a channel priority basis (highest channel first). Also, during readout there is an automatic hardware conversion from the 22 bit memory format to a 16 bit output format (Fig. 8). All zeros in the data (bits 1-12) represent a wrap around word accompanied by the appropriate channel(s) that receives MWPC signals at this time. Here, the wrap flag has the highest channel number and is therefore always read out first. Bear in mind many digitizers will be storing MWPC data, simultaneously. For software convenience, the first word to be read during any readout process is the module's identification. All subsequence words are formatted as discussed above. A typical data printout is illustrated in Table 1.

TESTS

Phase and temperature tests were performed by varying the times of arrival of all nine inputs, simultaneously, over a period of the system's 28 MHz clock. A divide by 13 was used to provide adequate spacing between successive inputs while producing both odd and even numbers (Fig. 9).

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* This work was done under the auspices of the United States Department Of Energy. Any conclusions or opinions expressed in this report represent solely those of the author and not necessarily those of the Regents of the University of California, the Lawrence Berkeley Laboratory or the United States Department Of Energy.

**Manufactured by Fairchild Semiconductor, Mountain View, California. Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the United States Department Of Energy to the exclusion of others that may be suitable.

RESULTS OF TESTS

1. There are no phase problems with respect to hits arriving at various times of the clock as shown in Table 2.

   A. 1 EVENT = count = 6 x 1024/13 = 472 + 1 WRAP

   B. WRAP = wrap around = 1 (clock = 6)

   C. QERR = 1 for each valid count

   D. CHANA = correct channels are read

   E. VALUE = word value measured against an expected value

   F. CHANR = only valid channels are 0-9

   G. ID = the module's identification

   H. DLY = represents one nanosecond increment. A total of 37 ns covers the 28 MHz clock's period

   Note that zeros mean no errors in Table 2.

2. The unit operates very well for ambient temperatures up to 130°F. This test was performed by enclosing the unit in a box containing a thermocouple and a pancake fan which circulated the hot air.

3. A 30 MHz oscillator was installed in the clock module and tested with this digitizer. Results indicate this digitizer operated well for a 10 hr. period runs.

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Table 1. A typical data printout with all channels receiving data.

177451 (Module's Identification)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
055531	065531	075531	105531	005546	015546	025546	035546	045546	055546	065546	075546	105546	005563	015563	025563
035563	045563	055563	065563	075563	105563	005600	015600	025600	035600	045600	055600	065600	075600	105600	005615
015615	025615	035615	045615	055615	065615	075615	105615	005632	015632	025632	035632	045632	055632	065632	075632
105632	005647	015647	025647	035647	045647	055647	065647	075647	105647	005664	015664	025664	035664	045664	055664
065664	075664	105664	005701	015701	025701	035701	045701	055701	065701	075701	105701	005716	015716	025716	035716
045716	055716	065716	075716	105716	005733	015733	025733	035733	045733	055733	065733	075733	105733	005750	015750
025750	035750	045750	055750	065750	075750	105750	005765	015765	025765	035765	045765	055765	065765	075765	105765
							0	1	2	3	4	5	6	7	8

Channel Numbers

Table 2. A chart of the test results which show zero errors throughout a clock period.

CRATE 1, CLOCK STN 1, DGTZR STN 11, DELAY STN 16 DIGTZR ID 41

ACTIVE CHANNELS 1 1 1 1 1 1 1 1 1 MAX EVENTS 100 KDIV 13

ERROR SUMMARY - TOTAL EVENT = 100 MEMORY ERES = 0/ 0 LAM ERRS 0/ 0

DLY	EVENTS	ID	CHANR	VALUE	CHANA	QERR	WRAP	COUNT
1	100	0	0	0	0	0	0	0
2	100	0	0	0	0	0	0	0
3	100	0	0	0	0	0	0	0
4	100	0	0	0	0	0	0	0
5	100	0	0	0	0	0	0	0
6	100	0	0	0	0	0	0	0
7	100	0	0	0	0	0	0	0
8	100	0	0	0	0	0	0	0
9	100	0	0	0	0	0	0	0
10	100	0	0	0	0	0	0	0
11	100	0	0	0	0	0	0	0
12	100	0	0	0	0	0	0	0
13	100	0	0	0	0	0	0	0
14	100	0	0	0	0	0	0	0
15	100	0	0	0	0	0	0	0
16	100	0	0	0	0	0	0	0
17	100	0	0	0	0	0	0	0
18	100	0	0	0	0	0	0	0
19	100	0	0	0	0	0	0	0
20	100	0	0	0	0	0	0	0
21	100	0	0	0	0	0	0	0
22	100	0	0	0	0	0	0	0
23	100	0	0	0	0	0	0	0
24	100	0	0	0	0	0	0	0
25	100	0	0	0	0	0	0	0
26	100	0	0	0	0	0	0	0
27	100	0	0	0	0	0	0	0
28	100	0	0	0	0	0	0	0
29	100	0	0	0	0	0	0	0
30	100	0	0	0	0	0	0	0
31	100	0	0	0	0	0	0	0
32	100	0	0	0	0	0	0	0
33	100	0	0	0	0	0	0	0
34	100	0	0	0	0	0	0	0
35	100	0	0	0	0	0	0	0
36	100	0	0	0	0	0	0	0
37	100	0	0	0	0	0	0	0
38	0	0	0	0	0	0	0	0
39	0	0	0	0	0	0	0	0
40	0	0	0	0	0	0	0	0

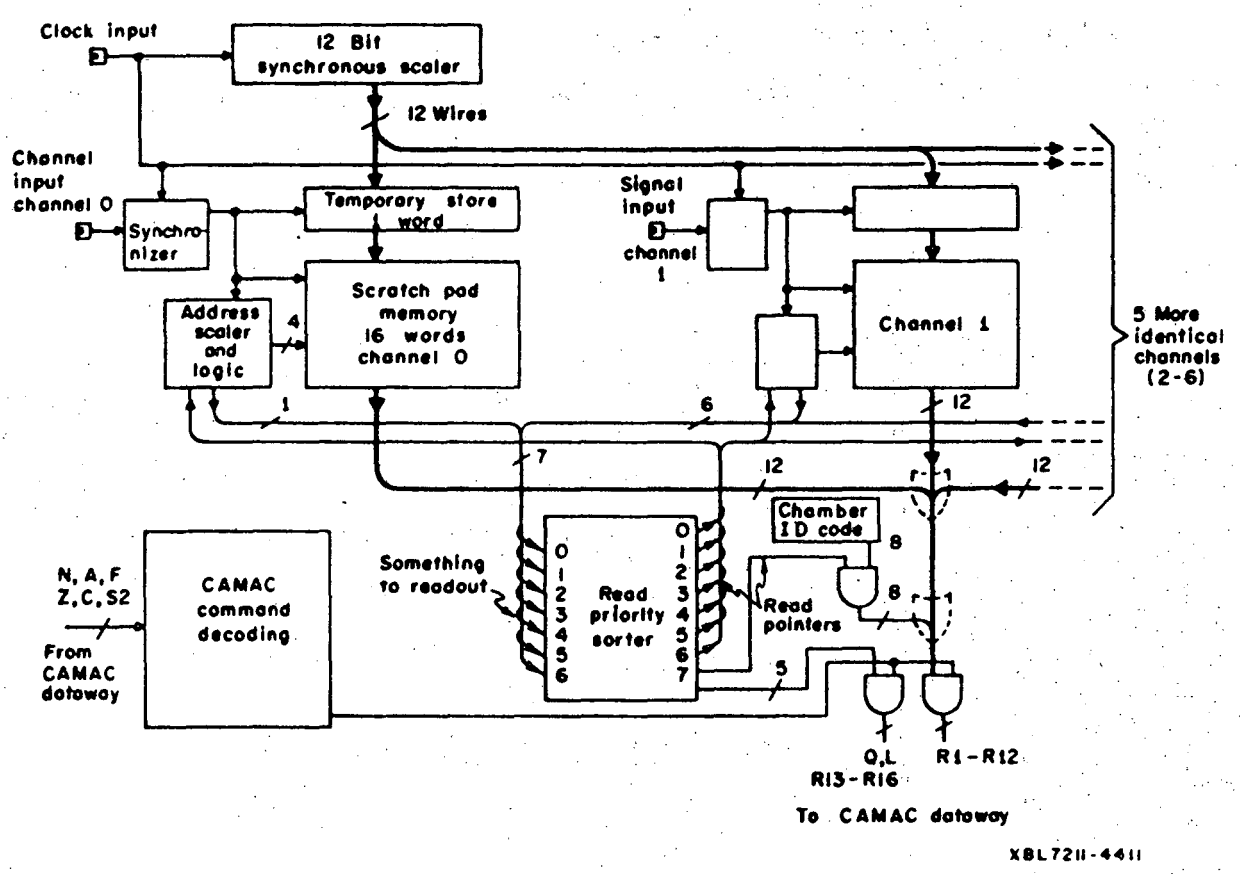

Fig. 1. Block diagram of the first EMI Seven Channel Digitizer

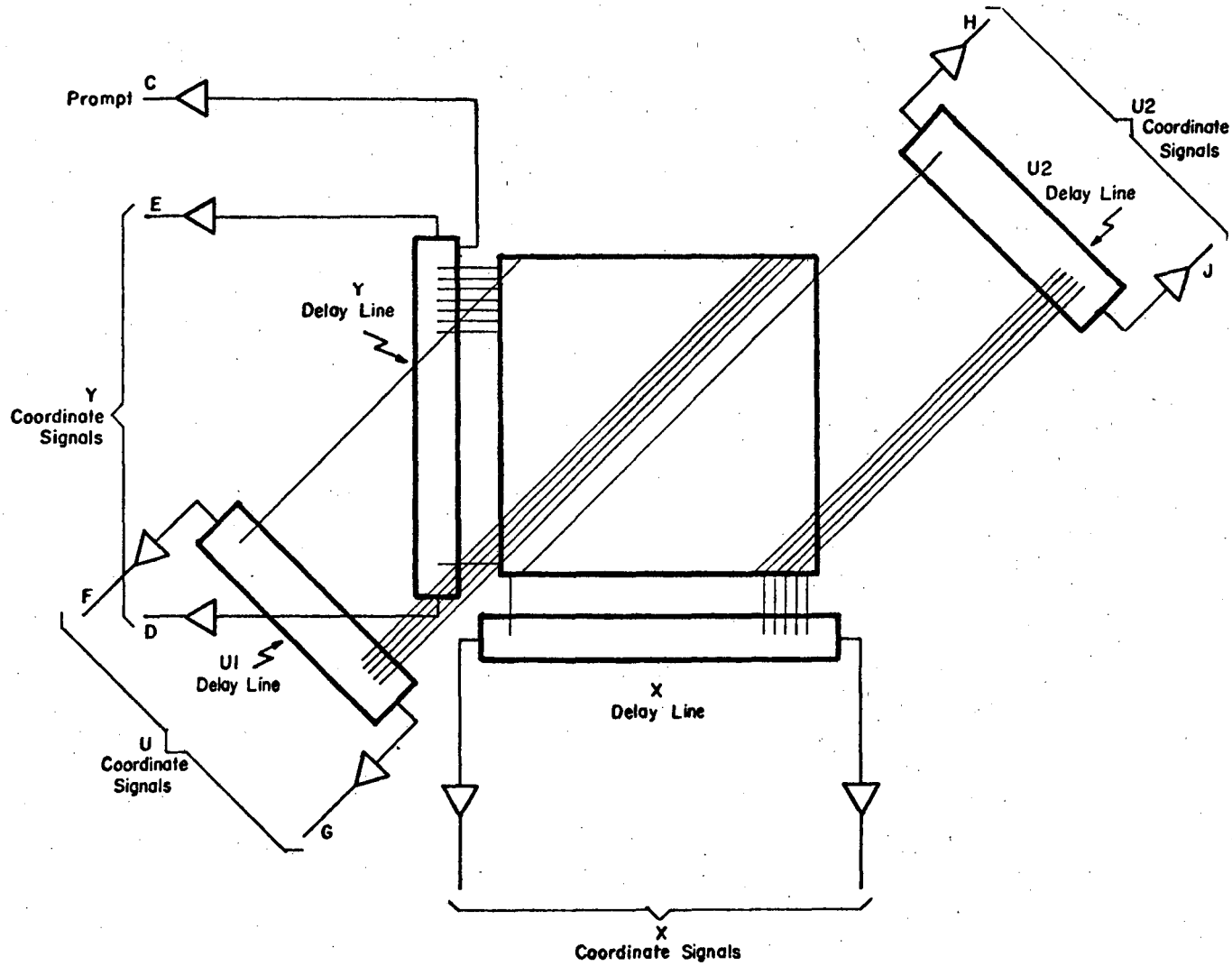

Fig. 2. A simplified schematic of present MWPC. Note that the U plane is now split to give added redundancy.

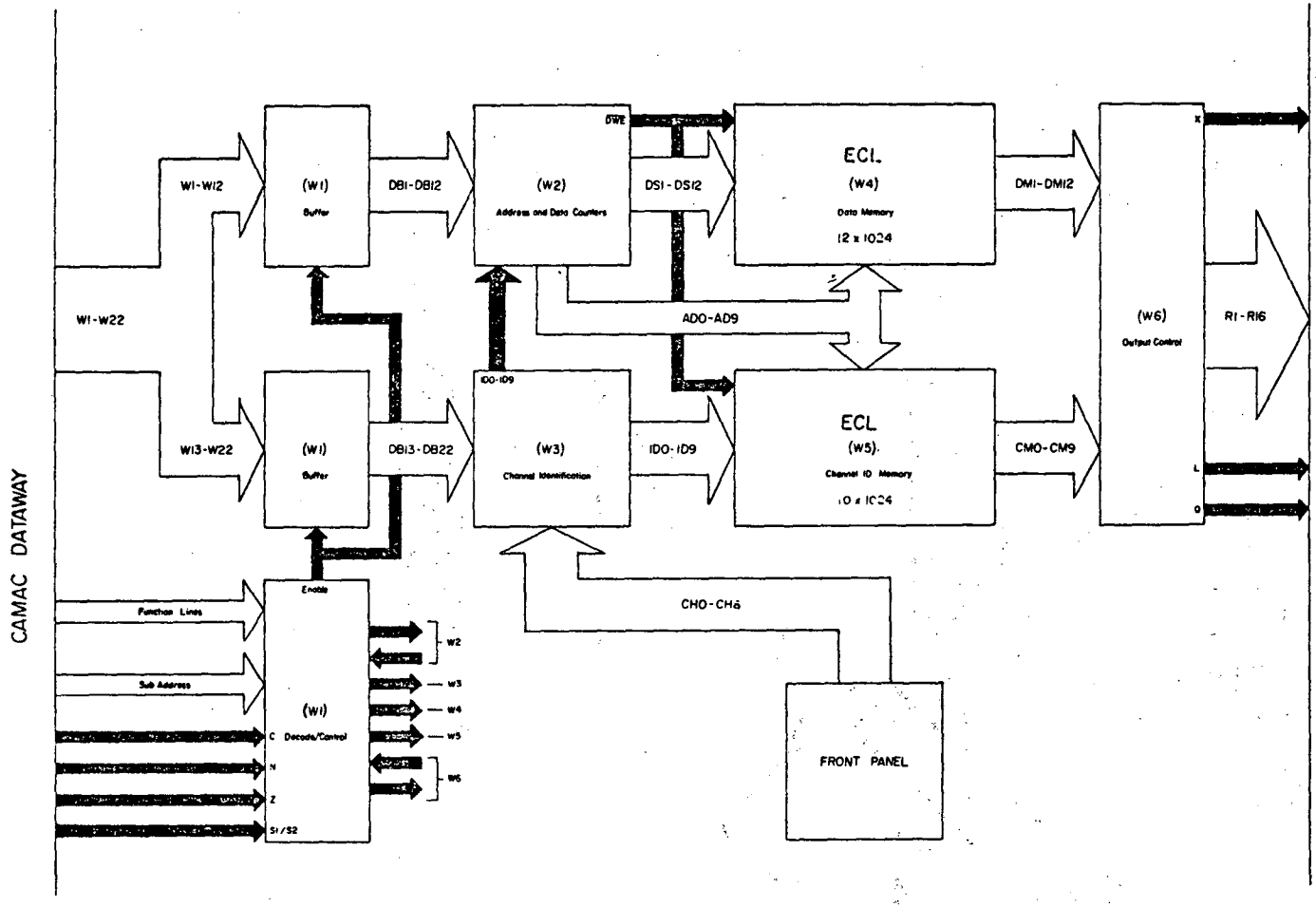

Fig. 3. This block diagram presents the overall layout of the module.

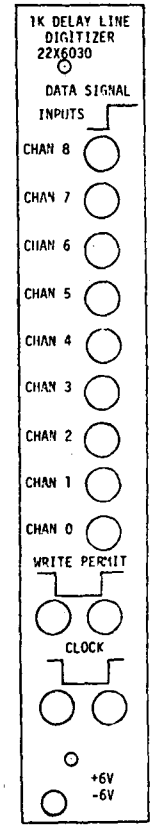

Fig. 4. Front Panel for the 1K Delay Line Digitizer

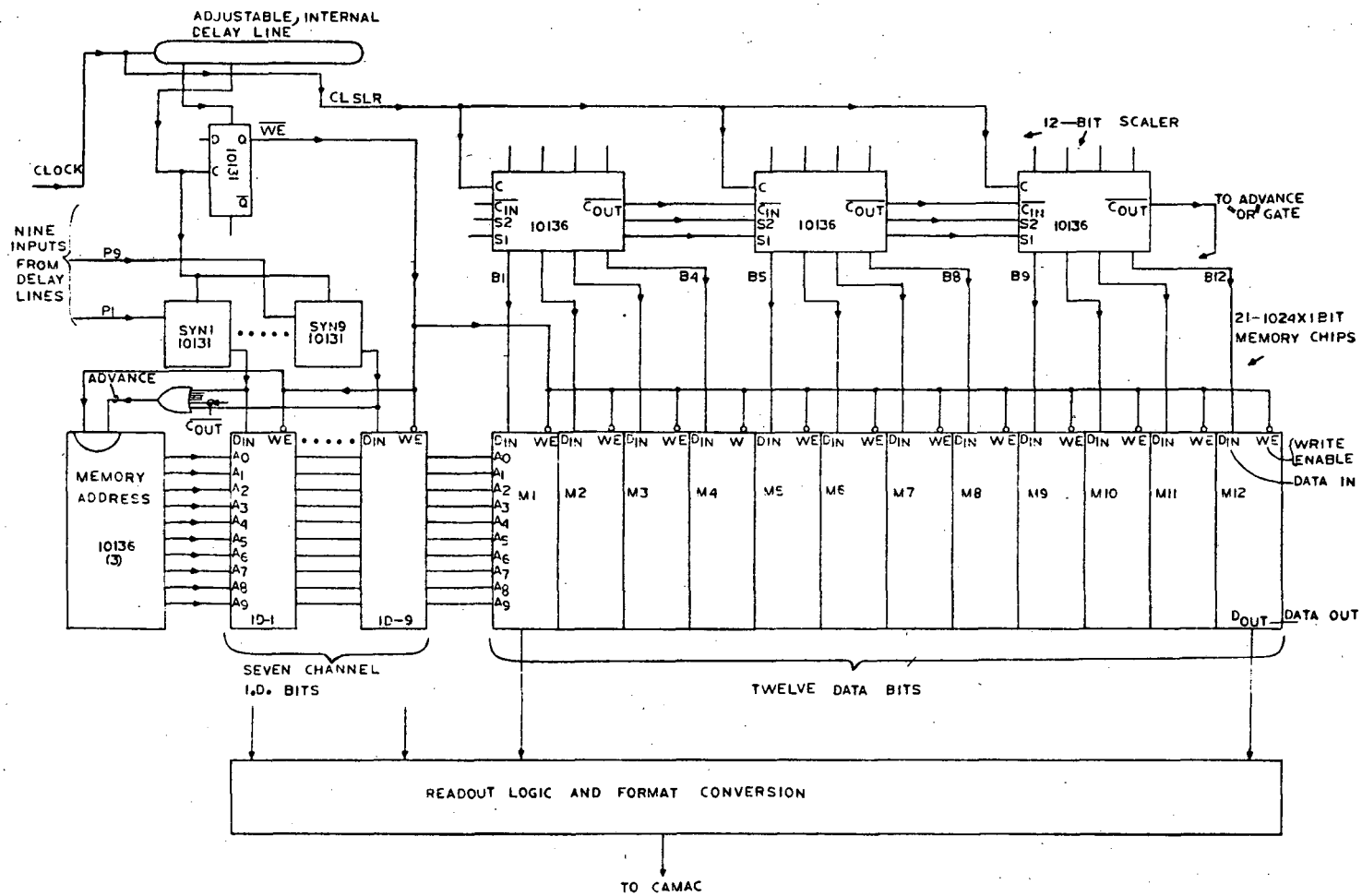

Fig. 5. Schematic representation of how the digitizer processes the 12 bits of data and the 10 channels

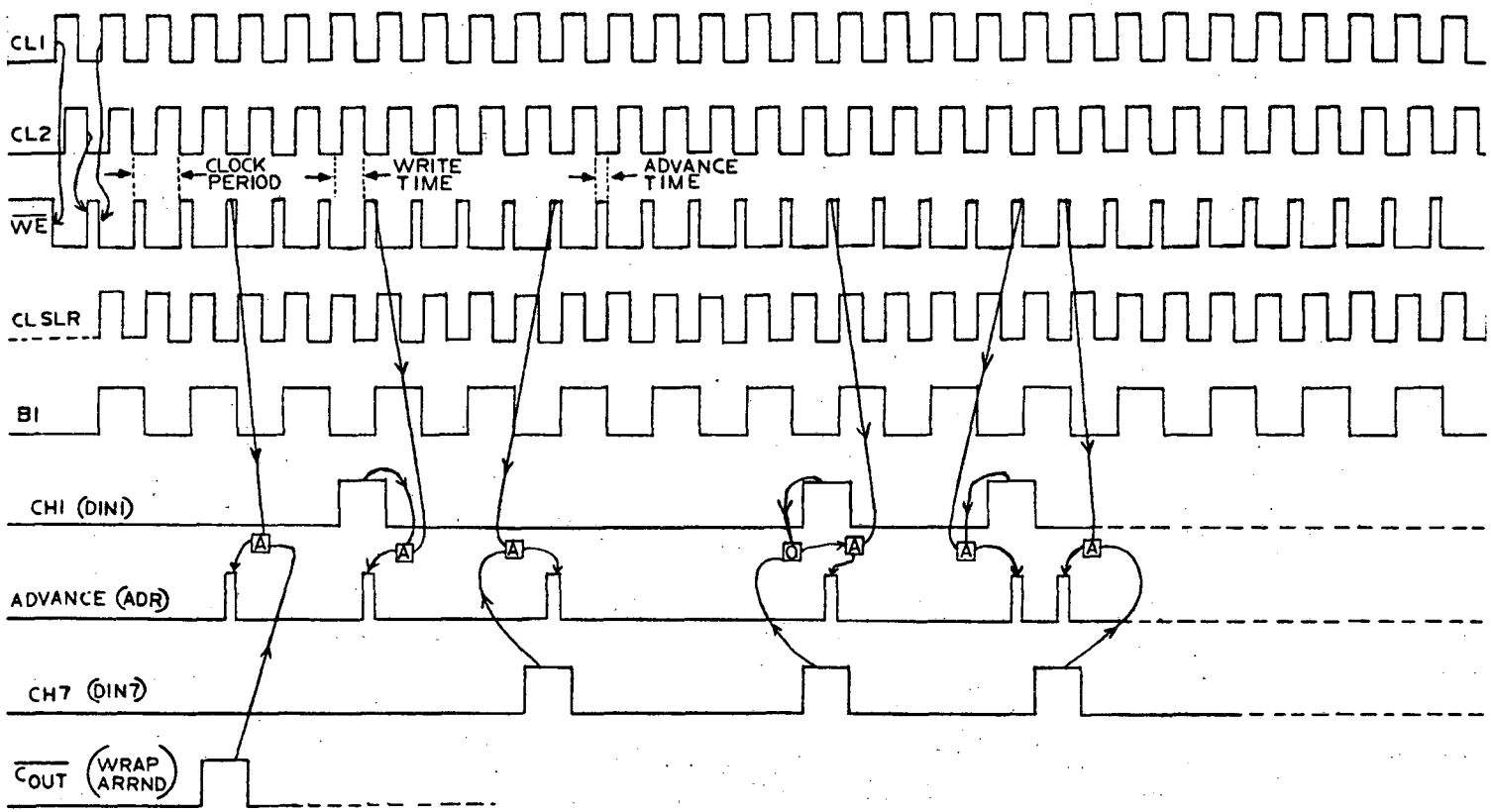

Fig. 6. A timing diagram that illustrates how and when the memory addresses are advanced.

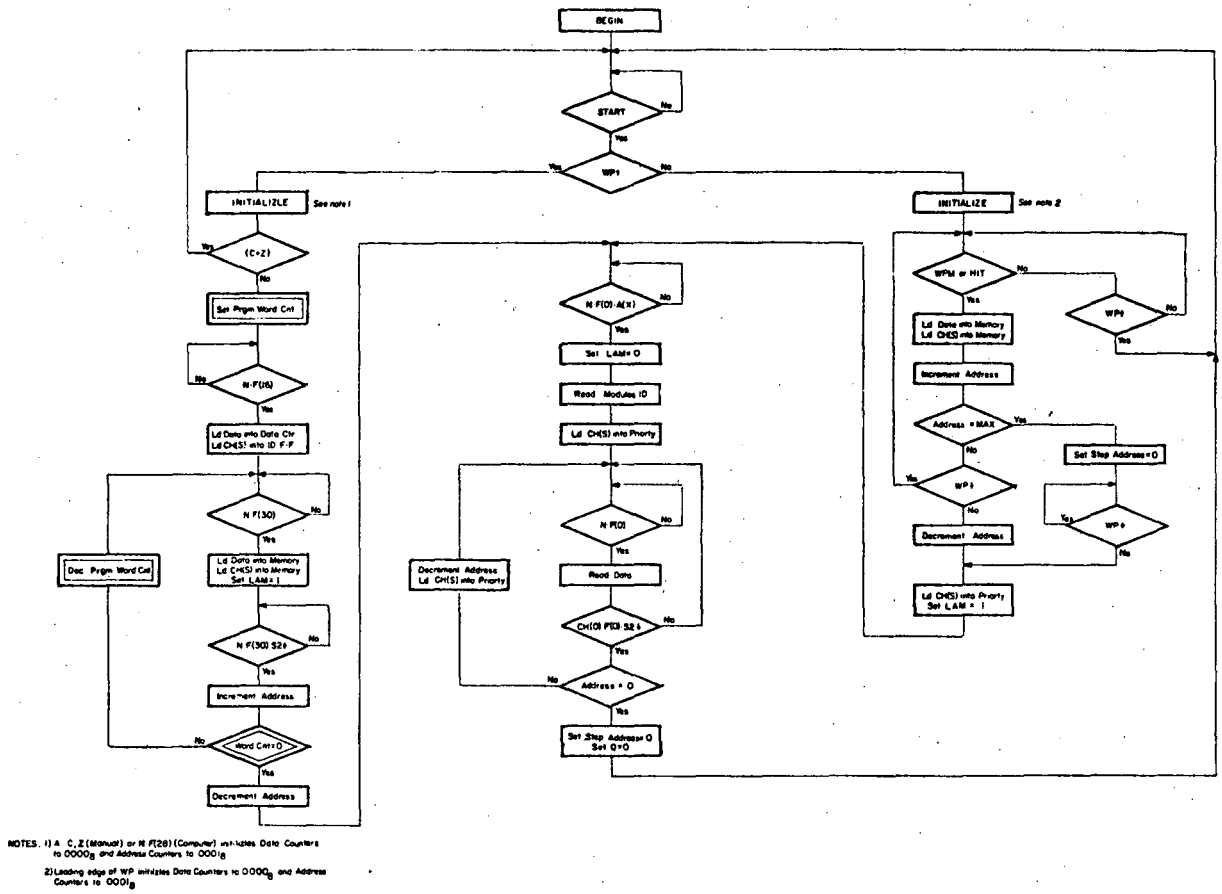

Fig. 7. Flow chart which shows the readout process is the same regardless of data source.

Automatic Conversion between Memory Format and Output Format .

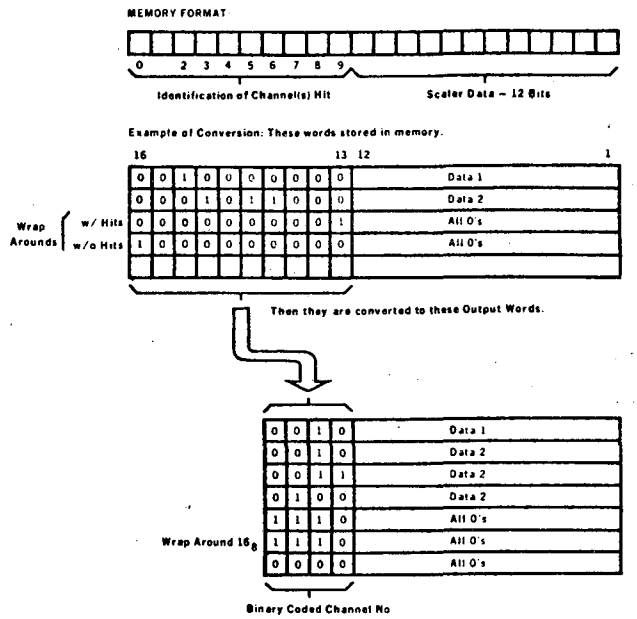

Fig. 8. Format diagram indicating the conversion from a 22-bit memory format to a 16-bit output format. The wrap flag is represented as 16_8 in the output.

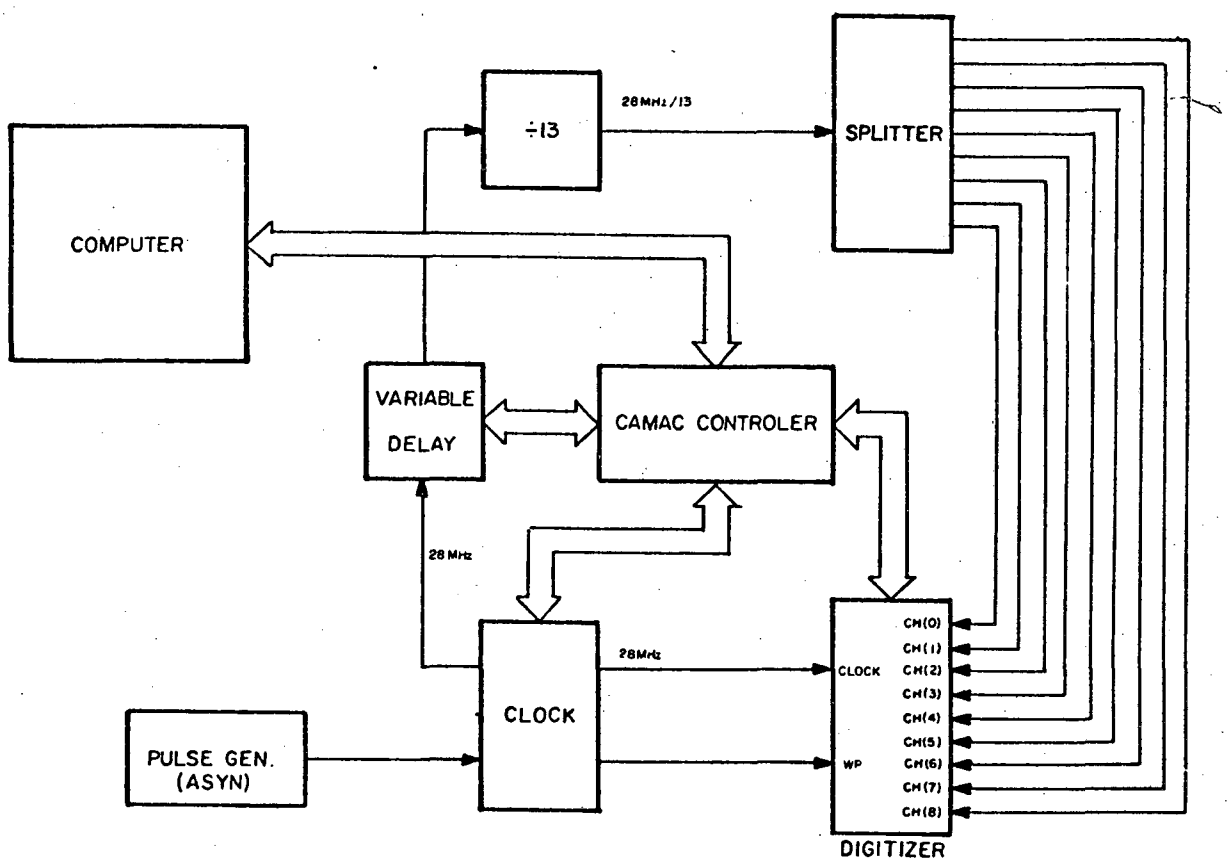

Fig. 9. An outline of the method used to see whether the digitizer was sensitive to input signals arriving at various phases of the clock.

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