Processing Issues in Top-Down Approaches to Quantum Computer Development in Silicon

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Electron and nuclear spins of ^{31}P atoms in silicon are promising candidates for the realization of a scalable solid state quantum computer architecture.[1,2] Three components are required in order to fabricate a test device: 1] an array of single, activated ^{31}P atoms, 2] integrated control gates and 3] single spin readout devices.

Single ion implantation with low energy (<10 keV), highly charged ions offers a path to the formation of single ^{31}P atom arrays. We describe our development of single ion placement technology and discuss the means by which individual ^{31}P atoms may be activated and the damage associated with the implantation process repaired.[3] Figure 2 shows the low activation ratios for low dose P implants and the effect of a co-implant of Si in increasing the activation ratio.

In the original Kane proposal[4] the qubit spacing of 20 nm is dictated by the need to ensure direct wavefunction overlap between neighbouring ^{31}P atoms – with corresponding gate pitches of 10 nm, beyond the current state of the art in lithography. Using "electron shuttling" as a means of entanglement relaxes this requirement, up to 1 –10% of the spin coherence path length for the shuttled electrons.[1] This path length has to be determined experimentally, but is expected to be on the order of 1 μm. We will discuss the need for gate pitch optimization with regard to the spin coherence path length, qubit encoding schemes and the limits of the nanofabrication process.

Single electron transistors (SET's) are promising candidates for single spin readout devices.[5] The need for large-scale integration makes formation of SET's in Si highly desirable. Figure 3 shows an SEM image of the initial stages of the Si-nanowire based SET fabrication process. We will present the latest results from our Si-SET program and discuss the various limitations of the overall fabrication scheme.

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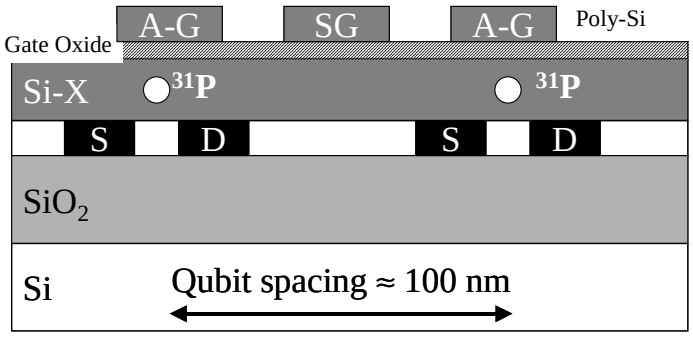

Figure 1. Conceptual layout of a two-qubit test structure.

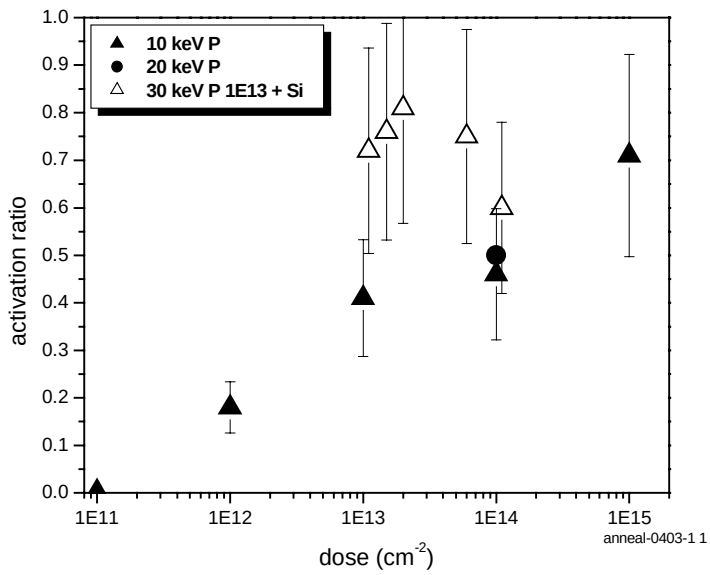

Figure 2. Activation ratios determined by spreading resistance analysis as a function of ion dose. The corresponding dose for a Kane-type solid state quantum computer is 10^{10} – $2.10^{11}cm^{-2}$. The open symbols show the results of adding an increasing Si dose to a base dose of 10^{13} P. All samples were annealed for 1 minute at 1000 C in a N_2 atmosphere.

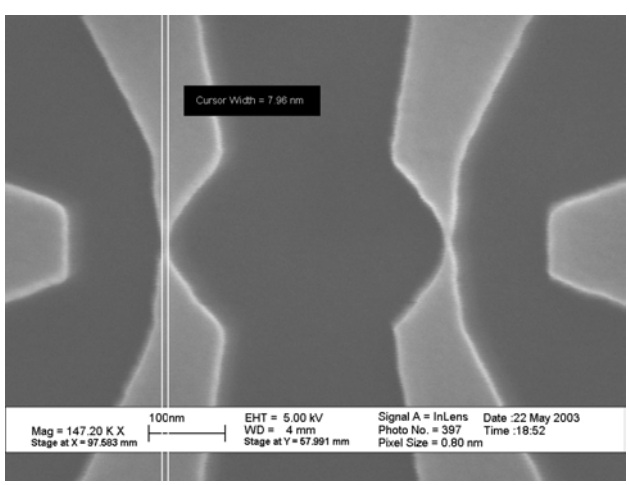

Figure 3. SEM of a potential Si SET-pair structure defined in HSQ resist.