

ALS Control System IP I/O Module Upgrade*

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Abstract. The Control System for the Advanced Light Source uses in-house designed IndustryPack (IP) I/O Modules in compact PCI (cPCI) chassis to control instrumentation. Each module consists of digital I/O ports and 16-bit analog I/O interfaced to instrumentation via a cPCI rear I/O card. During the past few years of installed operation, several factors have prompted investigation into the design of a new IP I/O Module. The ADC channels have significant offset drift over periods of days of initial installed operation. An in-situ calibration procedure was developed to address this problem, but it lacks speed and is inconvenient to perform. Digital I/O port limitations have led to increasing amounts of wasted I/O. Fast orbit feedback requires faster ADC sampling and better filtering than the current IP module offers. This paper discusses the issues related to the current IP I/O Module and the design of a new Double-size IP I/O Module.

INTRODUCTION

The ALS Instrumentation Group designed custom IP Modules for the ALS Control System. Housed in cPCI crates, these modules control instruments such as magnet power supplies and beam position monitors (BPMs). Each IP Module consists of two 8-bit digital I/O ports, two 16-bit analog control channels (DACs), and four 16-bit analog monitor channels (ADCs). The modules interface to instrumentation via a custom cPCI rear I/O card. To increase channel accuracy and make modules interchangeable, each analog channel is calibrated for gain and offset compensation and the calibration data is stored in an onboard EEPROM. After several years of installed operation including changes to the control system and implementation of fast orbit feedback at the ALS, the cPCI-based hardware requires an upgrade. This upgrade will keep intact the hardware infrastructure of existing IP Carriers, cPCI chassis, and I/O Controllers (IOCs) while new versions of the IP Module and cPCI rear I/O card will replace the existing ones. The motivation for and design of the new IP Module will be presented.

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MOTIVATION

Several factors motivated the IP Module upgrade. First, long term monitoring of installed IP Modules revealed that the ADC offsets drift gradually up to 25mV in the first month of installation. The ADC data sheet specifies a maximum zero offset error of $\pm 10\text{mV}$ with a typical drift of $\pm 2\text{ppm}/^\circ\text{C}$. ALS instrumentation and control requires a maximum drift of less than 10mV/year. Since the ADC offset drift is well outside the component specifications and ALS operational requirements, an in-situ calibration procedure was developed to recalibrate installed IP Modules. The in-situ calibration compensates for the ADC offset drift, but performing the procedure is inconvenient and time-consuming.

Second, after the IP Modules were installed, developments in the fast orbit feedback required greater precision from the IP Module DACs controlling corrector magnets. To meet this requirement, a second version of the cPCI rear I/O card was developed which contains a 16-bit trim DAC divided by ten and summed with the output of each IP Module DAC for an effective resolution of $19\frac{1}{2}$ bits. This version of the cPCI rear I/O card is installed only in locations used by the fast orbit feedback. As a result, there are different versions of the card in different locations which complicates maintenance and troubleshooting of control system hardware.

Finally, upgrading or modifying the IP Module firmware requires replacing the configuration PROM for the FPGA. To replace the PROM, the IP Carrier must be removed from the cPCI chassis and the IP Module removed from the IP Carrier. The ALS Control System currently uses over one hundred IP Modules making firmware upgrades and modifications laborious. The IP2 Module uses an in-system programmable PROM that replaces the one-time programmable PROM, which greatly increases the flexibility of the FPGA firmware.

DESIGN

Physical Characteristics

IP Modules are installed in SBS Greenspring cPCI IP Carrier boards. Each IP Carrier has four IP slots and can accommodate up to four single IP Modules or two double-size IP Modules. The new Double-size IP I/O Module (IP2 Module) has twice the I/O capability of a single IP Module, maintaining the current number of analog and digital I/O channels per IP slot while freeing IP Module board space for additional features. The size of the IP2 Module (3.6" x 3.9") presented a challenge for the board layout, which resulted in a 10 layer board with components tightly packed together on both the top and bottom of the board. Figure 1 shows the IP2 Module next to its predecessor, the IP Module.

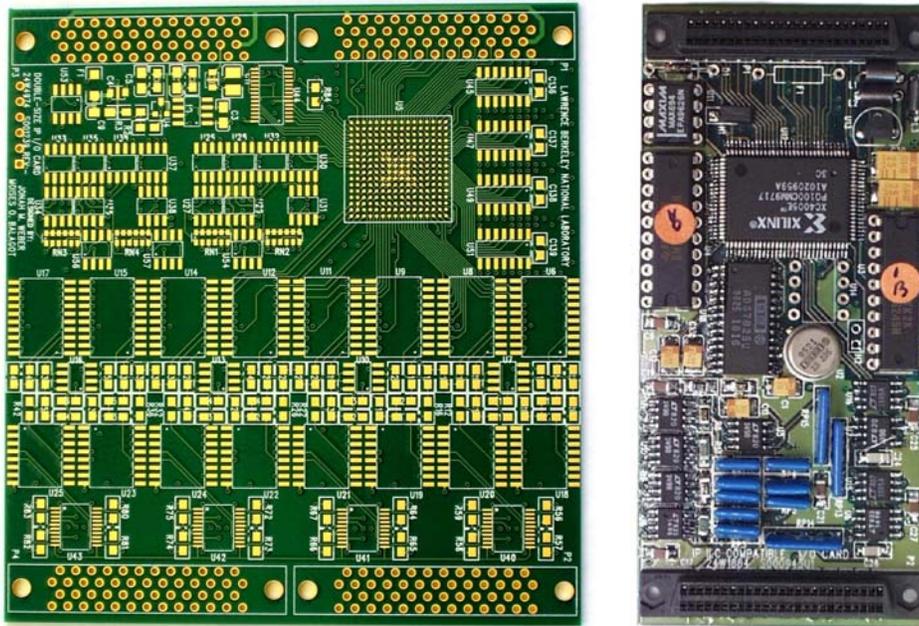


Figure 1. The IP2 Module top side (left) and the IP Module top side (right).

The IP2 Module has two logic connectors and two I/O connectors, one of each per IP slot. All signals on each I/O connector are pin compatible with the IP Module so that the modules may be interchanged if necessary. This allows use of the IP2 Module with existing and new cPCI rear I/O cards. One of the IP2 logic connectors is used as the IP bus interface and the other has only power and ground connections. Although the IP bus interface is the same in both modules, the IP2 Module has a modified register map requiring development of a new software driver. A block diagram of the IP2 Module design is shown in Figure 2.

FPGA Programming

The IP Module contains an FPGA that interfaces the IP bus to I/O. Since the FPGA has volatile memory, it uses a PROM for configuration on power-up and reset. The current IP Module uses a one-time programmable configuration PROM, which must be replaced to update the FPGA logic design. To replace a PROM on an installed IP Module, the module must be removed from the cPCI chassis and the IP Carrier. As the control system expands requiring greater I/O capability, replacing every PROM is an increasingly laborious process. To allow easier reprogramming of the FPGA, the IP2 Module uses an in-system programmable PROM accessible both onboard and through a connector on the new cPCI rear I/O card.

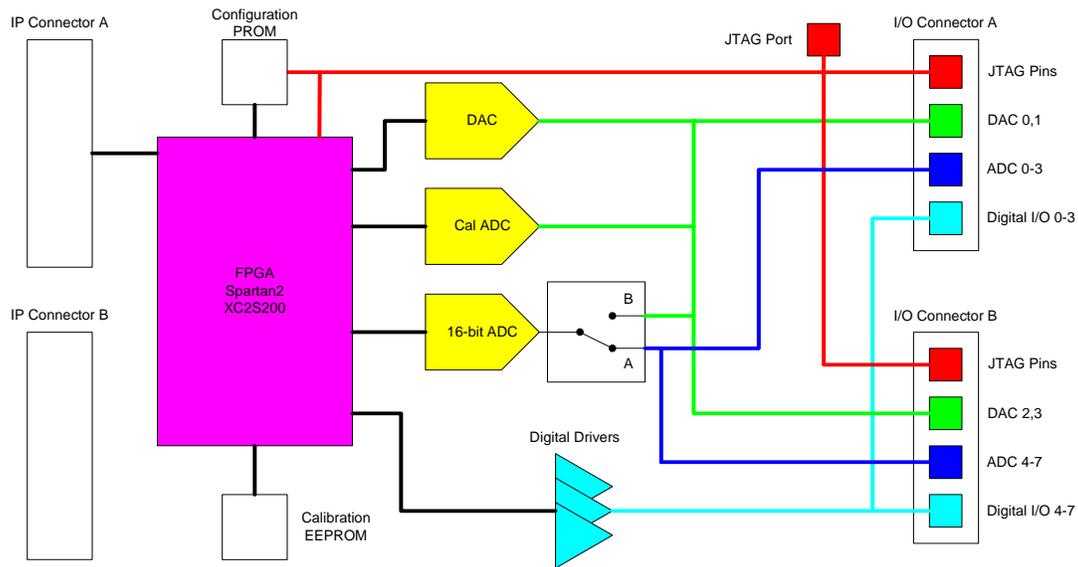


Figure 2. Block diagram of the IP2 Module design.

Digital I/O

The IP Module contains 16 bits of digital I/O in two 8-bit ports. The direction of each port is controlled independently. Since many applications do not require digital I/O in 8-bit increments, some bits of the digital I/O ports are unused and inaccessible. The IP2 Module contains 32 bits of digital I/O available on eight 4-bit ports. These ports allow greater direction flexibility for the digital I/O while maintaining 16 bits of digital I/O per IP Slot.

Analog Inputs

The IP Module has four 16-bit differential analog input channels on a single multiplexed ADC (Burr Brown ADS7825) sampling continuously at 10 kHz per channel. To achieve greater performance from the fast feedback, the analog inputs must sample at a higher rate for more effective filtering. Accelerator Physics also desires greater resolution from the ADC channels. The IP2 Module analog inputs must accept $\pm 10V$ differential signals. To eliminate ADC offset drift, a different ADC component and PCB assembly house are used for the IP2 Module.

The IP2 Module boasts 8 independent 16-bit analog input channels sampling at 200 kHz each with programmable gain settings of 1, 2, 4, and 8. The LTC1609A ADC used for each input accepts $\pm 10V$ differential signals. The LTC1609A noise

and linearity specs are comparable to the ADS7825 used on the IP Module. The programmable gain circuit on each analog input increases the LSB resolution from 305 μV over a $\pm 10\text{V}$ range to 38 μV over a $\pm 1.25\text{V}$ range. Each channel has a 100 kHz analog anti-aliasing filter. Additional digital filtering capability is available within the FPGA to accommodate fast feedback sampling. Figure 3 shows one of the IP2 Module analog input channels.

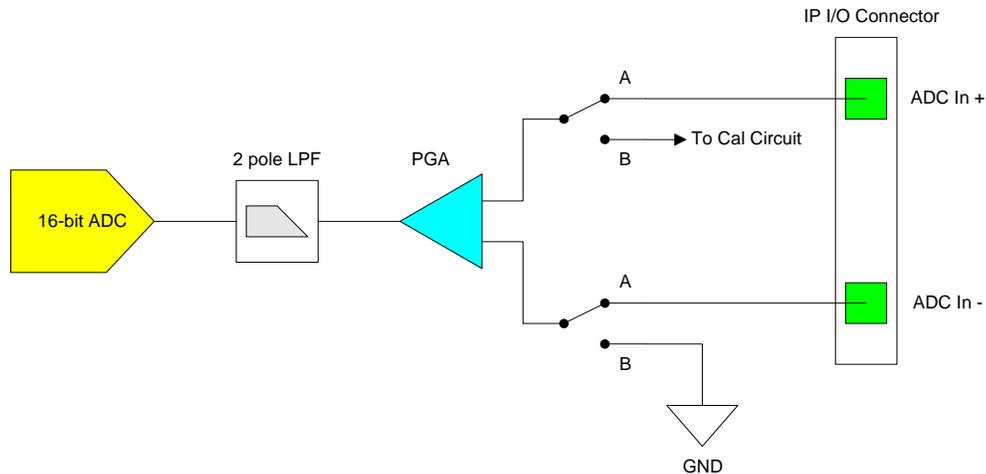


Figure 3. IP2 Module analog input circuit block diagram.

Analog Outputs

The IP Module uses two LTC1595 16-bit DACs for analog control. Development of the fast orbit feedback required greater precision from the DACs to control corrector magnets. An additional version of the cPCI rear I/O card was designed and is currently installed to interface to instrumentation used by the fast feedback. This card includes an LTC1595 “trim” DAC divided by ten summed with the output of each IP Module DAC to create analog output. This coarse and trim DAC circuit has proven effective for fast feedback control and is used in the new IP2 Module design.

Each IP2 Module contains four analog output channels consisting of two LTC1595 DACs. Figure 4 shows one analog output channel. As with the cPCI rear I/O card, each coarse DAC is summed with a trim DAC divided by ten to achieve an effective 19½-bit resolution. Since the trim DACs are onboard, they can be controlled directly by the FPGA, and each DAC summing circuit requires fewer precision components to control the gain of the DAC outputs.

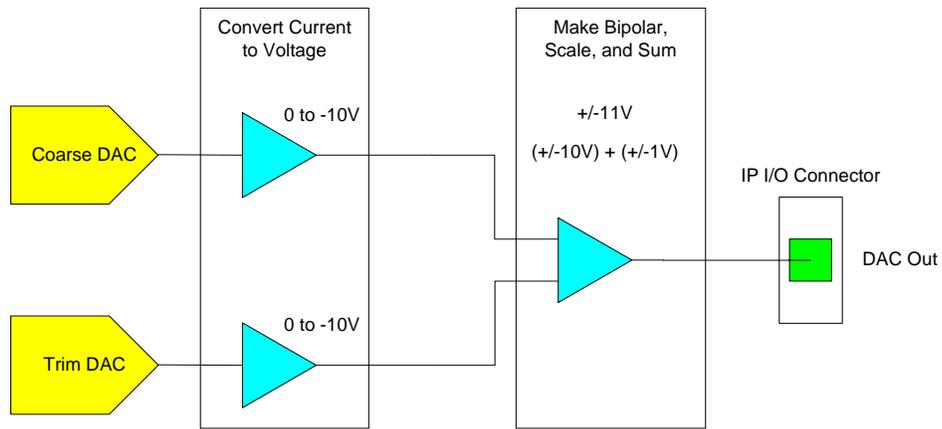


Figure 4. IP2 Module analog output circuit block diagram.

Analog I/O Calibration

Presently, an in-situ calibration system consisting of a laptop, voltmeter/switch unit, custom cable harness, and LabVIEW calibration software is used to calibrate analog channels. The procedure involves swapping cables and porting a laptop and voltmeter/switch unit to each cPCI chassis requiring calibration. The IP2 Module includes an onboard analog calibration circuit shown in Figure 5. Calibration can be performed without any additional test fixtures or cable swapping by switching the analog inputs to an internal network. The control system uses calibration software to generate the calibration constants.

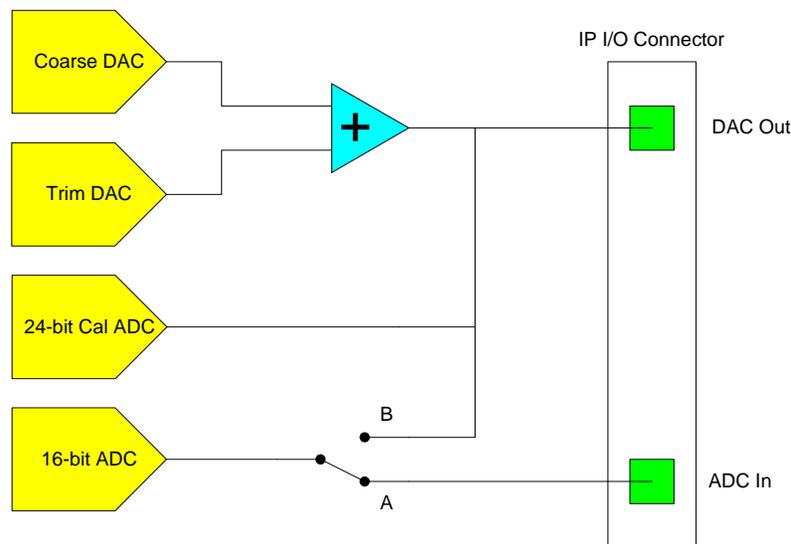


Figure 5. IP2 Module analog calibration circuit block diagram.

SUMMARY

The ALS Control System hardware upgrade consists of designing new versions of both the IP Module and the cPCI rear I/O card. The IP2 Module addresses the ADC offset drift with a different ADC and in-circuit calibration capability. It accommodates developments in fast feedback requirements by providing onboard trim DACs and superior filtering potential with front end analog filters on ADC inputs and digital filtering capability in the FPGA. The IP2 Module adds the convenience of in-system FPGA configuration to increase the flexibility of the FPGA program. In addition, the IP2 Module features programmable gain on ADC channels to allow greater precision in monitoring physics experiments. Finally, 4-bit digital I/O ports reduce wasted bits by increasing the flexibility of the digital I/O.

The IP2 Module PCBs have been fabricated and are currently in the prototype testing stage. Once working prototypes have been initially tested, a few IP2 Modules will be installed in a test cPCI chassis in the ALS storage ring for further testing and ADC offset drift characterization. The projected permanent installation date for the first set of IP2 Modules is early 2005.

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