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AUTOMATIC CONTROL SYSTEM FOR DETECTION OF NUCLEAR MAGNETIC RESONANCE

C. C. Wang

August 3, 1967

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ABSTRACT

An automatic control system for detection of the nuclear magnetic resonance is described. The system is the combination of the commercially available instruments and the modular units developed in the Lab. The frequency of interest is anywhere between 100 Mhz and 900 Mhz. The range of the frequency sweeping is determined by the sample under observation, which is seldomly over 100 Mhz. The accuracy of the frequency repetition is within 100 Khz.

INTRODUCTION

The absorption of energy from an oscillating magnetic field by nuclei subject to a fixed magnetic field of a few hundred gauss enable the processional frequency and the nuclear g-factor to be determined. The combination of perturbed angular correlations and nuclear magnetic resonance provide a technique for investigating hyperfine interactions in short lived excited nuclear states.

In the experiment to detect nuclear magnetic resonance, the experimenter sets two 3-in. × 3-in. NaI(Tl) counters at 180° to record the coincidences. The analyzer is in the multi-scaler mode of operation. The sample was polarized in a strong dc field along the counter axis. Perpendicular to this field, an oscillating field is swept back and forth in a pre-determined frequency range f1 and f2 by a fixed amount Δf in each step. Starting from channel zero, each successive channel in the analyzer corresponds to the incremented frequency. The frequency of interest is anywhere between 100 Mhz and 900 Mhz depending upon the sample under observation. The swing of the frequency is, however, seldomly over 100 Mhz. Resonant absorption is detected by the drop in the coincidence rate centered at a certain frequency, which is observed as a dip in the analyzer.

In doing this kind of experiment, the frequency was swept manually. The time for each frequency setting is around five minutes. Since the sample under observation is short lived, the experiment therefore has to be completed in a short period of time. One could imagine that it would be a painful experiment if certain results were to be expected after two days or so. Therefore, it was urgent that the experiment be automated. This report is to describe this automatic control system which is now used at LRL Berkeley.

THE SYSTEM OPERATION

The block diagram for the automatic control system is shown in Fig. 1. As should be noticed, this system is the combination of the commerically available instruments and the modular units developed in the lab. The commercial instruments are briefly described. For more information, the reader is advised to look into the catalogs or contact the factories directly. Most of the modular units developed in the lab are presented in the block diagram form and the operations are described in detail.

First of all, the system operation is presented. The initial frequency of the power oscillator can be set by adjusting the "DC level" control pot on the front panel of the step voltage generator (15X9432). In the initial design of the step voltage generator, the output step voltage happens to be going downward and then upward; therefore, the initial frequency is to be set such that it is the highest one. The frequency counter displays the frequency and the H. P. digital to analog converters put out a dc level proportional to those columns which are selected by the column selected by the column selectors. The information in column five of the frequency counter is taken out from the fifth column board of H. P. 562A as the inputs to the DAC sixth column control unit (15X9873). The information in the said column is used to control the dc level shift when column six of the frequency counter is changed by ±1 digit (more details will be given later). Through a proportional summing amplifier (19X1952), a dc level appears at the other input of the null detector. The two-phase motor is turning in such a direction that the dc level from the step voltage generator and that from the summing amplifier are to be the same. In the null state, the two-phase motor is stopped and the initial condition is thus set.

On the front panel of the TIBO (switch programmed time base oscillator, 15X9410, has two time bases, i.e. $\Delta T1$, $\Delta T2$. See more details on page 5), suppose that the $\Delta T1$ time base is set to be five minutes and the $\Delta T2$ time base is set to be 15 sec. Let's follow the loop shown in the block diagram starting from the TIBO and observe how the system is operating.

Push the "start push button" to start the TIBO. After five minutes $\Delta T1$ pulse is generated and the step voltage generator puts out a lower dc level. Notice that the H.P. printer gate (15X9862) is also executed at this time. Therefore, the first frequency is printed by the printer. In the meantime, the null detector senses the difference and hence drives the two-phase motor. Through a directional coupler, the frequency counter reads the frequency of the oscillator and generates 1248 positive logic code to the digital to analog converters. Therefore, out of the summing amplifier, a dc level in proportion to those digits selected by the column selectors is shown on another input of the null detector. The motor will keep turning until the two inputs of the null detector are balanced. A new frequency is thus reached. It usually takes about 10-15 sec. One cycle of operation is complete. Another five minutes later, the same cycle will be executed and the same process keeps going on. The direction of the motor and hence the frequency sweeping are controlled by the step voltage generator. The system operation can be stopped if TIBO, which is the master of the system, is called to stop.

DESCRIPTION OF INSTRUMENTS

1. C202 Power Oscillator

Model C202 high power signal generator is developed and manufactured by Applied Microwave Laboratory, Inc., Andover, Massachusetts. The C202 covers the

frequency range from 150 to 950 Mhz with the nominal power of 100 W for the plug in head that covers frequency from 150 to 500 Mhz and 50 W for the plug in head that covers frequency from 500 to 950 Mhz. The nominal power represents the maximum power available. The average life time of the power tube in the oscillator is 500 hr for continuous use.

2. 945 Frequency Counter

Model 945 is a direct frequency counter. The operation range is from dc to 4 Ghz. The good feature of this counter is that in high frequency measurement the "direct" counting eliminates the need for heterodyne and transfer oscillators. The 1248 positive logic BCD is available at the back of the instrument. Model 945 is manufactured by Eldorado Electronics.

3. H. P. 562A Printer with the Digital to Analog Converter

This unit is a special order from Hewlett Packard. Its functions are to accept the BCD signal from the frequency counter, change it proportionally to a dc voltage and print the frequency shown in the frequency counter. In the automatic control system described, the columns are selected to transfer the information in columns 3, 4, and 5 of the frequency counter. The printer is gated by the H. P. printer gate (15X9862) so that it can only print when the gate is executed.

4. H. P. 580A Digital to Analog converter

This is another special order from Hewlett Packard. Its function is to respond to the BCD signal from the frequency counter and is the same as that of H. P. 562A DAC. However, the columns are selected to transfer the information in columns 1 and 2 of the frequency counter.

5. Null Detector

The null detector and the two-phase motor are a part of type G recorder made by Leeds and Northrup Company. The sensitivity of the null detector is affected by several factors, i.e. the noise from the summing amplifier and that of the step voltage generator, and the mechanical efficiency loss when the motor is driving the shaft of the frequency control pot in the C202 power oscillator through a chain of gear links. The noise was found to be approximately 2 mv (peak to peak). Therefore, it was not surprising that the null detector failed to respond to the two or three digits change in column 2 of the frequency counter, which represents 1 mv per digit in the system.

6. TIBO (15X 8410)

This is a switch programmed time base oscillator and was designed for use with most of the multi-channel analyzers in the multiscaler mode of operation. There are two time bases, namely, $\Delta T1$ and $\Delta T2$. TIBO may be switched from 10 μsec per channel to 990 sec per channel for one time base. With both time bases used, the maximum time can be 2 × 990 sec or 33 min per channnel. When the automatic control system is under operation, $\Delta T1$ time base is usually set to be five minutes while $\Delta T2$ time base is set to be 15 sec. In $\Delta T1$ time, the coincidences are recorded in the analyzer through the TIBO. The $\Delta T2$ time (15 sec) is the time for the motor to drive to the next frequency. In this period, the detector pulses are blocked by the TIBO. Therefore, no false information would be collected by the analyzer. At the end of $\Delta T2$ time base, the gate is opened and the analyzer sees the coincidences in the new frequency.

7. The Step Voltage Generator (15X9432)

The step voltage generator is essentially a binary count-up and count-down scaler together with a diode network and output amplifiers functioning as a digital to analog converter. The block diagram is shown in Fig. 2.

The binary scaler is ready to count up after reset (since the output amplifiers invert the signal out of the diode network, so the actual step voltage is ready to go down). The UP output leg of the "up and down control flip-flop (UNCFF)" is at the low state while the DOWN output is at the high state (see Fig. 2). The switches S1, S2, S3, and S4 are the "number of steps" selection switches. In Fig. 2 the switches are in such a position that when the scaler counts up to 16, there will be a pulse out of "AND gate 2" and hence the UDCFF changes state. From the next pulse on, the scaler will count downward. As all the binarys of the scaler reach zero state, "AND gate 1" is executed and the UDCFF changes state again. The scaler is ready to count up when the next pulse comes and the same precess keeps going on. The diode network transfers the digital information into dc voltage which in turn is amplified by the output amplifiers and appears at the output as the step voltage.

Each time when the UDCFF changes state, the pulse forming networks generate a 4 μsec pulse which, after amplified by the output amplifier, serves as the overflow pulse that resets the address of the analyzer back to channel zero. If the "overflow control switch" is in X1 position, the overflow pulse is generated only when the binary scaler reaches zero state. If the switch is in X2 position, the overflow pulse will be generated both when the binary scaler reaches zero state and reaches a state determined by the switches S1, S2, S3, and S4.

The noise was found to be approximately 2 mv (peak to peak) out of the step voltage generator and its dc drift is much smaller than the frequency drift

of the oscillator, so it can be neglected. The unit could be reset either by the front panel reset push button switch or by external positive pulses.

8. The H. P. Printer Gate (15X9862)

There is an automatic print command at the end of each count cycle out of the frequency counter. Since it is impractical to print the frequency at the end of each count cycle, once for each new frequency is enough. Therefore, the printer gate is devised in order that the printer can print only when the gate is executed. The block diagram and the timing sequences are shown in Fig. 3. Terminology such as "positive inhibit", "scan" are adopted from the operation manual of H. P. 562A. Referring to Fig. 3, the "positive pulse" comes from TIBO $\Delta T1$ pulse which in the system is generated every five minutes.

The "positive inhibit" and "scan" come from 562A digital recorder, which happen in every count cycle of the frequency counter. They are responsible for the printing of the recorder. The print command output is connected to the clutch solenoid and record switch in H. P. 562A. Normally, if the switch is closed (which can be done manually), the clutch solenoid is energized every count cycle and the frequency is thus printed. It is evident that the function of the H. P. printer gate is to block the printing information from going through unless we desire so, namely, only when $\Delta T1$ from the TIBO is presented.

In the steady state, the output of the flip-flop is high so the AND gate is closed. However, when the $\Delta T1$ pulse comes to trigger the flip-flop, the gate is opened. The 25 ms one shot generates a 25 ms pulse (25 ms is required because it takes this long to energize the mechanical link in H. P. 562A recorder). The relay is closed and the frequency corresponding to the time when $\Delta T1$ is presented is printed. Before the 25 ms is terminated, the "scan" is ended inside

H. P. 562A and is used to generate a suitable pulse to reset the flip-flop. Unless there is another ΔT1 pulse to re-trigger the flip-flop, the printer will not print.

9. The Summing Amplifier (19X1952)

The block diagram of the summing amplifier is shown in Fig. 4. The function of the summing amplifier is to amplify the dc voltages from the DACs and present this information to the null detector to balance that of the step voltage generator. The amplifiers shown in Fig. 4 are Zeltex M141 chopper stabilized amplifiers. The noise out of the summing amplifier is about 2 mv peak to peak. The dc drift of the amplifier is much smaller than the frequency drift in C202 power oscillator. Therefore, it can be neglected and the frequency from the nominal value can be well tracked.

For the following discussion, the reader is asked to refer to Fig. 5 for clearness.

The calibrated dc output of the H. P. digital to analog converters is 99.9 mv for three columns or 99 mv for the first two columns. Therefore, the unit column is 0.1 mv per digit, the tenth column is 1 mv per digit, and the hundredth column is 10 mv per digit. The input B of the summing amplifier is from H. P. 580A digital to analog converter which we select column one and two. These columns correspond to the first two columns in the frequency counter (from right to left). The gain for the input B is 1/10, therefore, the first column corresponds to 0.1 mv per digit, and the second column corresponds to 1 mv per digit. The input C of the summing amplifier comes from H. P. 562A in which columns three, four, and five are selected. These three columns correspond to columns three, four, and five of the frequency counter. The gain for the input

C is 100, so column three corresponds to 10 mv per digit, column four corresponds to 100 mv per digit, column five corresponds to 1 V per digit. For example, if the frequency counter reads 589.032 Mhz, this is corresponding to 8.9032 V. Column six is not controlled. As long as the frequency is within a hundred Mhz (the digit in the sixth column of the frequency counter is not changed), for instance, from 500.000 Mhz to 599.999 Mhz (this is the case when the step voltage generator sweeps between 0 and 9.9999 V) there will be no problem for the balance of the null detector. However, if the sixth column does change, for example, if the frequency range from 560.000 Mhz to 630.000 Mhz is required, the null detector will never find the required frequency range for us. Therefore, in order to have the system more flexible, the sixth column has to be controlled. The input A of the summing amplifier is the key to the problem and will be described in the next section.

10. Digital to Analog Converter Sixth Column Control Unit (15X9873)

There are several ways to deal with the problem of controlling column six. One thing that can be done is to arrange the two digital to analog converts so that one of them controls columns one, two, and three, and the other controls columns four, five, and six. One problem quickly arrives that in column six we are dealing with 10 V per digit. In others words, an amplifier with an output swing of 100 V has to be used. This is impractical. Should column six be chosen so that it were 1 V per digit, column two would be 0.1 mv per digit. Due to the noise which is around 2 mv, column two is then out of control. The accuracy of the frequency repetition to be within 100 Khz is not preserved. (Note that column two corresponds to 10 Khz per digit).

A relatively simple way is to add or subtract 10 V at a suitable time while we still transfer five columns of digital information into analog voltage. Under this condition, column two corresponds to 1 mv per digit so the accuracy of 100 Khz for the frequency repetition is preserved, and the use of an amplifier with 100 V swing is avoided. What we need is an amplifier with a 20 V output swing so that we can let the column six change one digit without affecting the system operation as pointed out before.

The block diagram of the unit that is of interest is shown in Fig. 6.

The inputs to the DAC sixth column control unit are from the fifth column board of the digital to analog converter (from 562A). After reset, the output of the unit is -10 V and is added to the negative input of the summing amplifier (note that the step voltage is going downward and then upward, so 10 V is added initially). Therefore, for the frequency, say, 630.580 Mhz, this will correspond to 13.058 V.

As soon as the fifth column of the frequency counter changes from 0 to 9, the AND gate 2 is executed so the flip-flop changes state and the -10 V are taken away. On the other hand when the fifth column changes from 9 to 0, the output of the AND gate 1 flips the flip-flop back to the original state and -10 V are added again. Therefore, we can sweep the frequency, for example, from 630.000 Mhz to 580.000 Mhz. Of course this unit is awkward if column six has changed two digits. Fortunately, this is unlikely to happen since the swing of frequency never goes over one hundred Mhz.

11. Data Protector

The nominal useful life of the power tube in the C202 oscillator is around 500 hrs for continuous use. When the tube is getting old, the oscillator is likely to be overloaded. If this happens in the middle of the experiment,

the data in the analyzer will be completely destroyed. The power tube is usually replaced every three weeks. However, in order to protect the data in case the oscillator fails in the middle of the experiment, a data protector is developed such that it will stop the TIBO (which is the control unit in the system) remotely.

By observing the schematic diagram of the oscillator, it was found that one side of its power meter is grounded. This means that a dc voltage exists at the other side of the meter. When the oscillator is overloeaded, the power is then gone and that dc voltage is therefore vanished. The presence or absence of the dc voltage is used to control a logic circuit which in turn allows or stops the TIBO. The circuit of the data protector is shown in Fig. 7.

If there is no input, Q1 is off and Q2 is on. The relay is energized and the TIBO is stopped remotely (TIBO is stopped if its "remote stop" has a 4 V input). In case there is a dc input, Q1 is on and Q2 is off. So the relay is not energized and the TIBO is allowed to go. In other words, as long as the power osciallator does not fail, the TIBO is allowed to process the operation of the system. Otherwise, the TIBO is called to stop and the data in the analyzer is preserved.

CONCLUSION

The operation of the system is quite satisfactory. The accuracy of the frequency repetition is well within 100 Khz. Table 1 shows the typical frequency sweeping in the experiment. Each frequency was set to be five minutes. Therefore, it took about 30 hrs to get these data. The numbers shown in the Table 1 were the frequencies printed by the H. P. 562A printer. The number of 616788, for example, represents a frequency of 616.788 Mhz.

Table 1

616788	616813	616811
615671	615738	615720
614622	614671	614653
613533	613569	613551
612519	612550	612552
611409	611443	611430
610363	610402	610391
609368	609403	609382
608282	608323	608322
607141	607181	607169
606081	606129	606120
604913	605020	605020
603902	604021	604029
602813	602833	602843
601781	601800	601792
600721	600761	600741
599401	599401	599403
598308	598310	598343
597222	597212	597229
596123	596133	596131
595080	595112	595113
593912	593938	593941
592859	592863	592852
591781	591783	591772
590683	590690	590712
589680	589702	589701
588620	588622	588650
587453	587463	587518
586470	586471	586473
585381	585383	585383
584313	584322	584333
583203	583248	583220
584328	585310	584339
585383	585383	585383
586462	586472	586468
587489	587480	587493
588592	588628	588629
589681	589680	589691
590691	590683	590689
591773	591779	591761
592851	592861	592853
593928	593930	593911
595091	595098	595082
596140	596129	596100
597239	597223	597211
598342	598329	598311
599420	599409	599399
600719	600683	600638

Table 1 (continued)

601790	601781	601728
602842	602829	602798
603932	603918	603849
604940	604931	604861
606129	606111	605949
607181	607161	607109
608331	608313	608252
609418	609393	609339
610393	610389	610338
611450	611432	611398
612570	612542	612481
613572	613552	613523
614672	614661	614612
615741	615720	615660
616760	616780	616742
615660	615678	615641
614608	614622	614582
613491	613523	613480
612483	612510	612470
611392	611408	611381
610341	610360	610329
609340	609359	609331
608253	608282	608253
607123	607140	607122
606063	606081	606058
604879	604912	604878
603873	603891	603871
602809	602809	602833
601741	601760	601790
600711	600710	600691
599391	599410	599392
698291	598319	598303
597190	597208	597212
596131	596092	596131
595073	595082	595082
593910	593890	593903
592833	592813	592840
591750	591738	591769
590671	590650	590679
589652	589652	589680
588593	588572	588630
587459	587440	587493
586450	586420	586480
585353	585342	585398
584288	584282	584339
583210	583180	583238
584292	584272	584338
585341	585353	585391
586422	586431	586489

Table 1 (continued)

587449	587450	587508
588563	588593	588582
589613	589632	589682
590642	590642	590713
591728	591723	591791
592830	592818	592862
593889	593883	593931
595040	595071	595129
596118	596073	596131
597181	597163	597229
598293	598281	598330
599390	599379	599413
600641	600623	600713
601730	601713	601791
602818	602780	602842
603862	603842	603923
604879	604843	604943
605970	605939	606123
607121	607083	607172
608270	608229	608328
609350	609312	609412
610353	610311	610391
611381	611372	611452
612513	612460	612553
613512	613470	613579
614620	614582	614669
615672	615648	615729

ACKNOWLEDGEMENTS

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APPENDIX

1. Procedures to set up the system

   1. Connect the analyzer as shown in Fig. 8.
   2. Connect the automatic control system according to Fig. 1.
   3. For the digital to analog converters, set the column selector on columns one and two in H. P. 580A and on columns three, four, and five in H. P. 562A.
   4. Adjust the power level of the power oscillator.
   5. Select the number of steps required by flipping the switches on the front panel of the step voltage generator. The overflow toggle switch should be in X1 position.
   6. Stop TIBO, reset the system by pushing the reset button on TIBO, on the step voltage generator and on the digital to analog sixth column control unit.
   7. Adjust the dc level pot on the front panel of the step voltage generator. By doing so, the required initial frequency can be adjusted. The initial frequency has to be started from the higher side of the frequency interval.
   8. Adjust the amplitude control pot on the front panel of the step voltage generator. This will control the frequency step in the experiment. (The amplitude control can also change the dc level, therefore, procedures 7 and 8 should be adjusted hand in hand).
   9. Adjust the TIBO front panel time base switches in order to set the desired $\Delta T1$ and $\Delta T2$ time bases. Usually $\Delta T1$ is set to be five minutes and $\Delta T2$ is set to be 15 sec.
   10. On the TIBO, the detector switch for the $\Delta T1$ time base is "yes" and for the $\Delta T2$ time base is "no".

11. Start the system operation by pushing the start button on TIBO.

12. The system operation can be stopped by pushing the stop button on the TIBO or by flipping its "stop at the end of the sweep" switch. By doing so the system will be stopped at the end of one sweep.

LIST OF FIGURE CAPTIONS

Figure

1. The system block diagram
2. The block diagram of the step voltage generator
3. The block diagram and the timing sequences of the H. P. printer gate.
4. The summing amplifier
5. Partial system block diagram.
6. DAC sixth column control unit.
7. Data protector.
8. The analyzer connection diagram in the system.

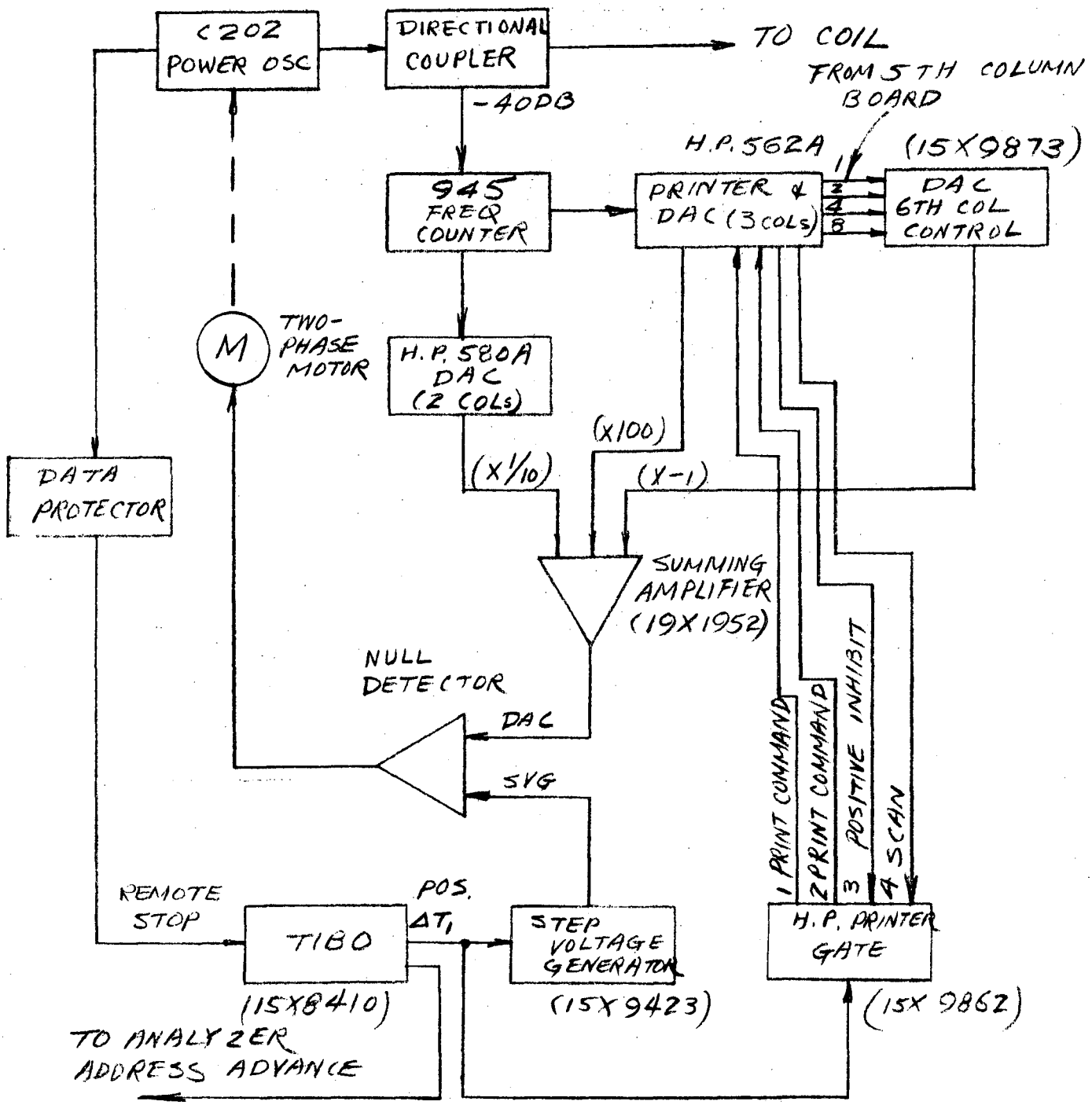


FIGURE 1 THE SYSTEM BLOCK DIAGRAM

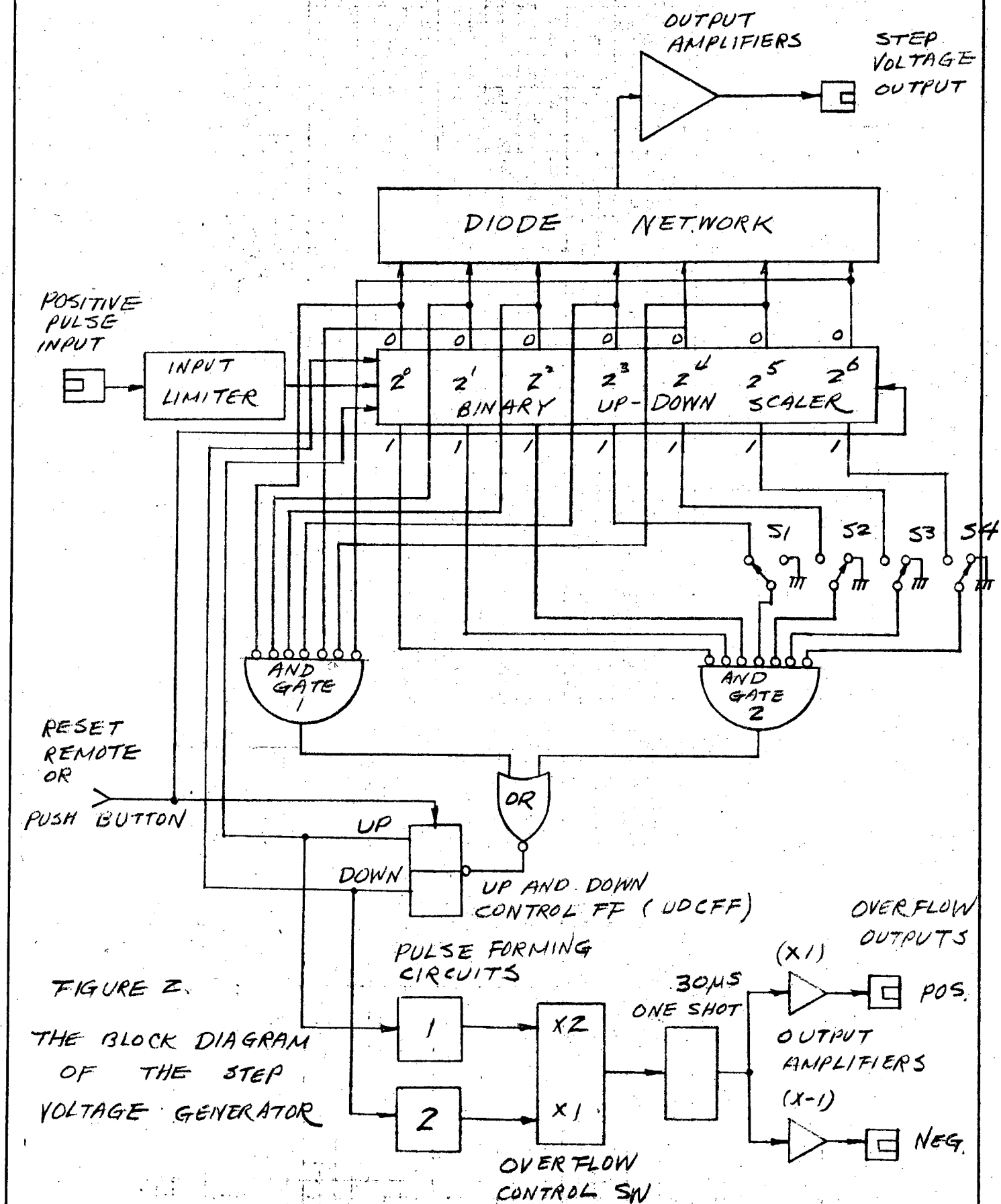
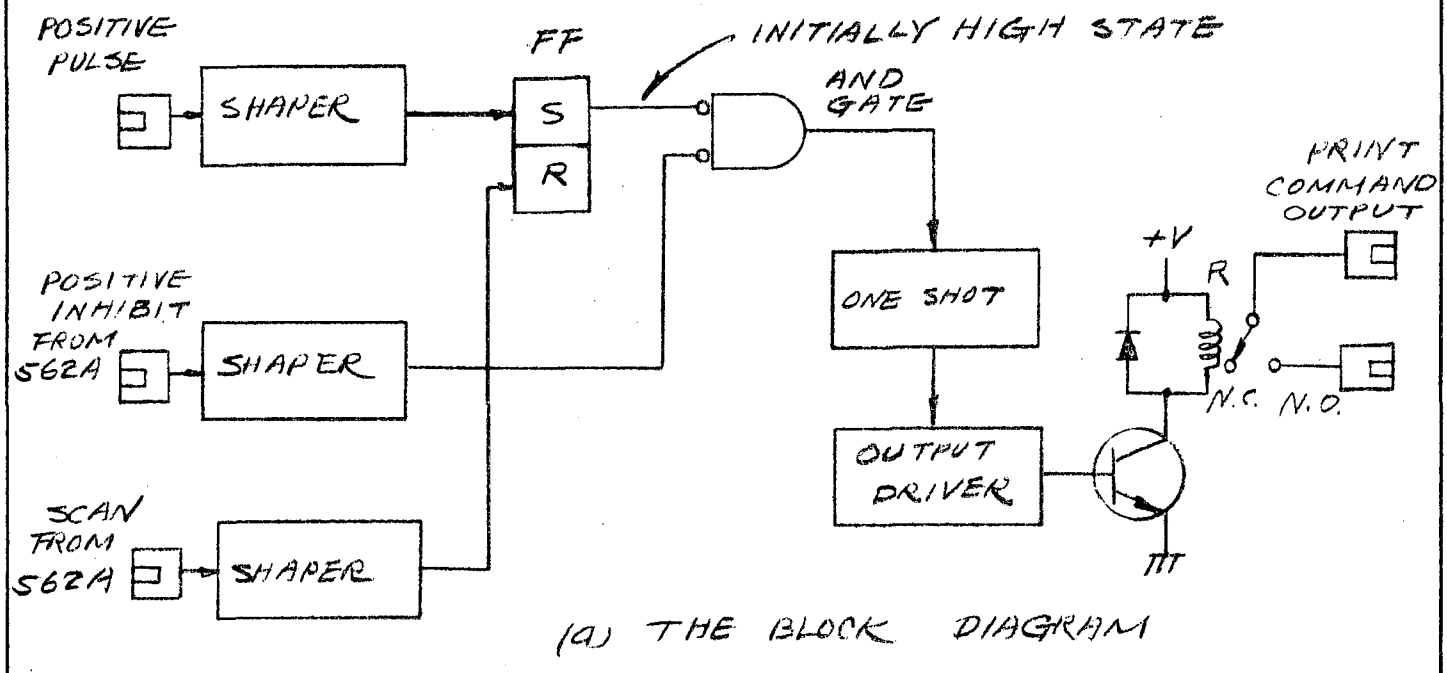
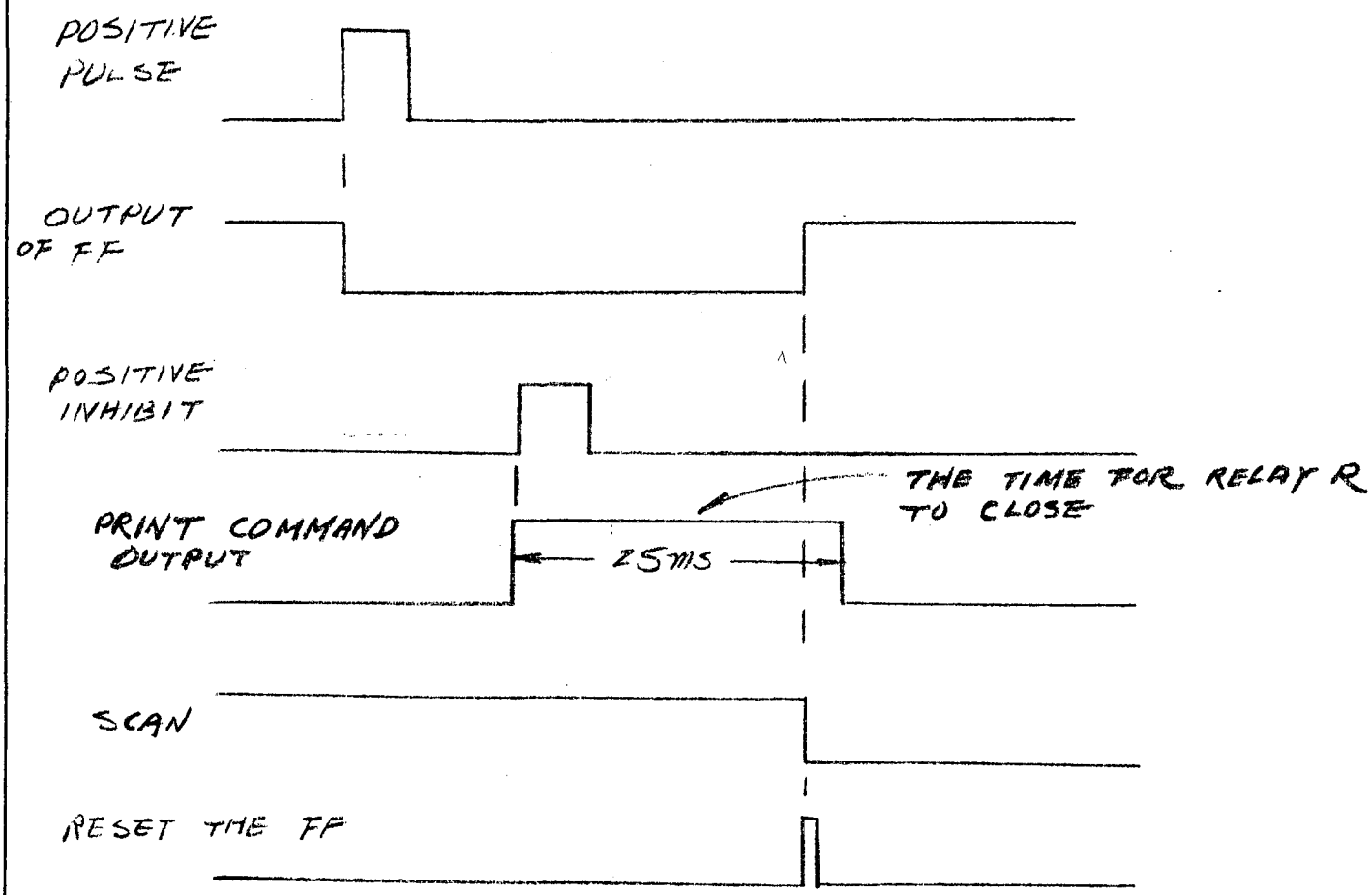


FIGURE 2.

THE BLOCK DIAGRAM OF THE STEP VOLTAGE GENERATOR



(a) THE BLOCK DIAGRAM



(b) THE TIMING SEQUENCES

FIGURE 3. THE BLOCK DIAGRAM AND THE TIMING SEQUENCES OF THE H.P. PRINTER GATE

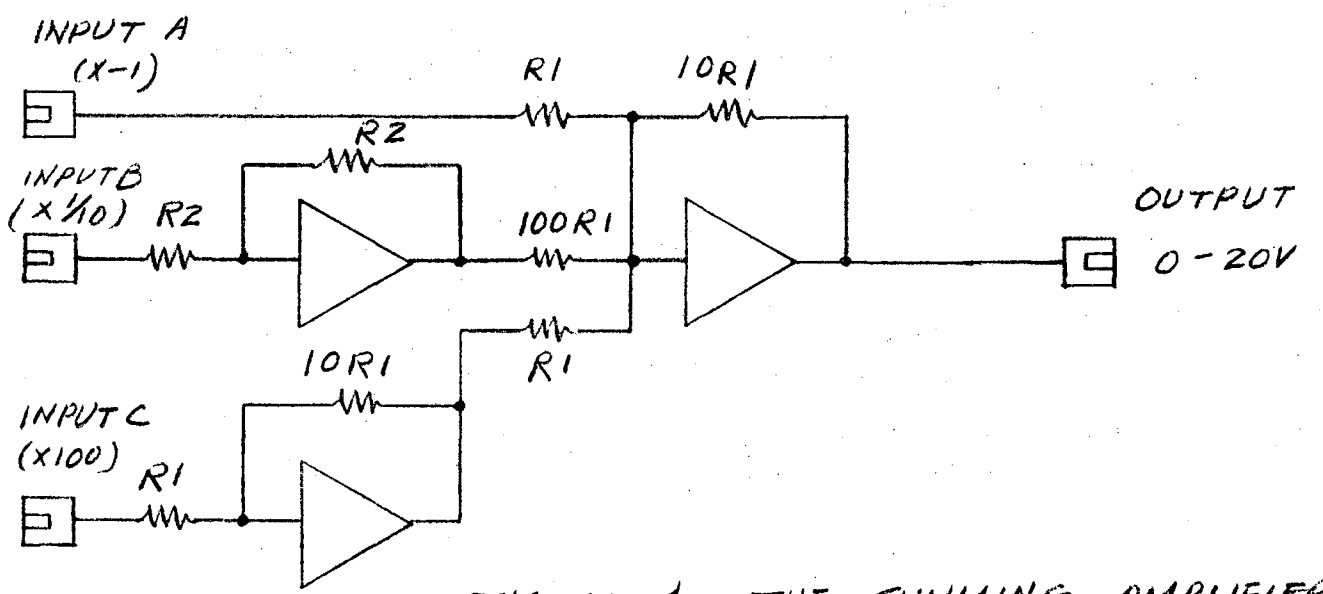


FIGURE 4 THE SUMMING AMPLIFIER

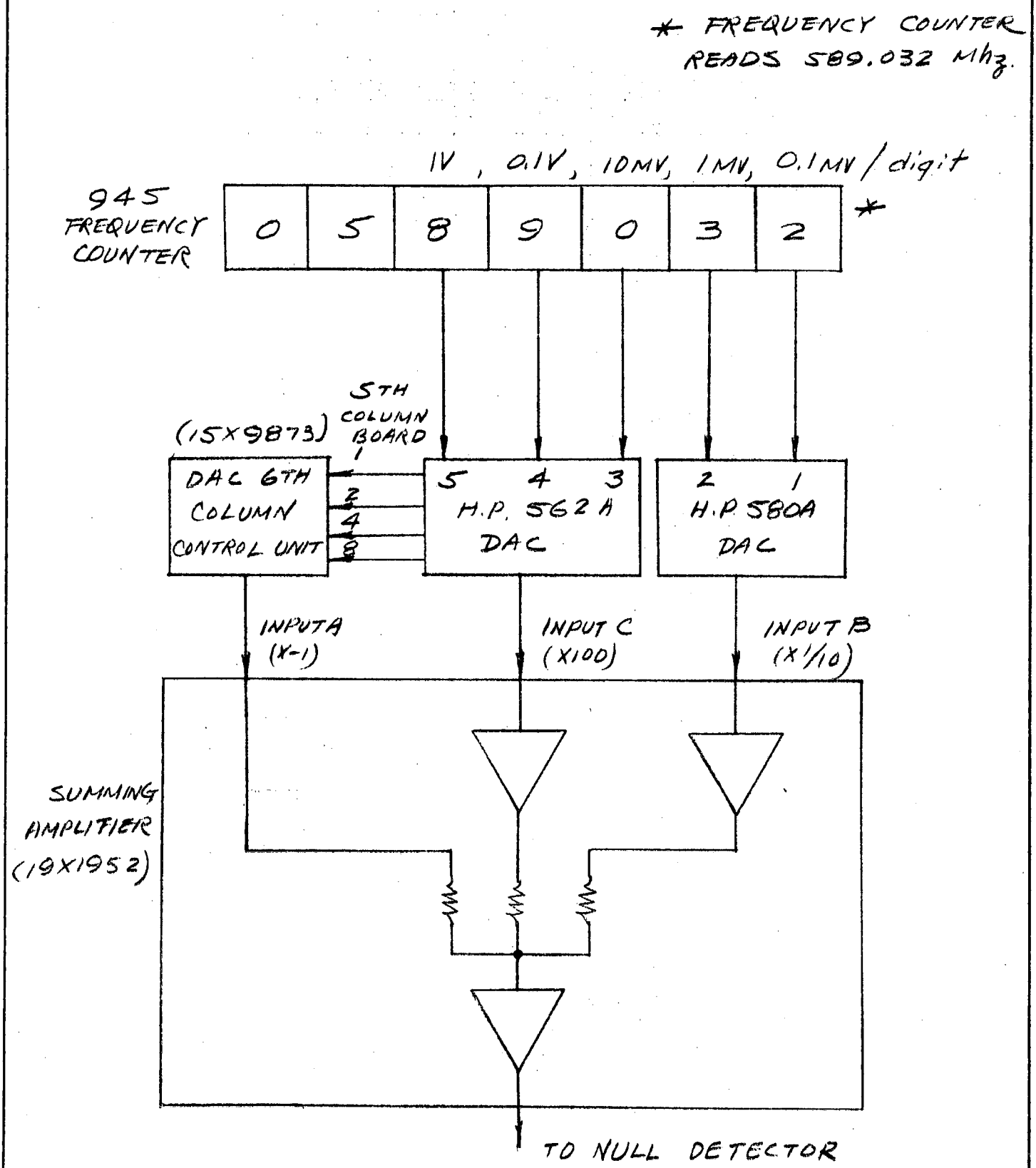


FIGURE 5 PARTIAL SYSTEM BLOCK DIAGRAM

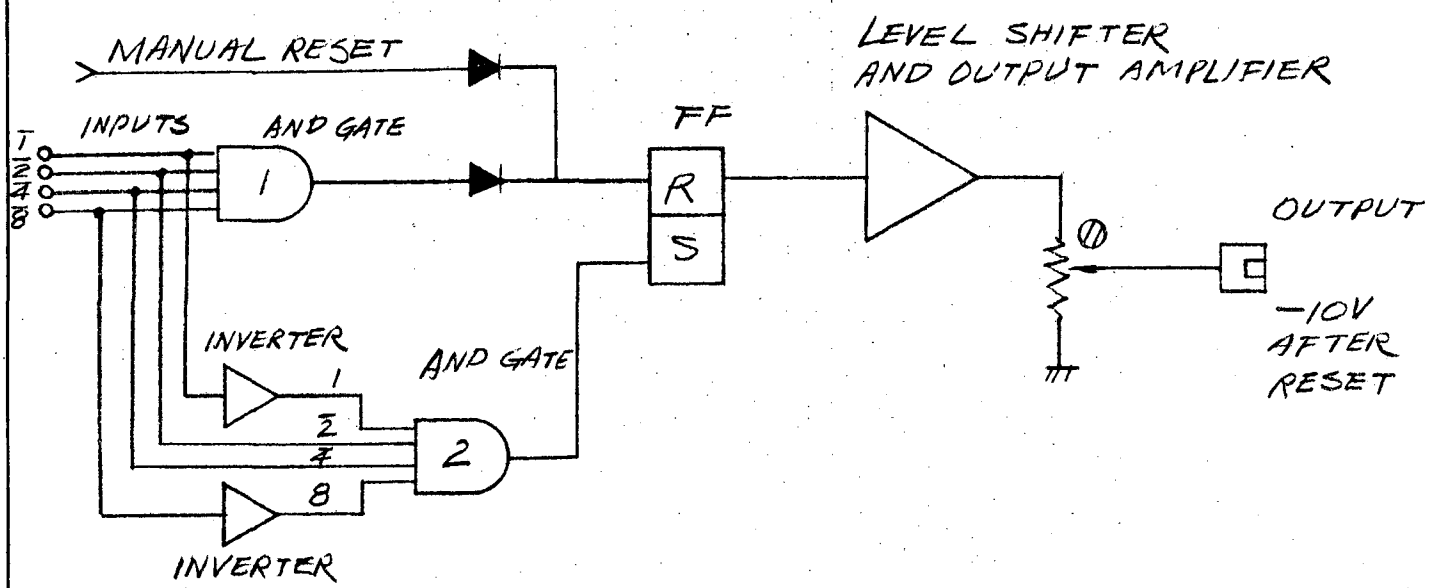


FIGURE 6. DAC 6TH COLUMN CONTROL UNIT

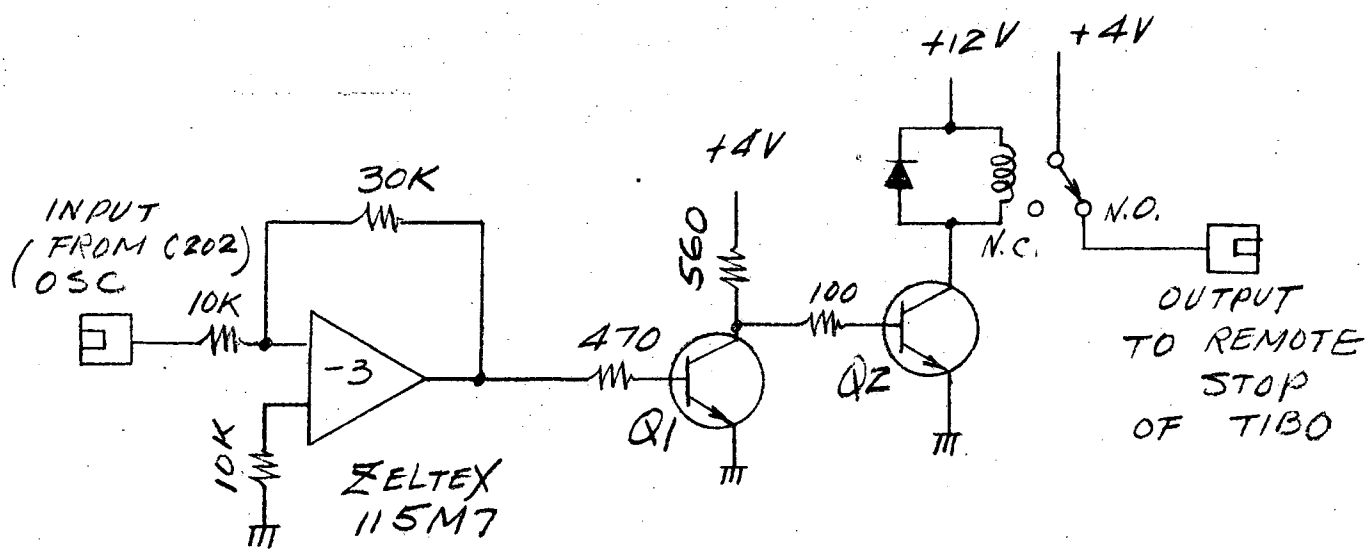


FIGURE 7. DATA PROTECTOR

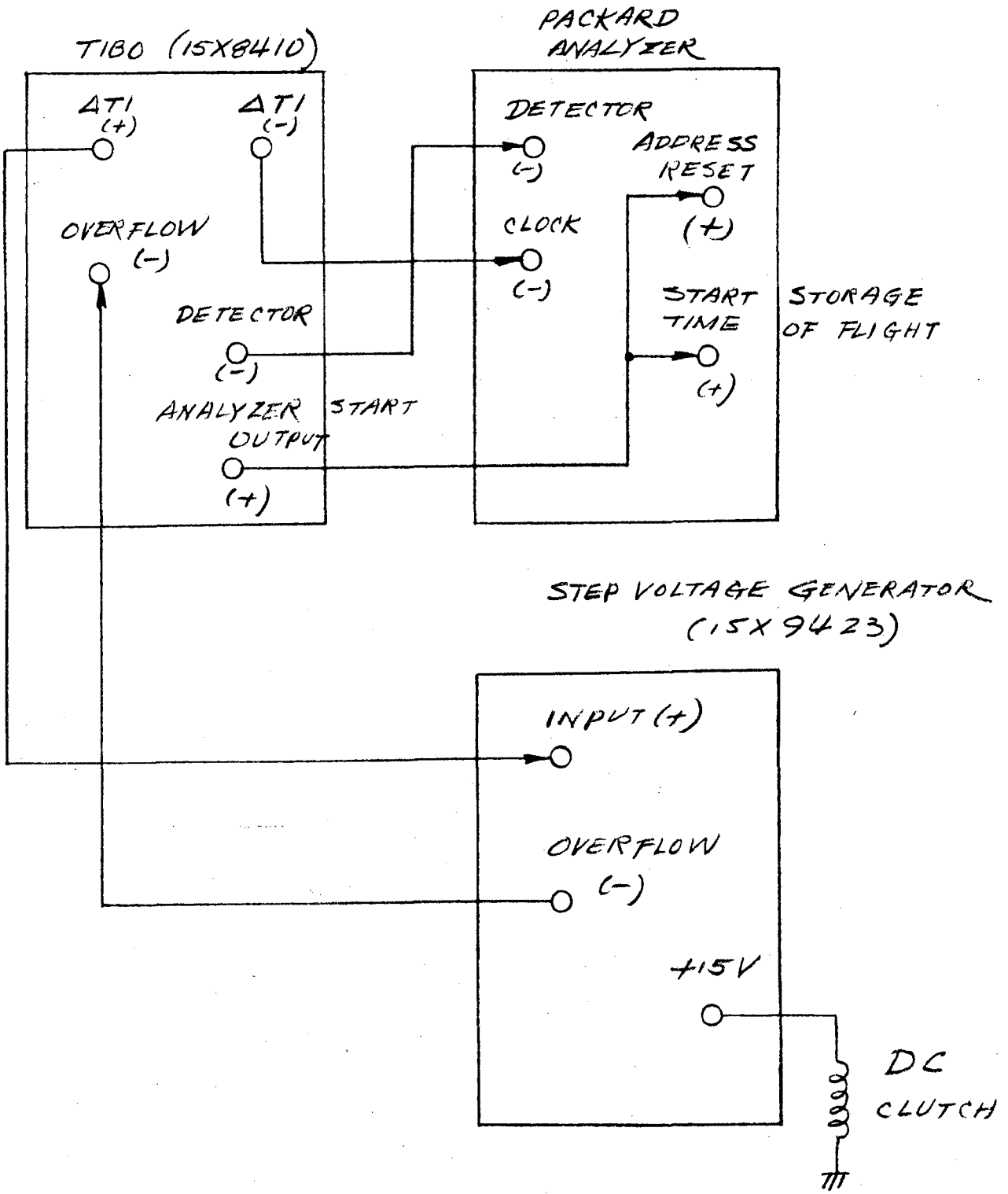


FIGURE 8 THE ANALYZER CONNECTION DIAGRAM IN THE SYSTEM.

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