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PUZZLE: A PROGRAM FOR COMPUTER-AIDED DESIGN OF PRINTED-CIRCUIT ARTWORK

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Abstract

A program developed to aid in the solution of the topological problems encountered in printed-circuit artwork design is described. It is emphasized that the program is intended as a tool for use by the designer to reduce the human effort required to produce both the topological solution and the graphic output needed for the manufacture of etched printed circuit boards. A method of describing the location of individual pads and a library of modular components is discussed. The program is intended to have maximum use in the area of two-sided printed-circuit boards for integrated circuits. It is also possible to design discrete component circuits with the existing version of the program.

PUZZLE: A PROGRAM FOR COMPUTER-AIDED DESIGN OF PRINTED CIRCUIT ARTWORK, Ronald Zane and Deanna A. Wilber, Lawrence Radiation Laboratory, University of California, Berkeley, California

PUZZLE is a program developed, at the Lawrence Radiation Laboratory in Berkeley, to serve as a design aid in the production of printed circuits. The emphasis has been on the reduction of costs and on decreasing the time required to convert a designer's sketch of a circuit into an operational circuit.

In view of the wide variety of criteria that may affect the placement of components and the routing of connections, it was decided to leave as much design control as possible in the hands of the designer. For this reason component placement, as determined by the input data, is fixed and may not be modified by the program. The input data coding is also arranged in such a manner that the method in which the data is presented to the computer influences the routing attempted by the computer. In earlier versions of PUZZLE the power and ground bus patterns were fixed and always appeared in the same locations. The fixed power and ground buses have been abandoned in favor of routings which are determined in the same manner as any other interconnections.

PUZZLE, at present, is capable of handling boards up to 5 by 10 in. in area. The field is considered to be an array of points on the intersections of grid lines with 0.1-in. centers horizontally and vertically. All components are placed on the 0.1-in. grid, and all interconnections are rectilinearly routed along the intersections of the grid. The field is further subdivided into a grid of 1-in. squares to aid in the placement of components. The squares are numbered with the identification numbers 01 through 50, with square 01 in the lower left-hand corner, 10 in the lower right corner, 41 in the upper left corner, and 50 in the upper right corner. A "library" of defined component codes greatly reduces the effort required to write a wiring table (Fig. 1). Each node is defined by a seven-digit code of the form Ommnnpp. The first digit is always zero. The two digits mm are determined from the library of component codes. The two digits nn define the square in which the component is placed. The digits pp identify the "pin" number on the component. When the code for a modular component is specified, the program always inserts the other pads needed for the module even if no connections are specified to some of the pins. Interconnected points are listed in a sequence of seven-digit codes on a single card. As many as eleven interconnected points may be listed on a card.

After the data cards containing the wiring list have been read into the computer, the program begins the task of solving the topological problem of finding interconnection paths between the points specified. All paths are required to stay on the 0.1-in. grid lines. In general vertical lines are predominantly on the component side of the board and horizontal lines are on the wiring side. In the present version all connections are made rectilinearly. An improved version of the program will permit lines to be produced on the 45° diagonals through the grid intersections.

The operational procedure of PUZZLE may be divided into three major portions: the initialization process, the actual routing of connections, and the production of the graphic output (see Fig. 2).

The first step in the initialization process is the acceptance of data. This includes reading the input, testing it for compliance with input specifications

and storing the connections to be made as data pairs. Next the input data is scanned in order to establish the horizontal and vertical limits to be used in the connection mapping. Thirdly the graphic output is begun: the label is written, the grid is established, and the necessary pads are drawn. The last portion of the initialization process sequences the data in such a way that the shortest paths will be drawn first.

Once the data has been sequenced, PUZZLE routes the connections. A stepping procedure is used to do the mapping. In general the path moves in the direction of the end point, that is, if the second terminal is to the left and above the first, the stepping procedure takes the path upward as far as possible and then moves to the left, changing again to the vertical when it is blocked, and so on. Frequently modifications of this procedure are used for particular areas, but the basic procedure is used whenever possible. In addition a "smoothing" process has been incorporated. After several steps have been completed tests are made to see if every direction change really was necessary. When the path is completed a message is printed and the path is recorded.

The last portion of the routing is a clean-up to make extra tries to complete the difficult paths. Any possible connection that would complete the circuit is tried.

The third major portion of PUZZLE is the production of the graphic out-put. The composite picture is drawn first. Then if the board is complete--i.e., there was no rejected data and no missing connections--two additional graphs are drawn, one for each side of the board.

When a data set has been completely processed, the next data card is checked. If it is blank PUZZLE processing is completed; if, however, it is a label card (the first card for each data set), control is returned to the beginning of the program, where the new data may be read.

After a successful plot of the interconnections has been obtained, the wiring side plot and component side plot are overlaid on a board outline which has been produced by conventional drafting techniques or plotted by another program called BLOP. Any necessary retouching is done at this point, as well as the addition of any paths not previously included. High-contrast negatives are produced by contact printing of the plots in an Ozalid machine using Dupont "Crolux" photopolymer.

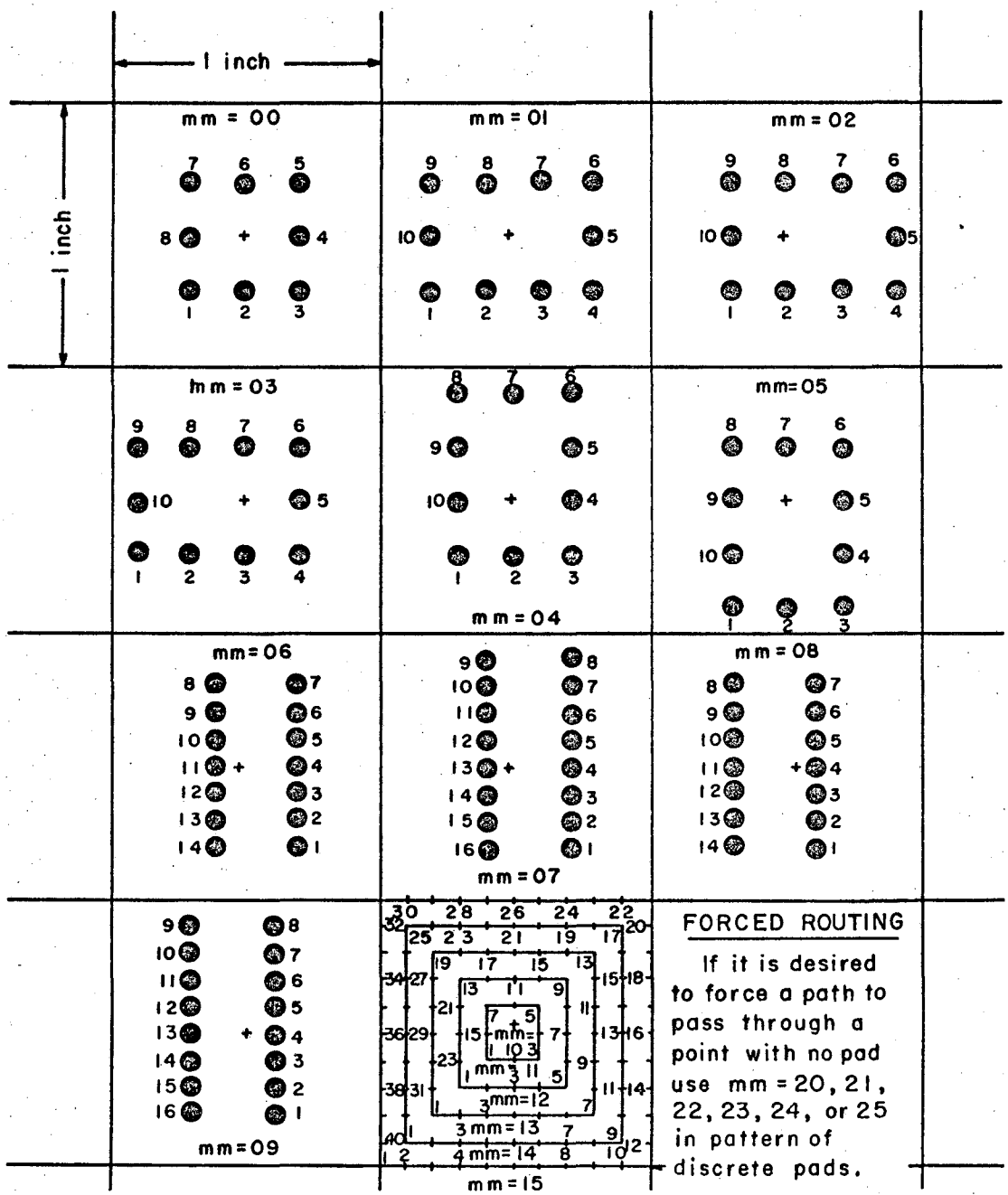

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Fig. 1

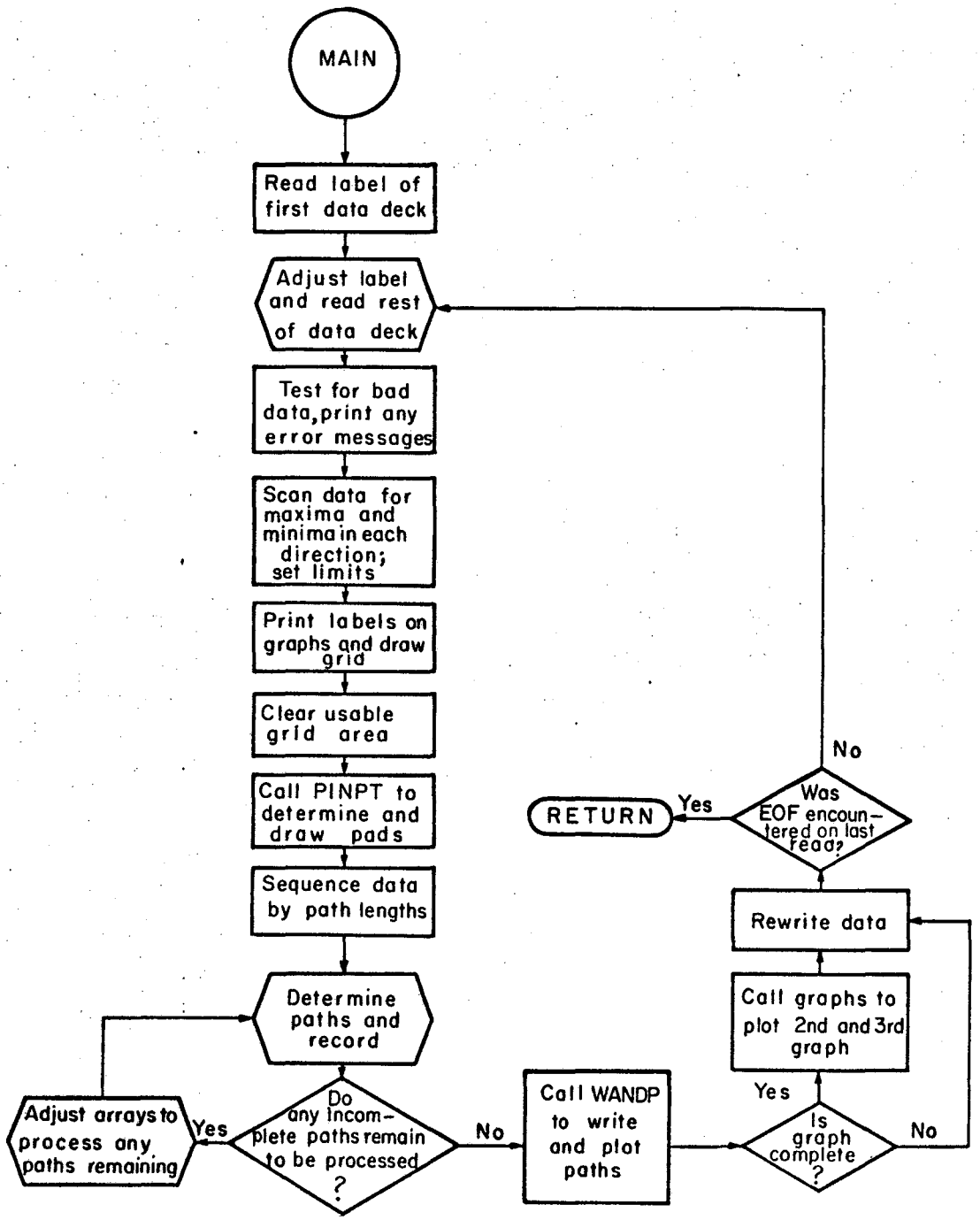

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Fig. 2

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