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A COMPREHENSIVE STUDY OF CIRCUS

Edward K. Chen

Master's Thesis

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A COMPREHENSIVE STUDY OF CIRCUS

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September 1969

ABSTRACT

CIRCUS is a computer program for the time-response analysis of electronic circuits. It is most suitable for analyzing circuits where nonlinearities are essential for proper operation. This report presents a self-contained study of CIRCUS. Models for all the present-day junction devices are studied in detail. Techniques to measure the model parameters are presented together with representative measurements. Comparison between the computer-predicted and experimental results of various digital circuits are shown. A description of how to use CIRCUS is also included.

CHAPTER 1. INTRODUCTION

With electronic circuits becoming more and more sophisticated and complex, a complete mathematical analysis by hand is impossible. At best a first-order analysis with crude approximations can be carried through. Experimentation and experience become vital in any design.

Since the advent of computer-aided design programs, the time-consuming and tedious task of solving complicated equations and experimentation is partially eliminated. Furthermore, a much more accurate model can be used to represent the devices. Side effects, which were not obvious in first-order analysis, will show up in the computer simulation. Parameter vairation effects can be compensated, optimum design is achievable, and extreme cases which are destructive to the circuit can be simulated and studied without actually destroying the circuit.

Among the various nonlinear computer-aided design programs, CIRCUS is one of the most general and versatile. It is the fourth generation of Branin's TAP[1)] and the direct descendent of Malmberg et al.'s NET-1 [2)]. Because of its generality and complexity, a detailed study is desirable.

The purpose of this report is to present a self-contained study of CIRCUS. First the models for bipolar transistors, junction field-effect transistors, switching diodes, zener diodes, tunnel diodes, and four-region devices are studied in detail. Techniques to measure the

model parameters are presented together with examplary measurements (for 2N709 and 2N2369A). Comparison between the computer predicted and the experimental results of various digital circuits are shown. A description of how to use CIRCUS is also included.

CHAPTER 2. GENERAL DESCRIPTION OF CIRCUS

In general, any time-domain circuit analysis program which is capable of handling nonlinear effects has to resolve three major problems:

(a) Suitable models, preferably nonlinear and applicable under all operating conditions, representing the large signal behavior of the devices must be found.

(b) The circuit analysis technique used should be simple and, for ease of computation, numerically oriented towards computer solution.

(c) Numerical technique should be sophisticated so that no excessive computer time is required.

For (a), CIRCUS has built-in nonlinear models for almost all present-day junction devices except the unijunction transistor (UJT), though suitable combinations of transistors and resistors can be made to model the UJT. Detailed discussions of these models will be presented later in this report.

For (b), CIRCUS adopts the state space approach [3,4]. This approach is no different from the traditional nodal or loop approaches except that it takes full advantage of the computer's capability and is most suitable for the solution of nonlinear differential equations.

The program first converts the junction devices into their equivalent circuit models with conventional R, L, C and voltage or current generators. Then the topology of the circuit is translated into the incidence matrix of zeros and ones, with a "1" representing a branch connecting two nodes, and a "0" if there is no branch connecting the two nodes. After this,

a normal tree *) is picked to insure the equations obtained later are all linearly independent. From the normal tree and the incidence matrix, n first-order differential equations can be written in the normal form:

$$[\dot{X}] = [Z]\,[X] + [S]\,[U] + [\hat{S}]\,[\dot{U}] - [I], \qquad (2\text{-}1)$$

where [X] is the independent branch currents and node voltages vector; these are the state variables,

[Z] is the matrix representing all the R, L, C elements,

[U] is the independent current and voltage sources vector,

[S] is the matrix for the independent voltage and current sources,

$[\hat{S}]$ is the matrix representing the derivative of the independent voltage and current sources,

$\cdot$ implies first derivative.

Since Eq. (2-1) involves only the first derivative, it is relatively easy to solve. There are different numerical integration techniques that can be used, but a common difficulty with most numerical integration techniques is the incompatibility of the circuit time constant with the integration step. This results in excessive computer time because of convergence difficulty. CIRCUS uses Pope's exponential numerical integration method [5], so that even if the integration steps are large the incompatibility problem between circuit time constant and the integration step may not be severe.

Besides the above-mentioned three major advantages, CIRCUS has the following desireable features **):

(a) The input format is so flexible that there are hardly any restrictions.

---

*) A tree is defined as the branches joining all the nodes in the circuit but forms no closed loop. A normal tree is then a tree of the circuit that contains all the independent voltage sources, no independent current sources, a maximum number of C's, and a minimum number of L's.

**) See Appendix A for detail.

(b) Any current, voltage, and power dissipation can be printed and plotted as outputs.

(c) Junction device parameters can be stored on a library tape and be used when called.

(d) Except for the ohmic resistances of the junction devices, all parameters can be varied one at a time or all at once.

CHAPTER 3. THE DEVICE MODELS

In order to simulate electronic circuits on the computer, all circuit elements must be properly described by well-behaved equations. Whereas the conventional elements like generators, resistors, inductors, and capacitors (R, L, C) are all described by either a linear equation or a linear differential equation, the electronic devices cannot be described by a simple equation compatible with those of R, L, C. These devices must be represented by a model.

An ideal device model should account for all the physical phenomena in terms of concepts that electrical engineers understand, via resistors, capacitors, generators, etc. In addition it should be powerful enough so that the model holds true under all operating conditions. Such an ideal model is too complicated, if not impossible. But any good model should follow the same reasoning.

The hybrid-π model is an example of a good transistor model [6]. That this is a linear model necessitates breaking it into several separate models under different operating conditions (normal, inverse, cut-off, and saturation operations) [7]. The transistor T model avoids this problem by incorporating nonlinearities as well as the charge-control concept in the model [8,9]. Using this model as the central idea, other models for p-n junction devices can be obtained with appropriate modifications.

The prime objective of this chapter is to describe the basic principles, assumptions, and limitations of the models so that CIRCUS users can avoid erroneous results or excessive computer time because of lack of understanding of the models.

A simple Ebers and Moll transistor model [10] is first described from reasonable assumptions. Some of these assumptions are then removed when additional circuit elements are added to complete the T model. Models appropriate for diodes, tunnel diodes, zener diodes, junction field-effect transistors, and four-layer devices are derived as a consequence of the transistor T model.

A. THE BIPOLAR TRANSISTOR "T" MODEL [10]

In order to make the mathematics simpler, it is convenient to make the following assumptions:

(i) The ohmic voltage drops in the base, emitter, and collector regions are neglected.

(ii) The effect of terminal currents on the stored charge in the base as well as in the depletion layers is ignored.

(iii) The transistor is operating under low-level injection *.

(iv) Recombination in the base is negligible.

(v) The transistor is assumed to be homogeneous.

From these assumptions and two more basic physical laws [11],

$$c' = c_o (e^{\Theta V} - 1), \tag{3-1}$$

the 'law of the junction,' and the continuity equation

$$D\nabla^2 c' = \frac{\partial c'}{\partial_t} + \frac{c'}{T_{BN}} - G, \tag{3-2}$$

where c' = excess minority carrier concentration at the edge of the p-n junction. It can either be hole concentration or electron concentration,

c_o = minority carrier concentration at thermal equilibrium. It can either be hole or electron concentration,

---

* Low level injection implies that the injected carriers are small compared to the majority carriers.

V = voltage across the junction,

$\Theta = \frac{q}{MKT}$ with M as the factor to account for the depletion layer and surface recombinations,

T_{BN} = average life time for the carriers,

G = hole-electron pair generation rate,

∇ = gradient.

Ebers and Moll have shown that the low-frequency, steady-state behavior of PNP bipolar transistor can be described in terms of terminal currents and voltages.

$$I_E = \frac{I_{ES}(1 + \beta_N)}{\beta_N}\left(e^{\Theta_N V_{eb}} - 1\right) - I_{CS}\left(e^{\Theta_I V_{cb}} - 1\right), \tag{3-3}$$

$$I_C = -I_{ES}\left(e^{\Theta_N V_{eb}} - 1\right) + \frac{I_{CS}(1 + \beta_I)}{\beta_I}\left(e^{\Theta_I V_{cb}} - 1\right)^{*}, \tag{3-4}$$

$$I_B = -I_E - I_C, \tag{3-5}$$

where

subscript N means normal operation of the transistor,

subscript I means inverse operation of the transistor.

---

* In order to be consistent with CIRCUS notation, these two equations are slightly different from the conventional Ebers and Moll equations:

$$I_E = a_{11}\left(e^{qV_{eb}/KT} - 1\right) + a_{21}\left(e^{qV_{cb}/KT} - 1\right),$$

$$I_C = a_{21}\left(e^{qV_{eb}/KT} - 1\right) + a_{22}\left(e^{qV_{cb}/KT} - 1\right).$$

Also, Ebers and Moll equations ignore surface- and depletion-layer recombination.

Schematically Eq. (3-3) and Eq. (3-4) can be represented as in Fig. 3-1,

where $$I_{EO} = \frac{I_{ES}(\beta_N + \beta_I + 1)}{\beta_N (\beta_I + 1)},$$

$$I_{CO} = \frac{I_{CS}(\beta_N + \beta_I + 1)}{\beta_I (\beta_N + 1)}.$$

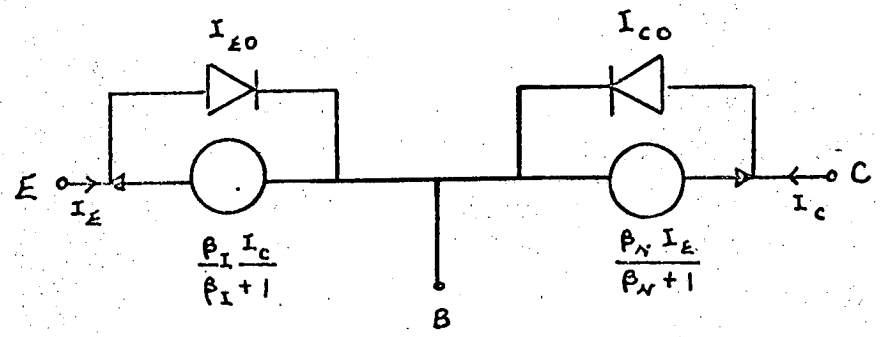


FIG. 3-1. Model of PNP Transistor.*

The model shown in Fig. 3-1 is good only at low frequencies. At higher frequencies, junction and diffusion capacitances must be included:

a. Junction Capacitance

Junction capacitance arises because of the difference in doping between the p and the n region. With this difference, a concentration gradient results on each side of the junction, giving rise to a tendency for holes to diffuse towards the n side and electrons to the p side. As the holes and electrons become thermally ionized from the doped atoms, they diffuse towards each other and leave behind the immobile charges, forming a depletion layer. This depletion layer acts very much as a capacitor because on one side there are positive immobile charges and on the other side there are negative charges. Upon application of reverse bias, more dopants are ionized and mobile charges

*Similar model for NPN Transistor but with current generators' directions reversed.

drift away from the junction, resembling very much the movement of charges when a voltage is impressed upon a capacitor.

Norwood and Shatz[12] have shown that in general, if the net dopants of the transistor follow a power law in the depletion regions (see Fig. 3-2),

$$N_D - N_A = BX^k, \tag{3-6}$$

where

N_D = donor concentration,
N_A = acceptor concentration,
B,k = constants;

then the equation for the junction capacitance can be found easily.

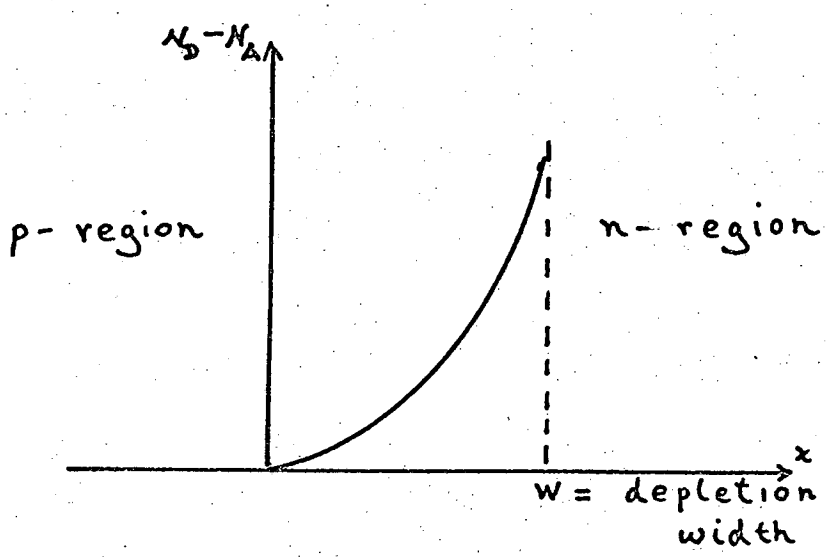


FIG. 3-2. Power Law Concentration in the Depletion Layer.

Using Poisson's law,

$$\frac{d^2\psi}{d_X{}^2} = q\frac{\left(N_D - N_A\right)}{\varepsilon} = -q\frac{BX^k}{\varepsilon}, \tag{3-7}$$

where q = electron charge,

ψ = potential across the depletion layer,

ε = dielectric constant,

and from electrostatics,

$$E = -\frac{d\psi}{d_X}, \tag{3-8}$$

they show that the junction capacitance follows an inverse power law:

$$C_T = \frac{a}{(V + \emptyset)^n}, \tag{3-9}$$

where $n = \frac{1}{k+2}$ = doping gradient, which varies between 0.2 and 2.0,

$$a = \left[\frac{q\ B\ \varepsilon^{(k+1)}}{k + 2}\right]^{\left(\frac{1}{k+2}\right)} = \text{constant},$$

$\emptyset$ = contact potential, which varies between 0.2 and 1.1 V.

Incorporating the two junction capacitors in the model, the new bipolar transistor model becomes:

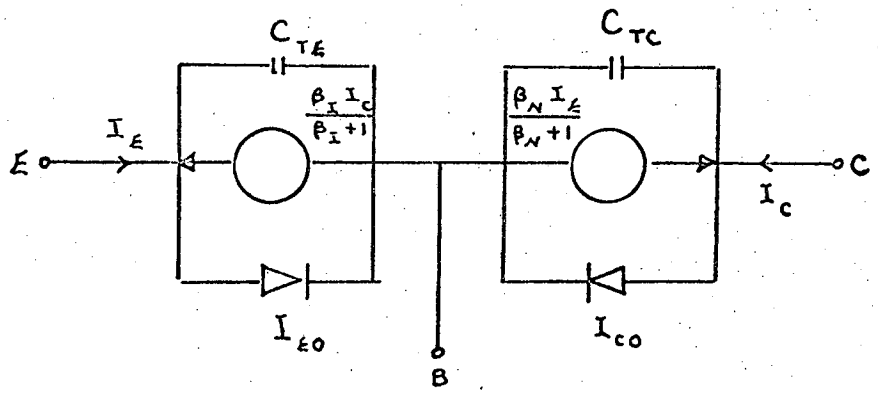


FIG. 3-3. The PNP Transistor Model with Junction Capacitors Included.

b. Diffusion Capacitors

The diffusion capacitance arises because of the charge storage in the collector, and in the emitter base. When the transistor is forward biased, there are charges stored in the base. As the junction voltage V_{BE} (V_{BC} for inverse operation) increases, majority carriers are injected from the emitter (collector for inverse operation). As a consequence, minority carriers are drawn into the base to neutralize the majority carriers. This balancing of charges can obviously be represented by a capacitance,

$$C_D = \frac{d\,Q_{BN}}{d|V_{BE}|} . \qquad (3\text{-}10)$$

If recombination is negligibly small in the base, the minority carrier distribution in the base is as shown in Fig. 3-4.

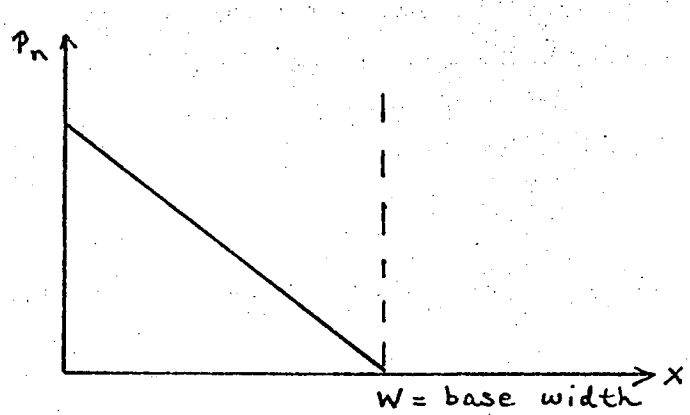


FIG. 3-4. Minority Carrier Distribution in the Base of a Homogeneous PNP Transistor.

Therefore, the net charge stored in the base Q_{BN} becomes the area under the straight line multiplied by the cross-sectional area of the transistor A and the electronic charge, q:

$$Q_{BN} = q\ A\ \frac{P_n W}{2}\ . \tag{3-11}$$

Combining Eq. (3-11) with Eq. (3-10) and remembering the Law of the junction, it is easy to show [6)]

$$C_D = \Theta_N I_{CN} \frac{W^2}{2D_p}\ ^{*}, \tag{3-12}$$

---

* In general it is $C_D = \Theta_N I_{CN} \frac{W^2}{KD_p}$,

where K is the factor to account for the field in the base. It varies between 2 (homogeneous) and 10.

where I_{CN} = normal collector current,

W = base width,

D_p = diffusion constant in the base.

Beaufoy and Sparkes [8,9] have shown that $\frac{W^2}{2D_p}$ is equal to the fundamental time constant of the intrinsic base region of the transistor, T_{CN},

$$T_{CN} = \frac{W^2}{2D_p} . \tag{3-13}$$

The importance of the fundamental time constant lies in the fact that the transistor is a charge-controlled device and the switching speed depends on the amount of charge supplied or removed from the device. Since to a first approximation the stored base charge Q_{BN} is directly related to the fundamental time constant T_{CN},

$$Q_{BN} = T_{CN} I_{CN} , \tag{3-14a}$$

the dominant factor of switching speed is the fundamental time constant. Furthermore, under the charge-controlled assumption Q_{BN} is related to the average minority carrier lifetime T_{BN},

$$Q_{BN} = T_{BN} I_{BN} , \tag{3-14b}$$

where I_{BN} = normal base current.

When the transistor is operating in the saturation region (or inverse operation), the collector base junction is forward biased and is injecting minority carriers into the base. Therefore, a similar T_{CI} can be introduced to model the inverse diffusion current. Of course when a junction is reverse biased, the diffusion capacitor becomes insignificant.

Including the diffusion capacitors in the high-frequency T model is the same as removing the constraint that the terminal currents do not affect the base charge storage. The high-frequency T model is shown in Fig. 3-5.

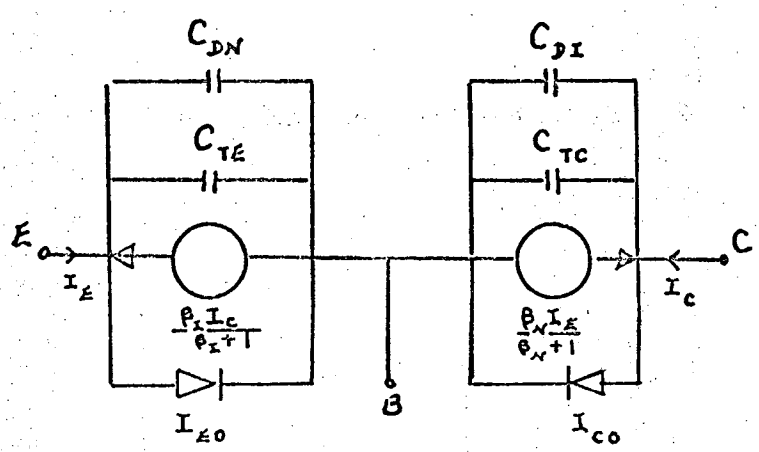


FIG. 3-5. High-Frequency Bipolar Transistor Model.

The constraint that there are no ohmic voltage drops in the three regions can be relaxed if ohmic resistances are added to the model (Fig. 3-6) as resistors.

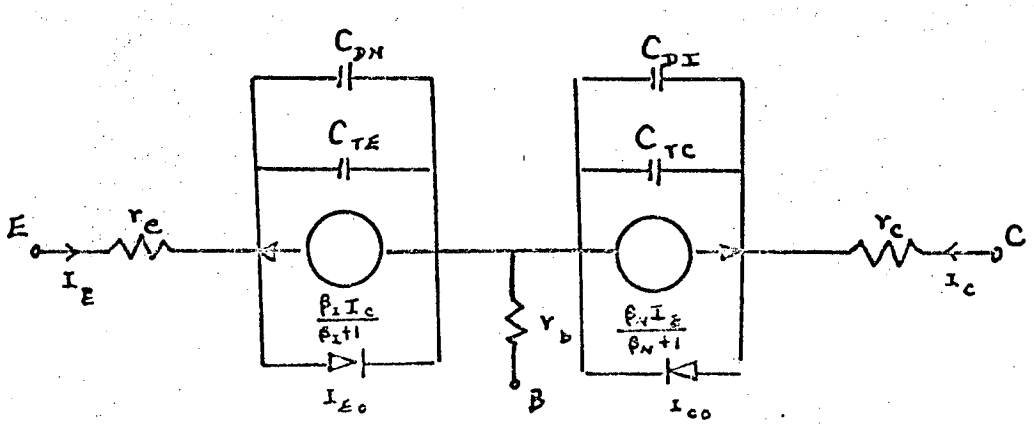


FIG. 3-6. The Bipolar Transistor with Ohmic Resistors Included.

In order to handle radiation effects, two independent photocurrent generators[13] (I_{pp}^*, I_{pp})* are added to Fig. 3-6, giving Fig. 3-7:

$$C_{be} = \frac{a_1}{(\phi_1+V_{be})^{n_1}} + \Theta_N T_{CN} I_{ES} \; e^{\Theta_N V_{be}},$$

$$C_{bc} = \frac{a_2}{(\phi_2+V_{bc})^{n_2}} + \Theta_I T_{CI} I_{CS} \; e^{\Theta_I V_{bc}},$$

$$I_{be} = (1 + \frac{1}{\beta_N}) \; I_{es} \left(e^{\Theta_N V_{be}} - 1\right) - I_{cs} \left(e^{\Theta_I V_{bc}} - 1\right),$$

$$I_{bc} = (1 + \frac{1}{\beta_I}) \; I_{cs} \left(e^{\Theta_I V_{bc}} - 1\right) - I_{es} \left(e^{\Theta_N V_{be}} - 1\right),$$

$$I_{pp}^* = f_1(t),$$

$$I_{pp} = f_2(t).$$

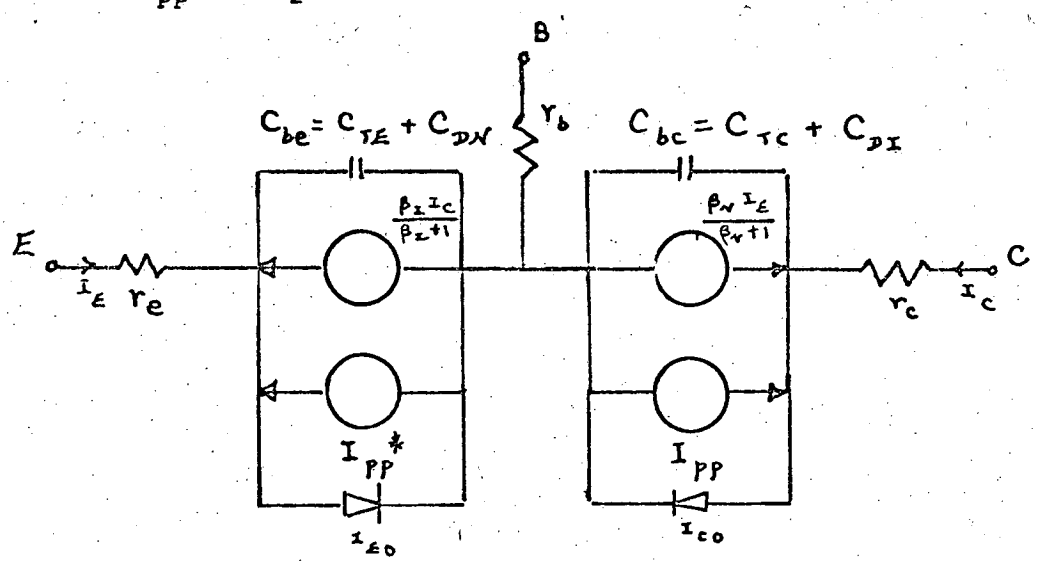


FIG. 3-7. Bipolar PNP Transistor Model used in CIRCUS*.

---

* For NPN, the current generators' directions are reversed.

c. Overall Constraints on the Bipolar Transistor Model

Although the derivation of the bipolar transistor model is based on homogeneous transistors, the model can be applied equally well to drift transistors (see Fig. 3-8 for differences between homogenous and drift transistors).

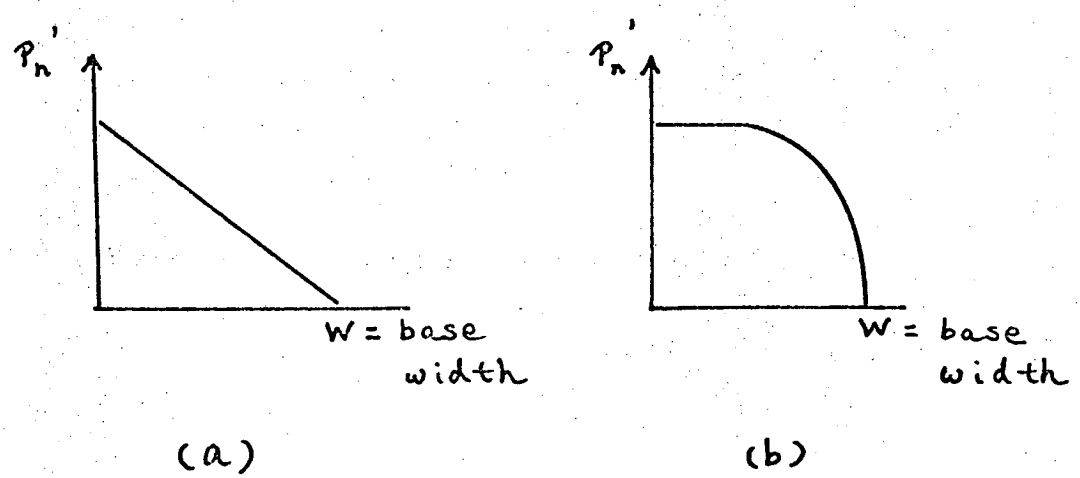


FIG. 3-8. Excess Minority Carrier Concentrations at the base of (a) homogeneous transistor, (b) drift transistor.

However, there are implicit assumptions used during the derivation of the model which should be considered as constraints of the model. These assumptions are:

(i) **Distributive** nature of the base is ignored[14].

In the development of the model, the base is not considered as a distributive structure but is modeled by a lumped element. Under this approach, the base resistance r_b is considered as one distinct lumped resistor which is independent of current level and frequency range. Of course, in reality this is not true. (see Fig. 3-9.)

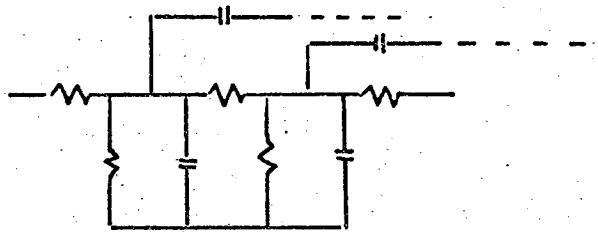


FIG. 3-9. Distributive Base.

Furthermore, because of the lumped assumption, the excess phase effect is not included. For instance, for a step-emitter current input, the charge built up in the base as predicted by the model will be as shown in Fig. 3-10a compared to the actual case in Fig. 3-10b.

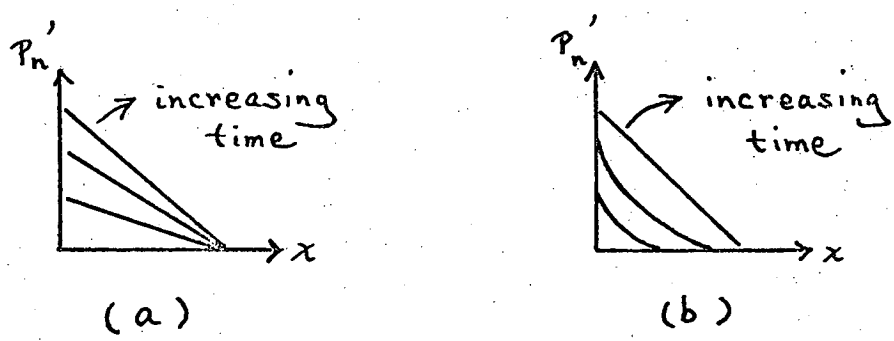


FIG. 3-10a and 3-10b. (a) Build up of the base charge predicted by the model, (b) Actual base charge build up.

Due to this excess phase effect, there may be some small discrepancies in the switching times.

(ii) **Thermal** effects of transistor parameters are not taken into account.

Among some of the important ones are β_N, β_I, I_{CS}, I_{ES}, T_{CN}, I_{CI}.

(iii) High level injection[14].

When the injected minority carrier concentration becomes comparable with that of the majority carriers, side effects may become appreciable and affect the performance of the transistor. These effects may cause:

(a) changes in contact potential,
(b) changes in collector resistance due to conductivity modulation by the minority carriers,
(c) appreciable drift current flowing in a primarily diffusion transistor,
(d) concentration of transistor action at the peripheral of emitter contacts,
(e) avalanche multiplication.

These effects are not included in CIRCUS, although junction-breakdown phenomena are specially handled by CIRCUS. Once breakdown voltage is reached, a special warning message is issued.

These constraints may lead to the conclusion that there is much more to be desired from the model. Yet it should be emphasized that these constraints are all higher-order effects and do not become important unless under extreme conditions. Moreover, many of the effects are actually included in the parameter measurements. For instance, the T_{CN} measurement to a certain extent includes the effect of the distributive nature of the base. Detailed discussion of parameter measurements will be presented in Chapter 4.

B. THE DIODE MODELS

a. Conventional Diode

$$C = \frac{a}{(\Theta + V_D)^n} + K_D I_s e^{\Theta V_D},$$

$$I_D = I_s \left(e^{\Theta V_D} - 1\right).$$

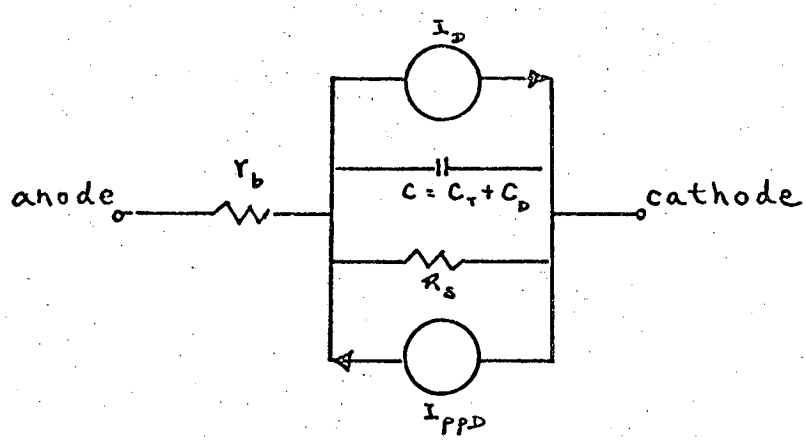


FIG. 3-12. Switching Diode Model.

Basically the switching diode model (Fig. 3-12) is embodied in the transistor model. It is just half of a transistor, minus the dependent current generator with similar equations for the junction capacitance and diffusion capacitance,

$$C_T = \frac{a}{(\Theta + V_D)^n}, \tag{3-15}$$

$$C_D = K_D (I_D + I_s). \tag{3-16}$$

The diode current, primarily diffusion, follows the well-known diode equation

$$I_D = I_s\left(e^{\Theta V_D}-1\right), \tag{3-17}$$

where I_s = reverse saturation current,

$$\Theta = \frac{q}{MKT}.$$

Again, I_{ppD} is the photocurrent generator.

b. Zener Diode

In a zener diode, besides the normal diode operation, the breakdown process becomes a vital part of the diode's current-voltage characteristic. Thus the zener diode model can be properly derived from the normal diode model by adding the carrier multiplication process. Miller empirically[15] showed that the reverse current of a zener diode follows

$$I_R = I_s N, \tag{3-18}$$

$$N = \frac{1}{\left(1 - \frac{V}{BV}\right)^m}, \tag{3-19}$$

where I_s = reverse saturation current without zener multiplication,

BV = breakdown voltage,

m = constant.

Therefore, if I_R (Eq. 3-18) is substituted for the reverse current I_s in the switching diode model (Fig. 3-12), a zener diode model results.

c. Tunnel Diode

Since the tunnel diode is formed by a p-type and an n-type material, one would expect its model (Fig. 3-13) to be similar to a switching diode (Fig. 3-12).

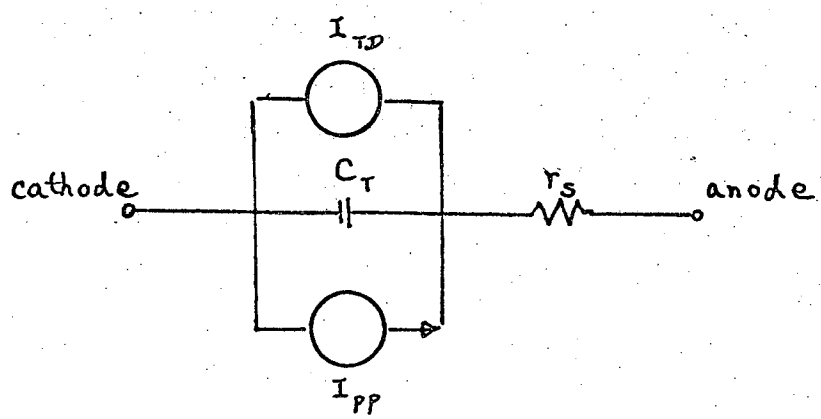


FIG. 3-13. Tunnel Diode Model.

The difference between a tunnel diode and a conventional diode is that due to degenerate doping a tunnel diode has a negative conductance region in its I-V characteristic (Fig. 3-14).

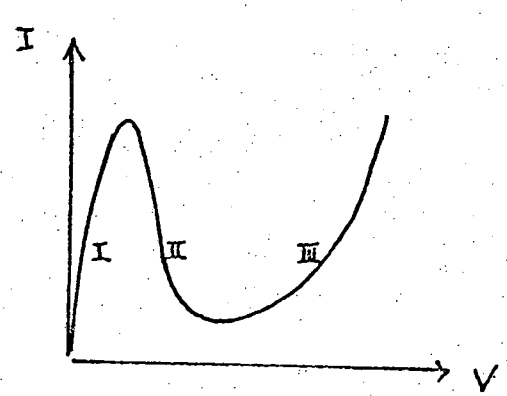


FIG. 3-14. I-V Curve of a Tunnel Diode.

Because of this special doping, the junction capacitance and the diffusion capacitance are extremely difficult to measure. Therefore, the diffusion capacitance is not included in the tunnel diode model (Fig. 3-13), and the junction capacitance is treated as a constant instead of voltage-dependent as in Eq. (3-9). Furthermore, it is obvious from the I-V curve (Fig. 3-14) that the curve has three distinct regions (I, II, and III) each of which can be represented by a form involving exponential term(s). A linear combination of these terms will then approximate the I-V curve:

$$I_{TD} = I_{tunnel} + I_{excess} + I_{diffusion}$$
$$= A_A V e^{-AV} + B_B\left(e^{B_1 V} - e^{-B_2 V}\right) + C_C\left(e^{CV} - 1\right) . \qquad (3\text{-}20)$$

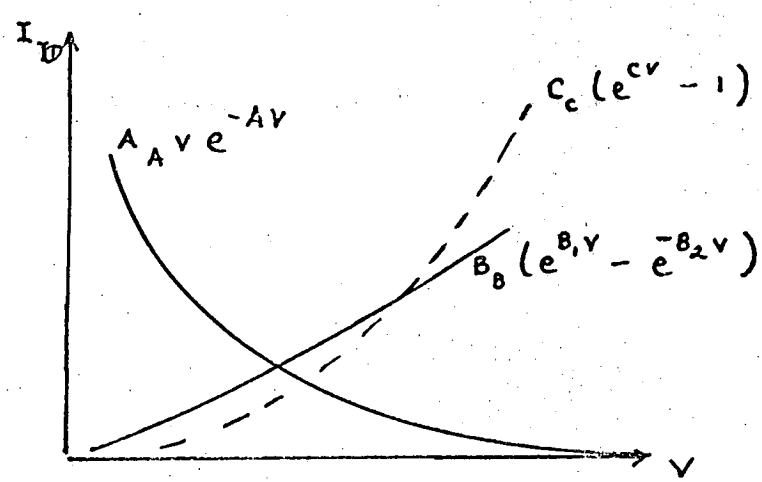
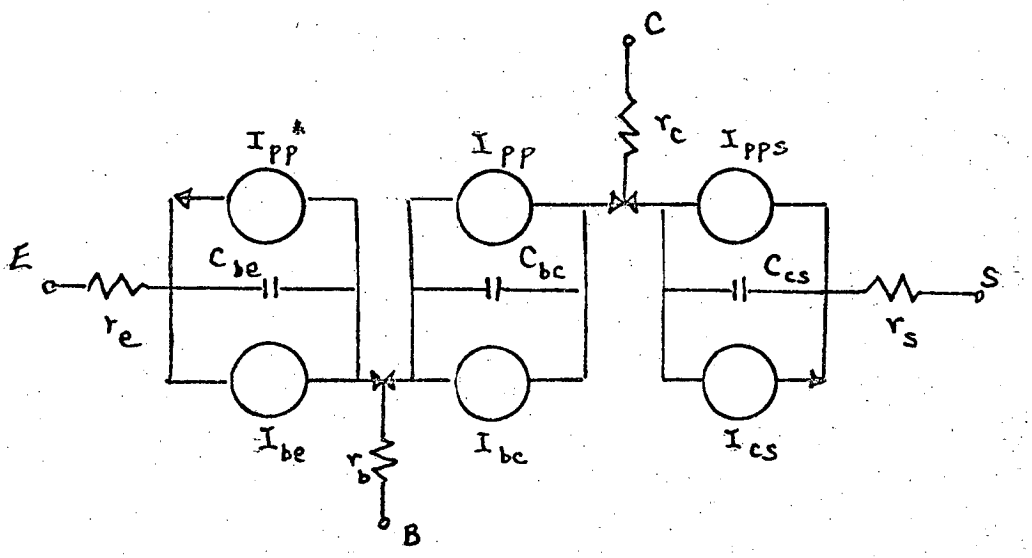


FIG. 3-15. The Various Current Components of the Tunnel Diode Current, I_{TD}.

d. The Four-Layer Device Model

The four-layer device model (Fig. 3-16) may represent either a silicon-controlled rectifier or transistor with a substrate as in an integrated circuit. It is an extension of the transistor model by connecting two complementary transistors to each other (Fig. 3-17):



$$C_{be} = \frac{a_1}{(\phi_1 + V_{be})^{n_1}} + \Theta_{N_1} T_{CN_1} I_{EC} e^{\Theta_{N_1} V_{be}},$$

$$C_{bc} = \frac{a_2}{(\phi_2 + V_{bc})^{n_2}} + \Theta_{I_1} T_{CI_1} I_{CE} e^{\Theta_{I_1} V_{bc}} + \Theta_{N_2} T_{CN_2} I_{BS} e^{\Theta_{N_2} V_{bc}},$$

$$C_{cs} = \frac{a_3}{(\phi_3 + V_{cs})^{n_3}} + \Theta_{I_2} T_{CI_2} I_{SB} e^{\Theta_{I_2} V_{cs}},$$

$$I_{be} = \left(1 + \frac{1}{\beta_{N_1}}\right) I_{EC}\left(e^{\Theta_{N_1} V_{be}} - 1\right) - I_{CE}\left(e^{\Theta_{I_1} V_{bc}} - 1\right),$$

$$I_{bc} = \left(1 + \frac{1}{\beta_{N_2}}\right) I_{BS}\left(e^{\Theta_{N_2} V_{bc}} - 1\right) + \left(1 + \frac{1}{\beta_{I_1}}\right) I_{CE}\left(e^{\Theta_{I_1} V_{bc}} - 1\right) - I_{EC}\left(e^{\Theta_{N_1} V_{be}} - 1\right) - I_{SB}\left(e^{\Theta_{I_2} V_{cs}} - 1\right),$$

$$I_{cs} = \left(1 + \frac{1}{\beta_{I_2}}\right) I_{SB}\left(e^{\Theta_{I_2} V_{cs}} - 1\right) - I_{BS}\left(e^{\Theta_{N_2} V_{bc}} - 1\right).$$

FIG. 3-16. Four-Layer Device Model.

FIG. 3-17.(a) Integrated circuit NPN transistor Equivalent circuit.

(b) Silicon-controlled Rectifier Equivalent Circuit.

C. THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET) MODEL

As can be seen in the construction of a typical junction field-effect transistor (Fig. 3-18), the device consists of two p-n junctions.

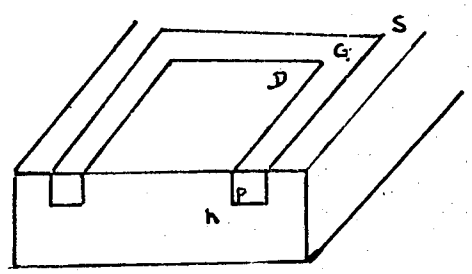


FIG. 3-18. N-Channel Junction Field-Effect Transistor.

Consequently, some of the pertinent concepts for a diode are used for the JFET too.

Just as in the transistor case, the modelling attempts to depict the behavior of the device in terms of terminal currents and voltages.

To a first approximation, the familiar I-V characteristic (Fig. 3-19) looks exceedingly similar to a series of exponentially rising curves of the form

$$I_D = I_{SY}\left(1 - e^{-\Theta_X V_{SD}}\right). \tag{3-21}$$

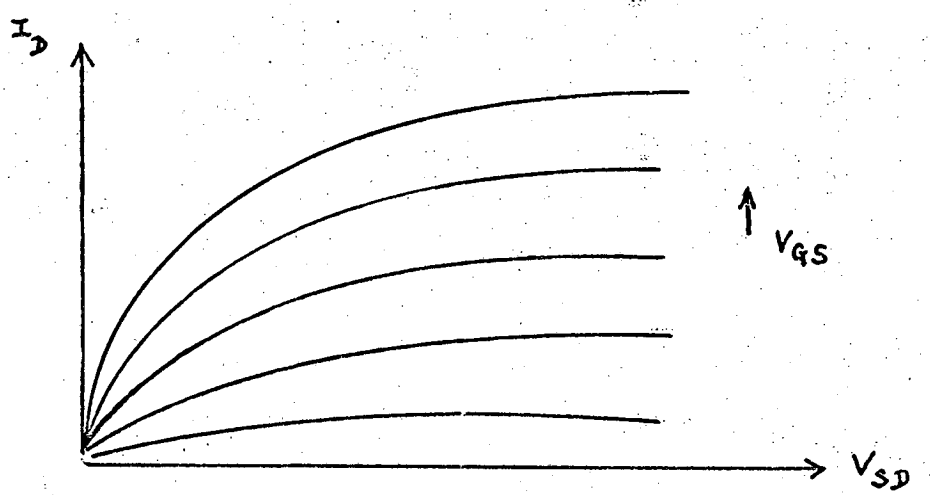


FIG. 3-19. Current Voltage Characteristics of the n-channel JFET.

Therefore, the dominant dc behavior of a JFET can be modeled by a current generator I_D. This generator depends exponentially on the source-drain voltage (V_{SD}) and gate-source voltage (V_{GS}):

$$I_D = I_{SY}\left(1 - e^{-\Theta_X V_{SD}}\right), \tag{3-22a}$$

$$I_{SY} = f_1\,(V_{GS}), \tag{3-22b}$$

$$\Theta_X = f_2\,(V_{GS}). \tag{3-22c}$$

In practice, for a large source-drain voltage the source drain current is approximately constant and Eq. (3-22a) predicts

$$I_D \approx I_{SY}. \tag{3-23}$$

Therefore, the model is quite accurate for a large source-drain voltage. However, for operation below pinch off, an accurate relation for the n-channel drain current * is[16]

$$I_D = G_o \left\{ V_{SD} - K \left[\left(V_{SD} + \phi - V_{GS} \right)^{3/2} - \left(\phi - V_{GS} \right)^{3/2} \right] \right\}, \tag{3-24}$$

where G_o, K are constants,

ϕ = contact potential;

but Eq. (3-22a) predicts

$$I_D = \Theta_X V_{SD} - \frac{\left(\Theta_X V_{SD}\right)^2}{2!} + \frac{\left(\Theta_X V_{SD}\right)^3}{3!} + \cdots. \tag{3-25}$$

Obviously Eq. (3-24) and Eq. (3-25) are slightly different. To minimize the discrepancy, I_{SY} and Θ_X should be measured carefully.

As mentioned earlier, there are two p-n junctions in a JFET so that two equivalent diode models can be used for the junctions. In other words, the current flowing through a junction is

$$I = I_o \left(e^{\Theta V} - 1 \right), \tag{3-26}$$

where I_o, Θ are constants,

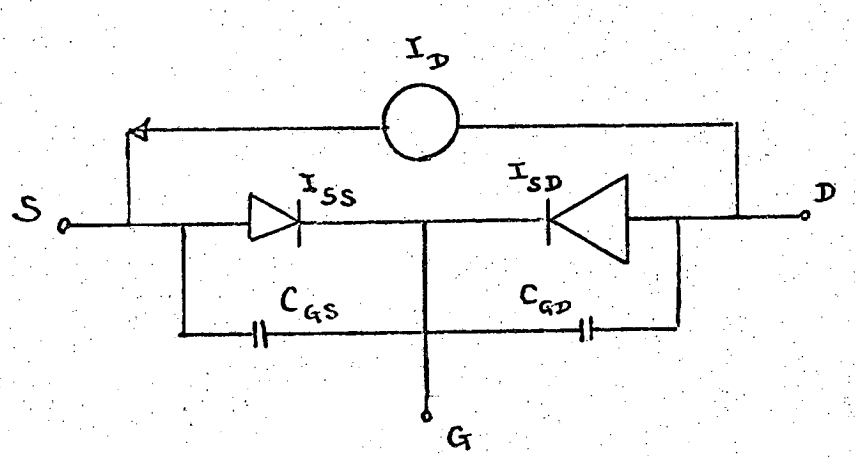
and the capacitance across a junction is

$$C = \frac{C_o}{(\phi + V)^n}. \tag{3-27}$$

Then the JFET model becomes (Fig. 3-20).

---

* For p channel, the sign of the voltage terms in Eq. (3-24) should be reversed.



$$I_D = I_{SY}\left(1 - e^{-\Theta_X V_{SD}}\right),$$

$$I_{SY} = f_1\,(V_{GS}),$$

$$\Theta_X = f_2(V_{GS}),$$

$$I_{GS} = I_{SS}\left(e^{\Theta_S V_{GS}} - 1\right),$$

$$I_{GD} = I_{SD}\left(e^{\Theta_D V_{GD}} - 1\right),$$

$$C_{GS} = \frac{C_{OS}}{(V_S + V_{GS})^{n_S}},$$

$$C_{GD} = \frac{C_{OD}}{(V_D + V_{GD})^{n_D}}.$$

FIG. 3-20. Simplified n-Channel JFET Model.

Incorporating ohmic resistances and photocurrent generators, the complete JFET model is

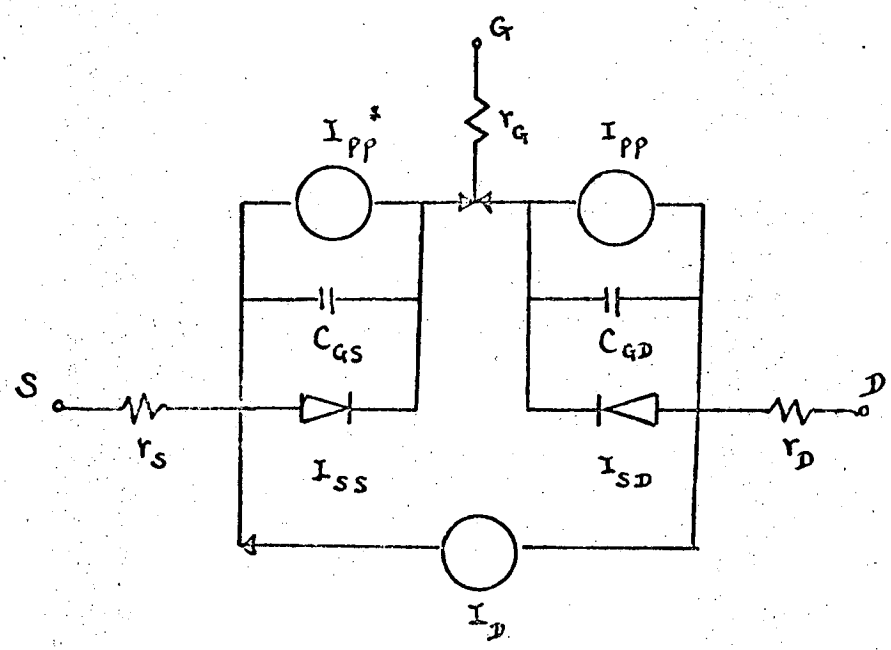


FIG. 3-21. Complete JFET Model.

It should be pointed out that the JFET is primarily a majority carrier device where current flow is mainly majority drift current. Therefore, there is no diffusion capacitor in the model. Moreover, of the various dependent current generators in the model, the most important is I_D, because under normal operation the two junctions are always reverse biased.

D. UNIJUNCTION TRANSISTOR (UJT) MODEL

Although there is no built-in model for the UJT, Steele[17] has suggested a two-transistor model which can be used in CIRCUS.*

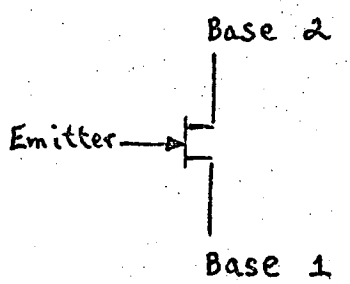


FIG. 3-22. UJT Symbol.

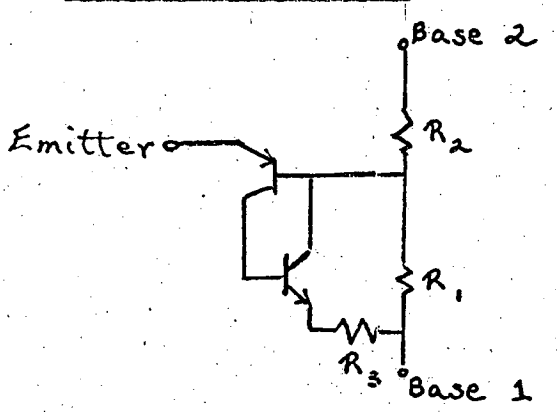


FIG. 3-23. Steele's UJT Model.

The model in Fig. 3-23 is most suitable for CIRCUS because the two transistors connected back-to-back form a four-layer device which is standard in CIRCUS.

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* D. A. Hodges has suggested a simpler two-transistor UJT model (see ref. 18).

CHAPTER 4. PARAMETER MEASUREMENTS [19]

This chapter describes the techniques used in measuring the device parameters. These techniques are far from unique, but they are the outgrowth of a comparison between different methods. They represent a compromise between ease and accuracy of the measurements.

Each of the six built-in device models in CIRCUS requires a different number of parameters (Table 4-1). However, many of the techniques are common to several device models and therefore will not be repeated for each device type.

It should be pointed out that in the models, each parameter is considered as a distinct entity. In actual measurement it is never possible to isolate one parameter from the other parameters and second-order effects. The best one can do is to minimize the contributions due to other parameters in each measurement. The inevitable inclusion of second-order effects in each parameter measurement tends to add accuracy to the models.

A. TRANSISTOR PARAMETERS

a. T_{CN}, T_{CI}

Of the two main ideas contained in the transistor model (viz., the charge control concept and the exponential I-V characteristic of the junctions) the charge control concept pertains more to the switching time estimates. Therefore, one would use the charge control idea to measure T_{CN}, T_{CI}.

If interest is focused on the time response of the continuity equation (3-2), one can obtain the basic charge control equation by letting the second derivative with respect to distance in equation (3-2) go to zero:

$$I_{BN} = \frac{Q_{BN}(t)}{\tau_{BN}} + \frac{d\,Q_{TN}(t)}{dt}, \qquad (4\text{-}1)$$

TYPE OF DEVICE	NO. OF REQUIRED SINGLE-VALUED PARAMETERS	SINGLE-VALUED PARAMETERS	NO. OF TABLE-VALUED PARAMETERS	TABLE-VALUED PARAMETERS ALL FUNCTIONS OF CURRENT
Transistor	13	RB, RC, RE, A1, PHI1, N1, A2 PHI2, N2 IES, ICS, THETAN, THETAI	4	BN, BI, TCN, TCI
Diode	8	RB, RS, A, PHI, N, IS, THETA, KD	0	
Tunnel Diode	9	RS, CJ, AA, A, BB, B1, B2, CC, C	0	
Zener Diode	10	RB, RS, A, PHI, N, IS, THETA, KD, M, BV	0	
Four-Layer Device	21	RE, RB, RC, RS, A1, PHI1, N1, A2, PHI2, N2, A3, PHI3, N3, ISN1, ISI1, ISN2, ISI2, THETN1, THETI1, THETN2, THETI2	8	BN1, BI1, BN2, BI2, TCN1, TCI1, TCN2, TCI2
Field-Effect Transistor	13	RS, RD, RG, COS, VS, NS, THETAS, ISS, COD, VD, ND, THETAD, ISD	2	THETAX, ISY

TABLE 4-1. Device Parameters required for each model.

The symbols have the same meaning as in the derivation of the models.

where Q_{TN} = total base charge

= base charge + charge in depletion layers

= $Q_{BN} + Q_{TC} + Q_{TE}$ (see Fig. 4-1),

T_{BN} = base time constant as defined in (3-36).

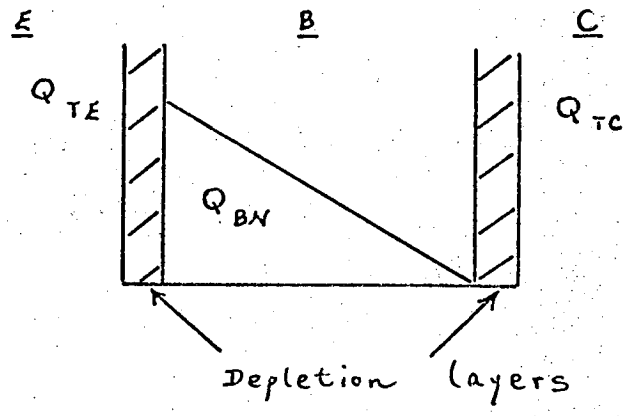


FIG. 4-1. Charges in the Base.

Since Q = CV, Eq. (4-1) can be put in terms of average depletion capacitances $\bar{C}_{ET}$ and $\bar{C}_{CT}$, with

$$\bar{C}_{ET} = \frac{\displaystyle\int_{|V_{EB\ initial}|}^{|V_{EB\ final}|} \frac{a_1}{(V_{eb} + \phi_1)^{n_1}}\, d|V_{eb}|}{|V_{EB\ final}| - |V_{EB\ initial}|}, \tag{4-2a}$$

$$\bar{C}_{CT} = \frac{\displaystyle\int_{|V_{CB\ initial}|}^{|V_{CB\ final}|} \frac{a_2}{(V_{cb} + \phi_2)^{n_2}}\, d|V_{cb}|}{|V_{CB\ final}| - |V_{CB\ initial}|}. \tag{4-2b}$$

Therefore, Eq. (4-1) becomes

$$I_{BN} = \frac{Q_{BN}(t)}{\tau_{BN}} + \bar{C}_{ET}\frac{d|V_{BE}(t)|}{dt} + \bar{C}_{CT}\frac{d|V_{CB}(t)|}{dt} + \frac{d|Q_{BN}(t)|}{dt}. \tag{4-3}$$

Remembering

$$I_{CN} = I_{ES}\left(e^{\theta_N V_{BE}} - 1\right), \tag{4-4}$$

therefore

$$\frac{d\,V_{BE}(t)}{dt} = \frac{1}{\frac{dI_{CN}}{dV_{BE}}}\;\frac{d\,I_{CN}(t)}{dt} \approx \frac{1}{\theta_N \bar{I}_{CN}}\;\frac{d\,I_{CN}(t)}{dt}, \tag{4-5}$$

where

$$\bar{I}_{CN} = \frac{I_{C\,final} - I_{C\,initial}}{2}.$$

Because

$$V_{CB}(t) = V_{CC} - V_{BE}(t) - KI_{CN}(t)\left(R_L + r_c\right), \tag{4-6}$$

where K, which is less than 1, is to account for the transistor loading effect on R_L,

then

$$\frac{d\,V_{CB}(t)}{dt} \approx K\,(R_L + r_C)\,\frac{d\,I_{CN}(t)}{dt} + \frac{1}{\theta_N \bar{I}_{CN}}\;\frac{d\,I_{CN}(t)}{dt}. \tag{4-7}$$

And from Eq. (3-14),

$$Q_{BN}(t) = I_{CN}(t)\,\tau_{CN}, \tag{4-8}$$

$$\frac{Q_{BN}(t)}{\tau_{BN}} = \frac{I_{CN}(t)}{\beta_N}. \tag{4-9}$$

Substituting equations (4-5), (4-7), (4-8), (4-9) in equation (4-3) gives

$$\beta_N I_{BN} = \beta_N \left[\tau_{CN} + (\bar{C}_{ET} + \bar{C}_{CT}) \frac{1}{\theta_N \bar{I}_{CN}} + K\, \bar{C}_{CT}\, (R_L + R_C) \right] \frac{d\, I_{CN}(t)}{dt} + I_{CN}(t); \tag{4-10}$$

solving Eq. (4-10),

$$I_{CN}(t) = \beta_N\, I_B \left(1 - e^{-\frac{t}{T}}\right), \tag{4-11}$$

where

$$T = \beta_N \left[\tau_{CN} + (\bar{C}_{CT} + \bar{C}_{ET}) \frac{1}{\theta_N \bar{I}_{CN}} + K\, \bar{C}_{CT}\, (R_L + r_c) \right]. \tag{4-12}$$

Since the 10% -90% turn on rise time (t_{rN}) is 2.2T,

then

$$t_{rN} = 2.2\, \beta_N \left[\tau_{CN} + (\bar{C}_{CT} + \bar{C}_{ET}) \frac{1}{\theta_N \bar{I}_{CN}} + K\, \bar{C}_{CT}\, (R_L + r_c) \right]. \tag{4-13}$$

Implicitly assumed in the charge control model, τ_{CN} is independent of collector current. Therefore, a plot of t_{rN} vs. $\frac{1}{\bar{I}_{CN}}$ will give a straight line and τ_{CN} can thus be extracted from the intercept. However, typical plots of t_{rN} vs. $\frac{1}{\bar{I}_{CN}}$ (Fig. 4-2) suggest T_{CN} is dependent on collector current.

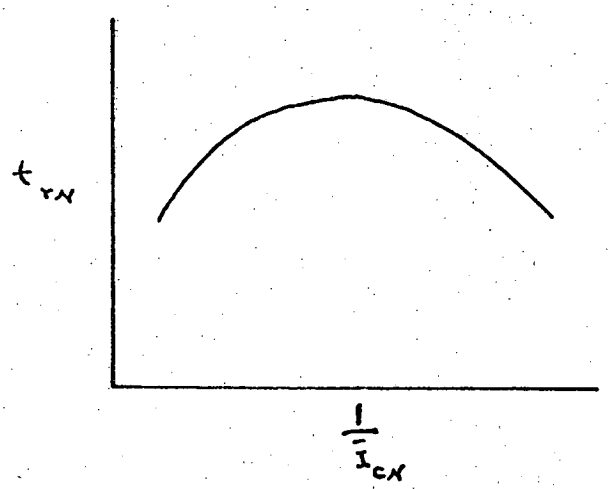


FIG. 4-2. Plot of t_{rN} vs. $\frac{1}{\bar{I}_{CN}}$.

To extract T_{CN}, Eq. (4-13) can be rearranged as

$$\tau_{CN} = \frac{t_{rN}}{2.2\beta_N} - \left[\left(\bar{C}_{CT} + \bar{C}_{ET}\right)\frac{1}{\theta_N \bar{I}_{CN}} + K\left(R_L + r_c\right)\bar{C}_{CT}\right]. \quad (4\text{-}14)$$

For small R_L, the approximation can be made,

$$\tau_{CN} \approx \frac{t_{rN}}{2.2\beta_N}. \quad (4\text{-}15)$$

The circuit used for the T_{CN} measurement is shown schematically in Fig. 4-3, and typical results are shown in Fig. 4-4 to Fig. 4-7.

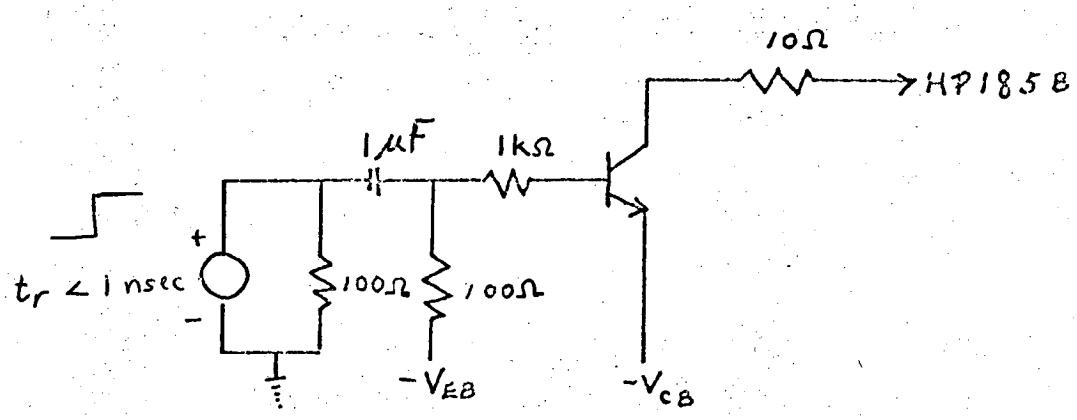


FIG. 4-3. T_{CN} Measurement (Similar measurement can be used to obtain T_{CI}).

b. I_{ES}, Θ_N, I_{CS}, Θ_I

from Eq. (3-4), at $V_{CB} = 0$

$$I_C = - I_{ES}\left(e^{\Theta_N V_{BE}} - 1\right); \tag{4-16}$$

if

$$V_{BE} >> -\frac{1}{\Theta_N}, \text{ then}$$

$$I_C \approx - I_{ES}\, e^{\Theta_N V_{BE}}. \tag{4-17}$$

A plot of log $|I_C|$ vs. V_{BE} yields Θ_N as the slope and I_{ES} as the intercept. The circuit used is as shown in Fig. 4-8.

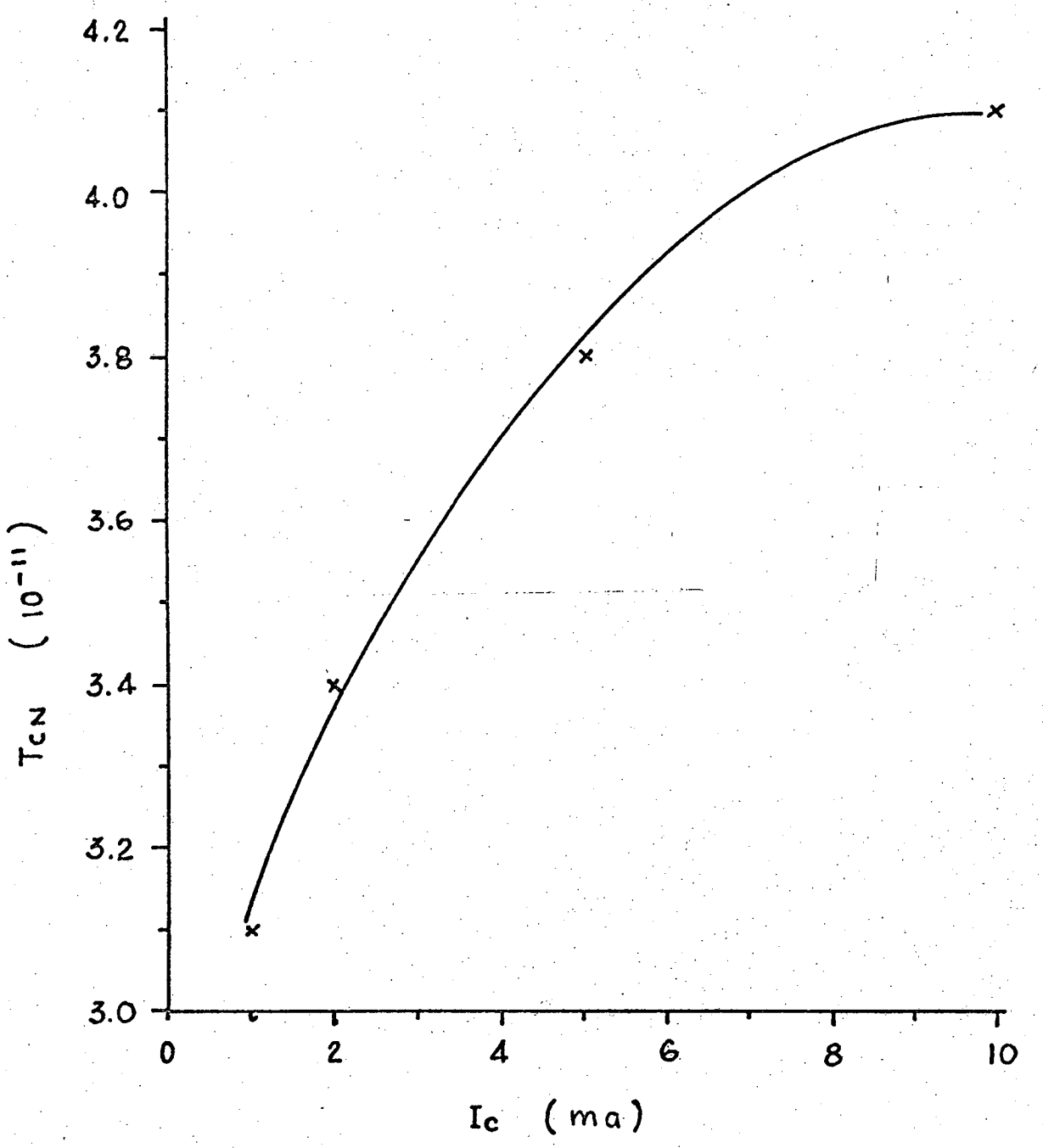


Fig. 4-4. T_{CN} vs I_C of 2N2369A.

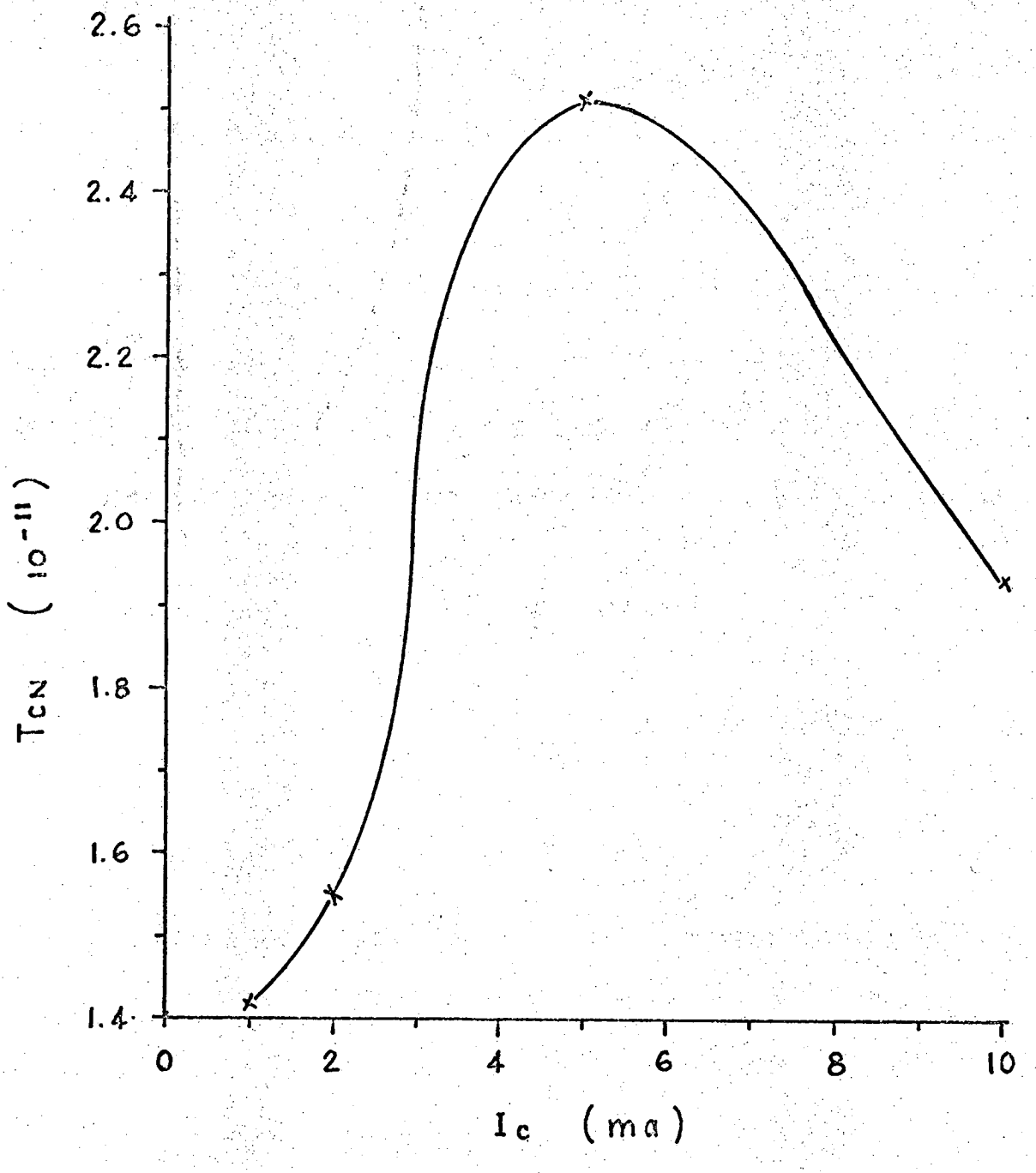


Fig. 4-5. T_{CN} vs I_C of 2N709.

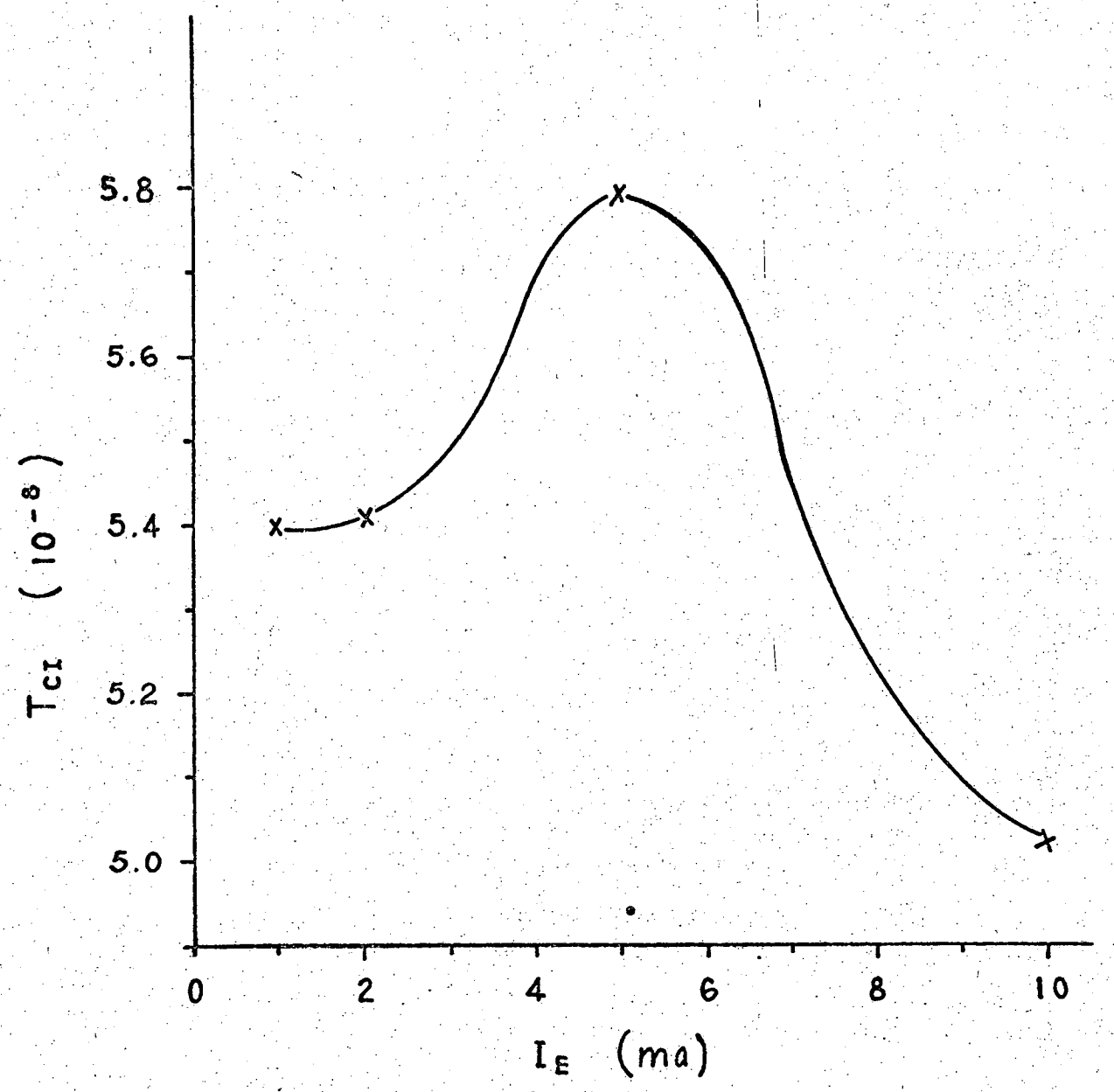


Fig. 4-6. T_{CI} vs I_E of 2N2369A.

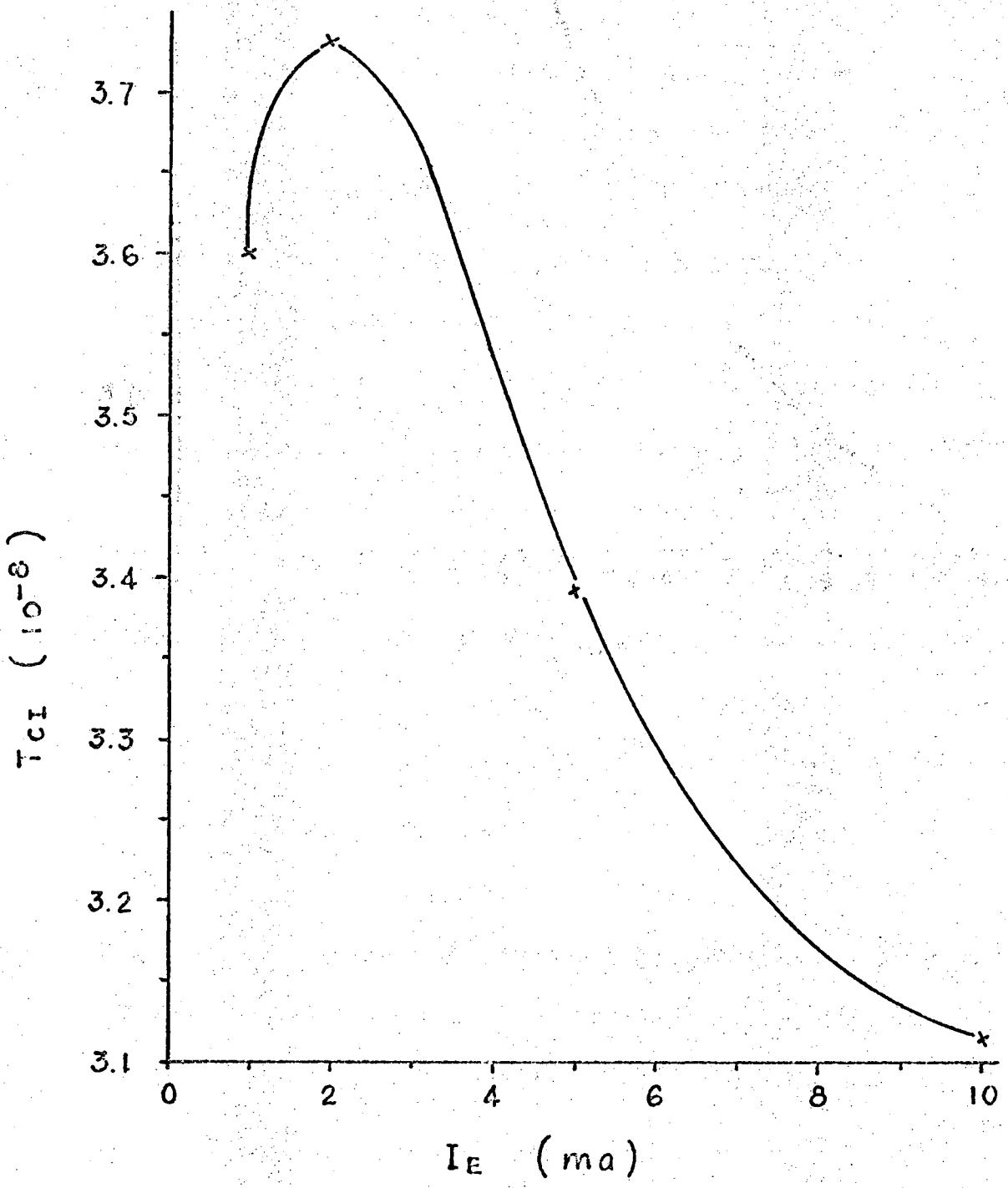


Fig. 4-7. T_{CI} vs I_E of 2N709.

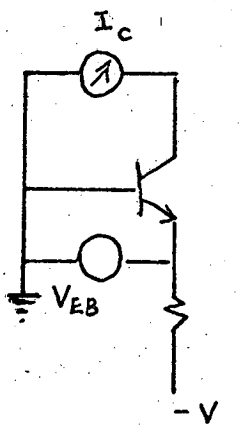


FIG. 4-8. Θ_N, I_{ES} Measurement.

A similar measurement (Fig. 4-9) can be used to obtain I_{CS} and Θ_I.

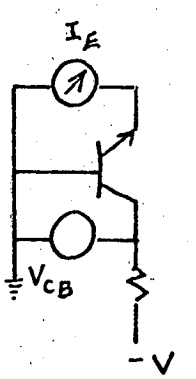


FIG. 4-9. Θ_I, I_{CS} Measurement.

At high current levels due to the onset of high-level injection, the straight-line behavior of log I_E vs. V_{CB} is no longer true. This can be interpreted as due to the ohmic voltage drop of the bulk resistance. Typical results are shown in Figs. 4-10 to 4-13 .

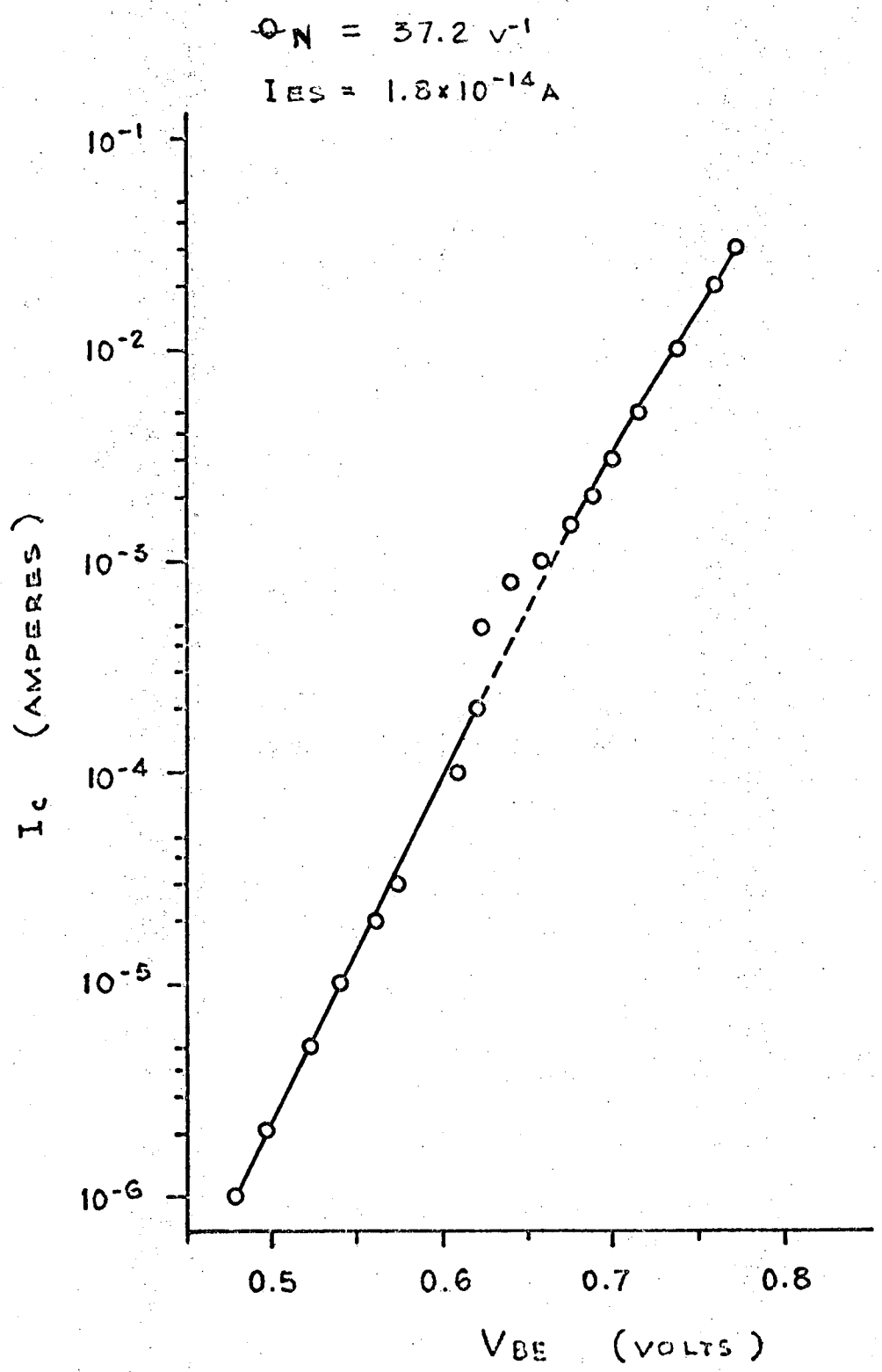


Fig.4-10. θ_N, I_{ES} of 2N2369A.

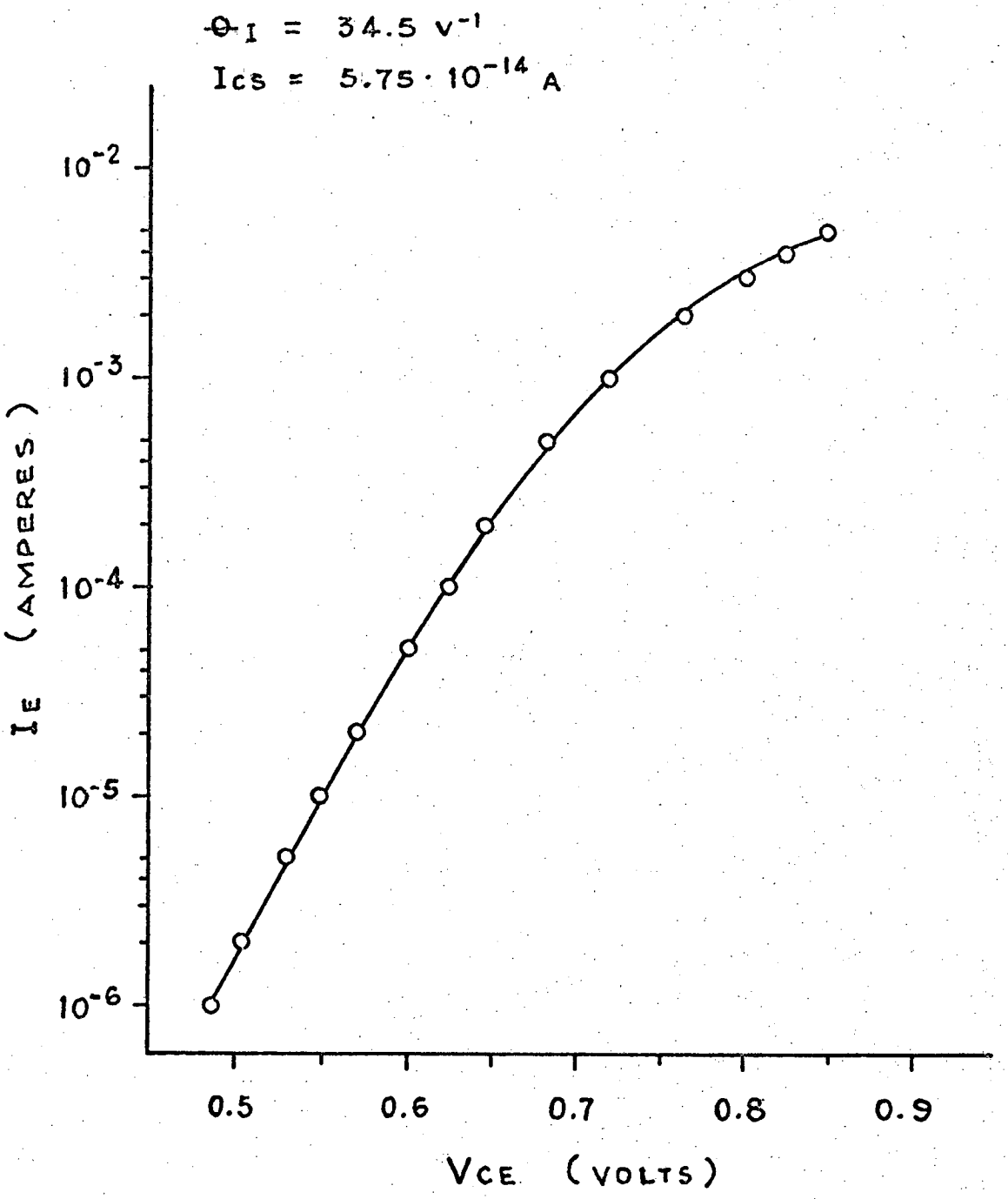


Fig. 4-11. θ_I, I_{CS} of 2N2369A.

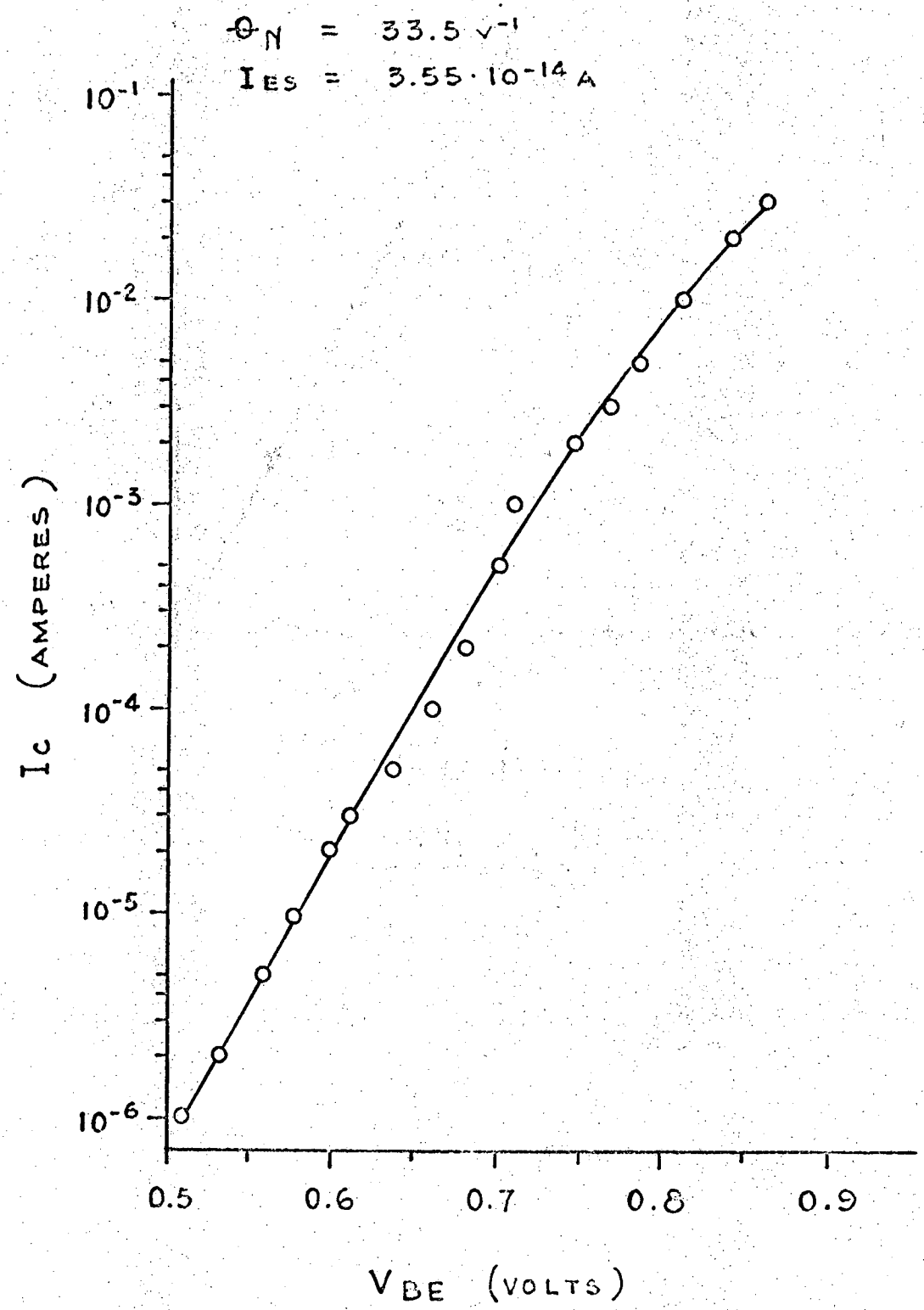


Fig. 4-12. θ_N, I_{ES} of 2N709.

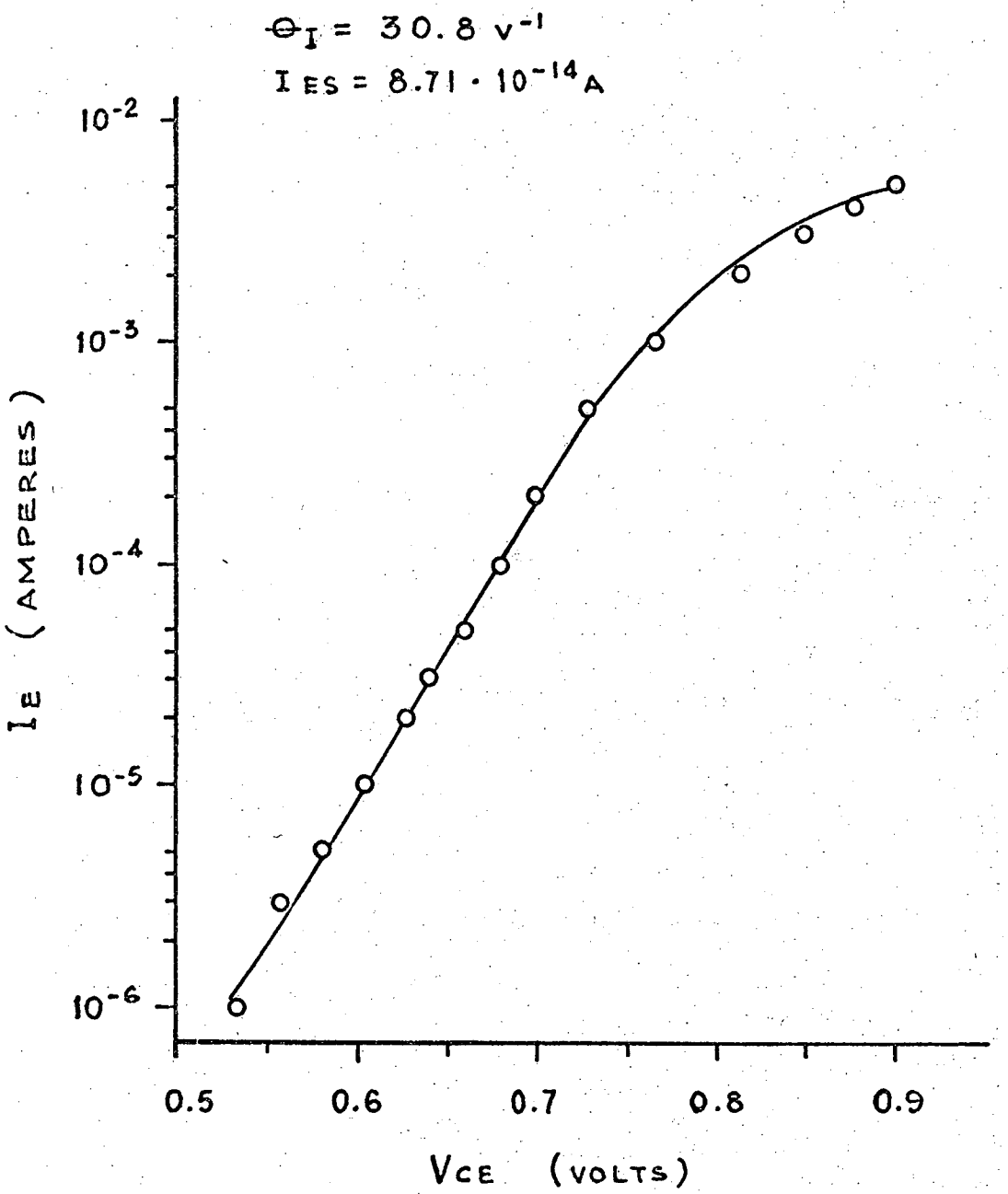


Fig. 4-13. θ_I, I_{CS} of 2N709.

c. r_b, r_e, r_c

r_b can be obtained from dc as well as ac measurement. As mentioned in the previous section, the dc r_b can be obtained from log $|I_C|$ vs. V_{eb} plot with

$$r_b \approx \frac{\Delta V}{I_{C_1}} \beta_N \quad \text{at high current and small } r_e. \qquad (4\text{-}18)$$

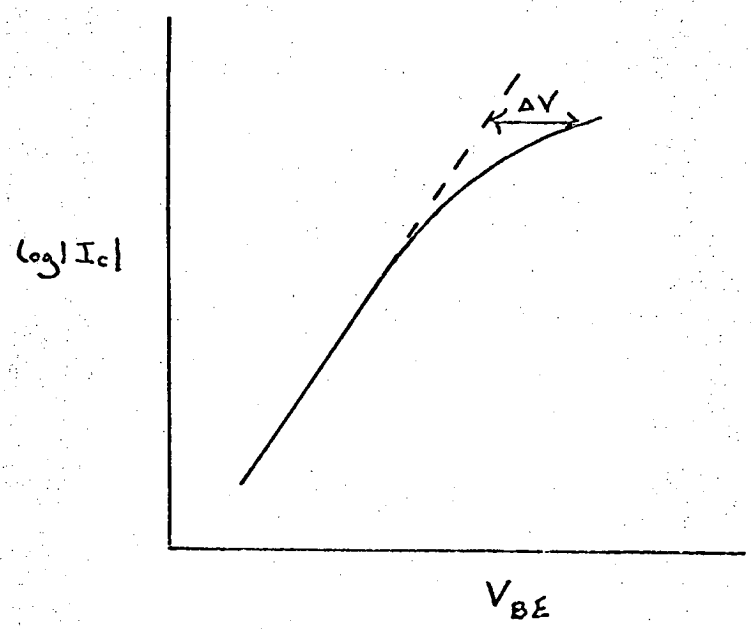


FIG. 4-14. dc r_b Measurement.

The ac measurement is based on the hybrid-π equivalent circuit (Fig. 4-15)[4].

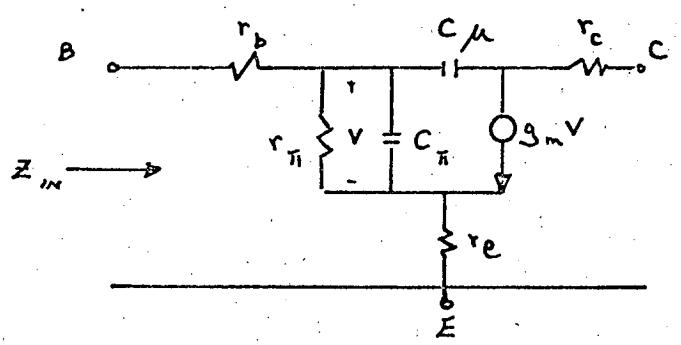


FIG. 4-15. Hybrid-π Equivalent Circuit.

It can be seen from Fig. 4-15 that when the imaginary part of Z_{in} equals zero, for small r_e the real part of Z_{in} is approximately r_b. To a first approximation, if $I_c r_b >> \frac{1}{\theta_N}$, and r_e small, then $R_{ey_{11}} \approx \frac{1}{r_b}$ at f_T. (Typical results: see Figs. 4-16 to 4-17.) This ac estimation gives a lower bound of r_b. Results of ac and dc measurement of r_b are shown in (Table 4-2). The apparent discrepancies between the two measurements are due to the distributive nature of the base, and current crowding effects.

	dc r_b	ac r_b at I_C = 5 mA
2N2369	50 Ohms	25 Ohms
2N709	84 Ohms	48 Ohms

Table 4-2. ac and dc r_b.

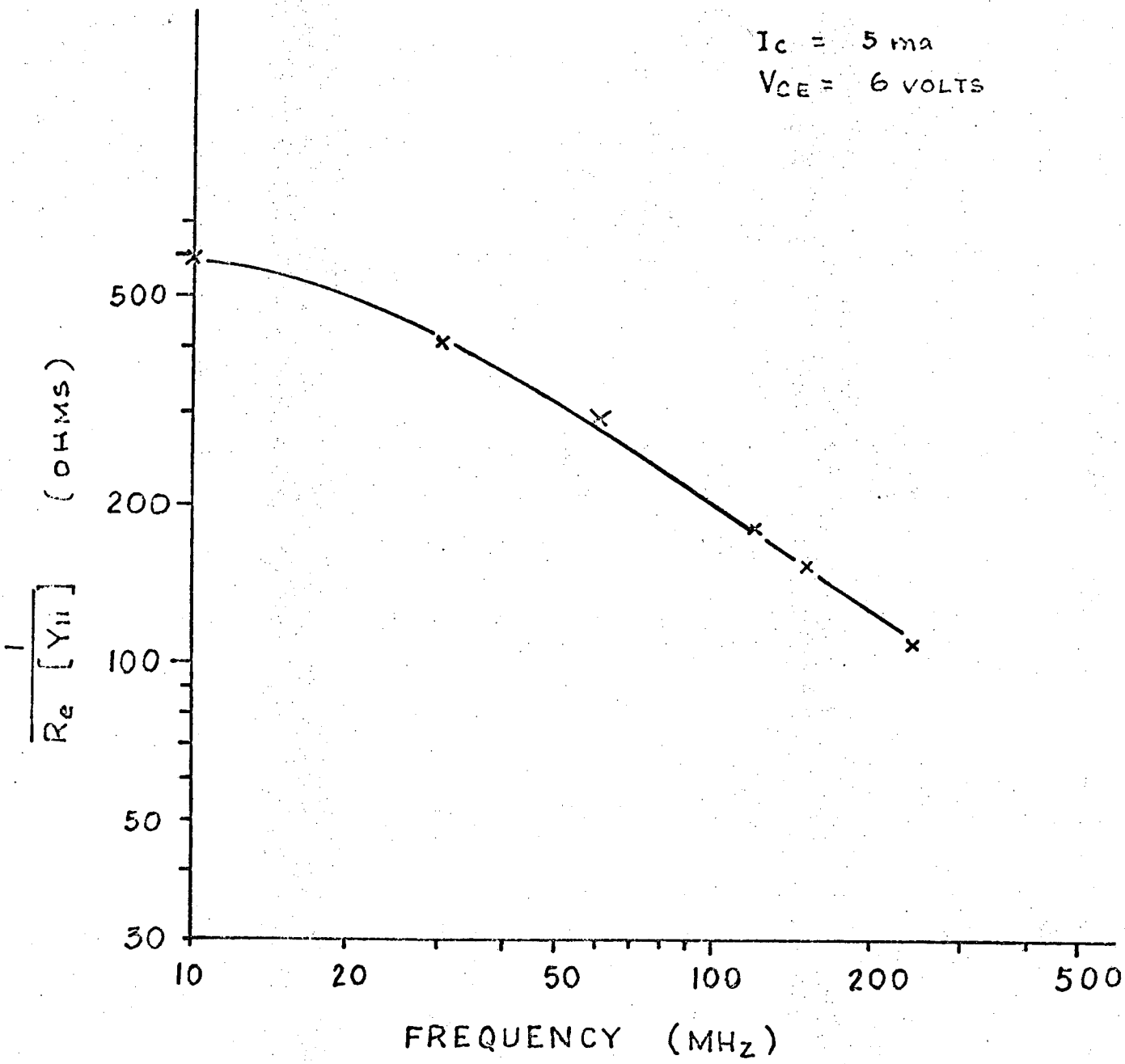


Fig. 4-16. ac r_b of 2N709 as obtained from Boonton R_x meter

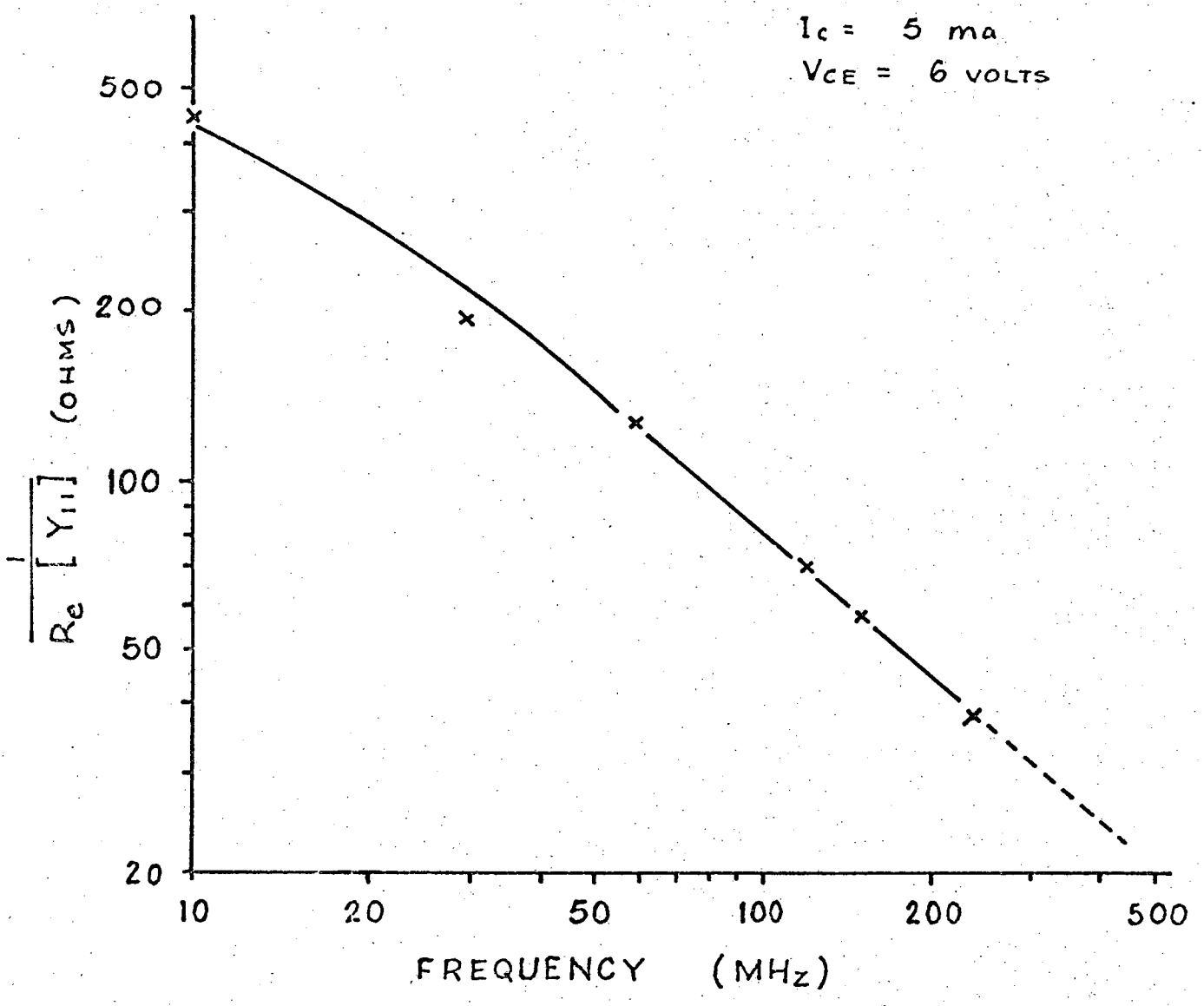


Fig. 4-17. ac r_b of 2N2369A as obtained from Boonton R_x meter

r_e can be obtained by plotting V_{CE} vs. I_B with the collector open (fig. 4-18).

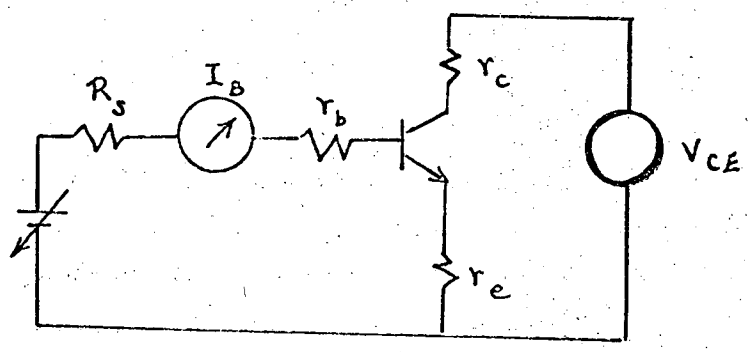


FIG. 4-18. r_e Measurement.

Since the collector is open, $V_{CE} = I_B\ r_e$ (i.e., the slope of V_{CE} vs. I_B is r_e). Practical measurements show, at low current level, the curve is not a straight line (fig. 4-19). This is due to the dependence of α on current level. For present-day transistors, r_e is always small and it can be assumed that r_e = 0.1 Ω instead of actually measuring it.

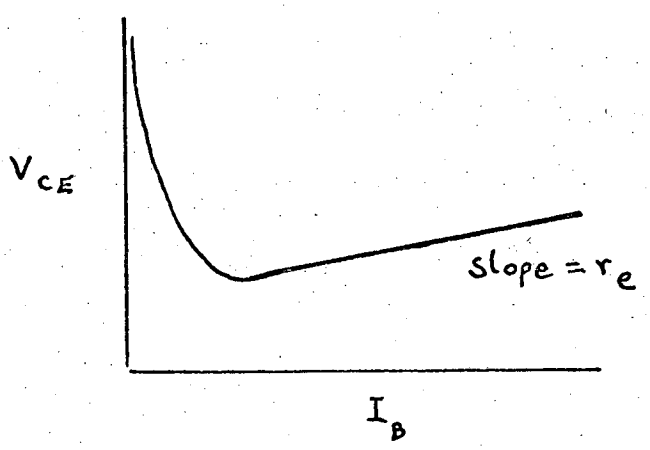


FIG. 4-19. V_{CE} vs. I_B.

Typical results of r_e are shown in Fig. 4-20 and Fig. 4-21 ; r_c can be obtained by plotting V_{CE} (sat) vs. I_C. At high collector current, the plot shows a straight line with a slope approximately equal to r_c. At low currents the nonideal behavior is again due to the anomalous nature of α. Typical results for r_c are shown in Figs. 4-22 and 4-23 .

d. a_1, ϕ_1, n_1, a_2, ϕ_2, n_2

Ideally, to obtain the three parameters for the depletion capacitance equation three linearly independent equations are needed:

$$C_T = \frac{a}{(V + \phi)^n} . \qquad (4\text{-}19)$$

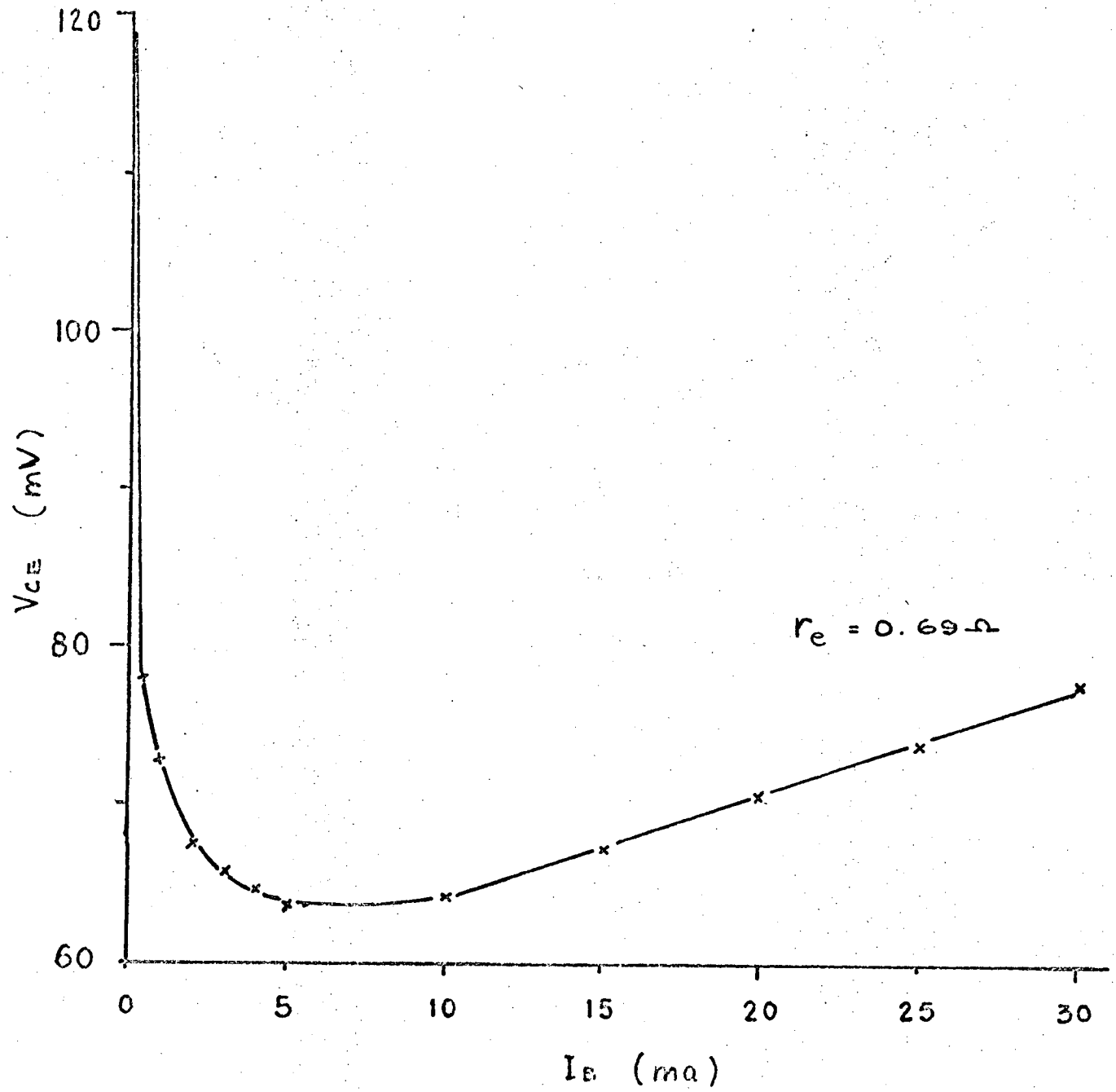


Fig. 4-20. r_e of 2N2369A.

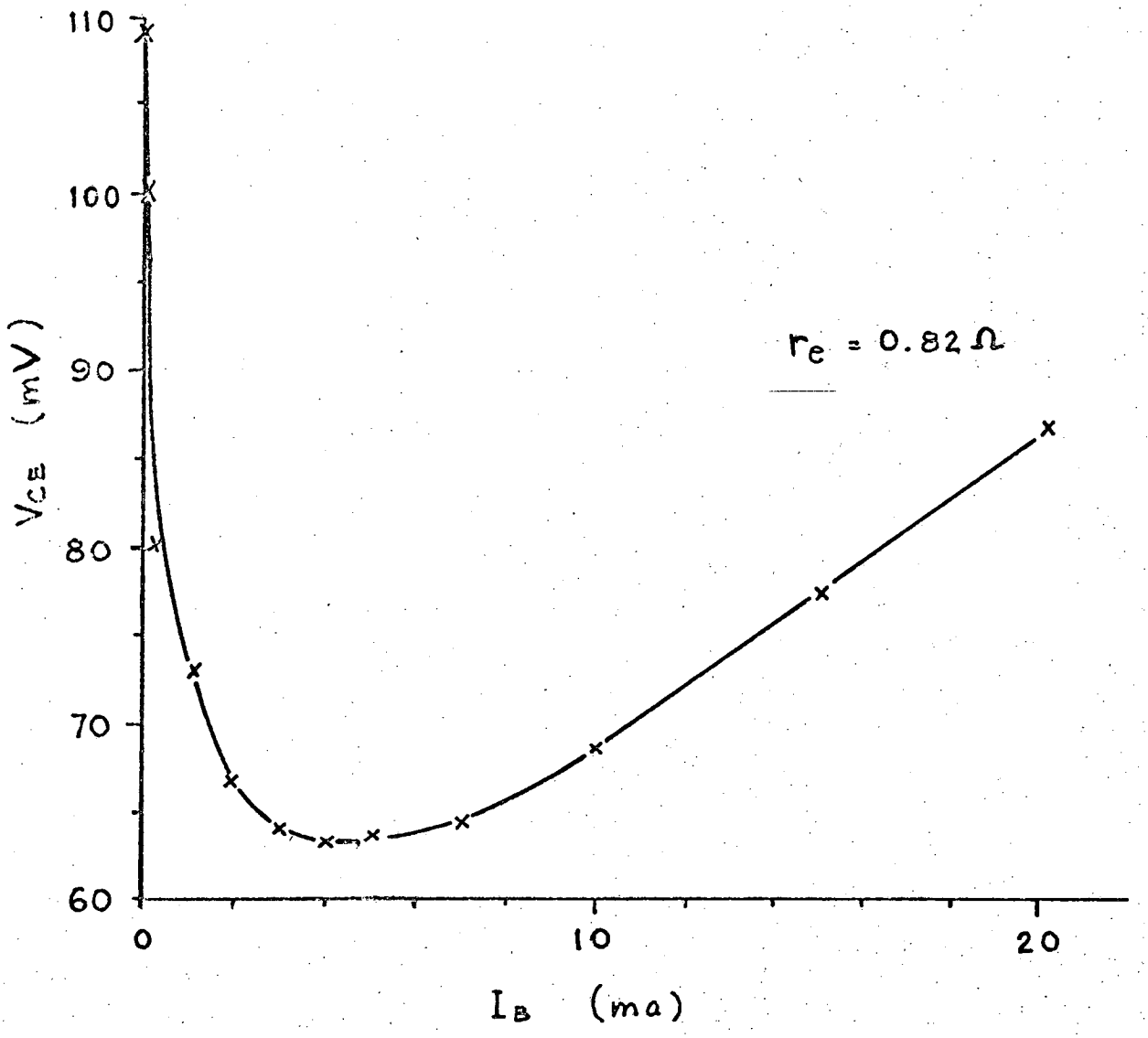


Fig. 4-21. r_e of 2N709.

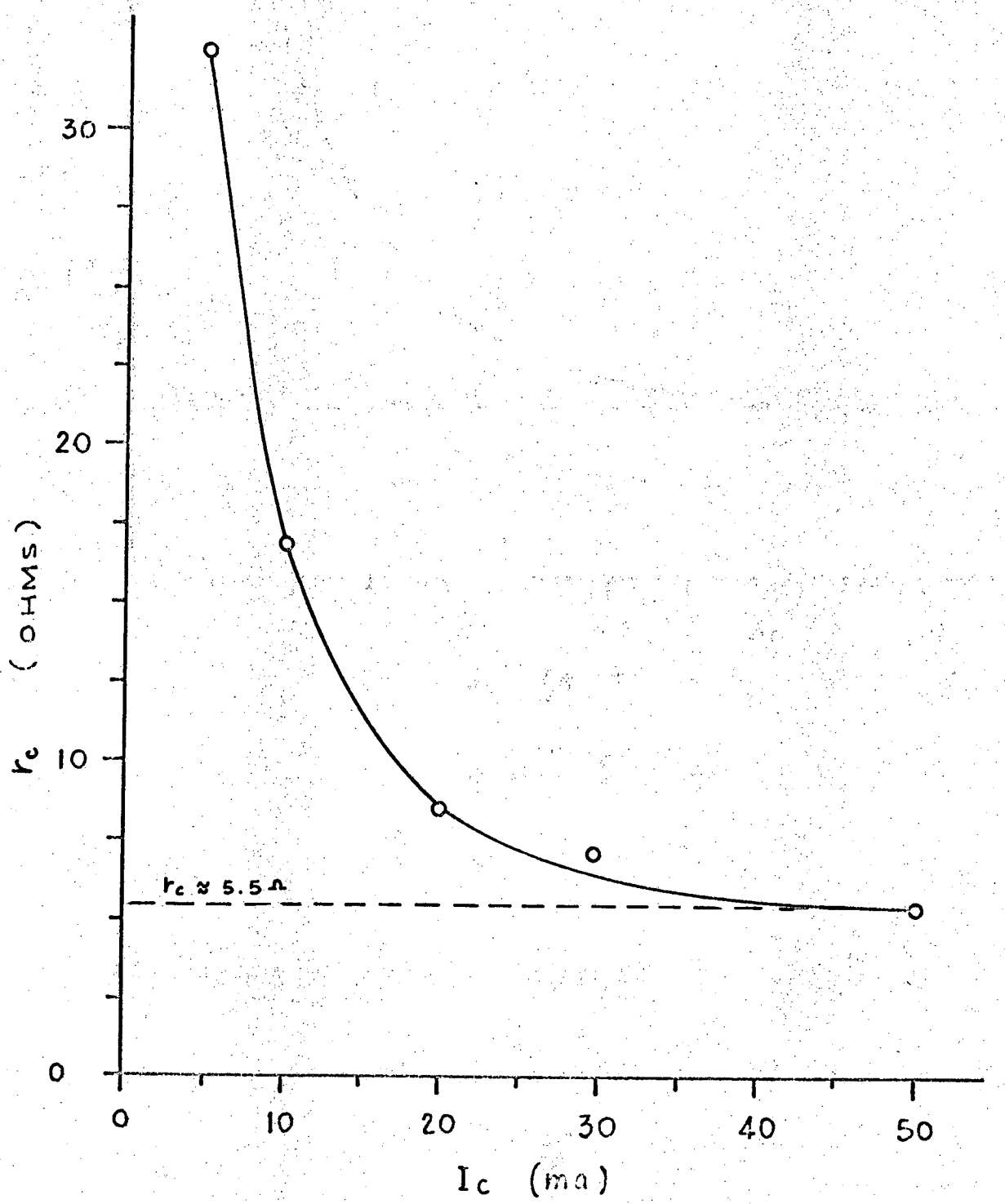


Fig. 4-22. r_c of 2N709.

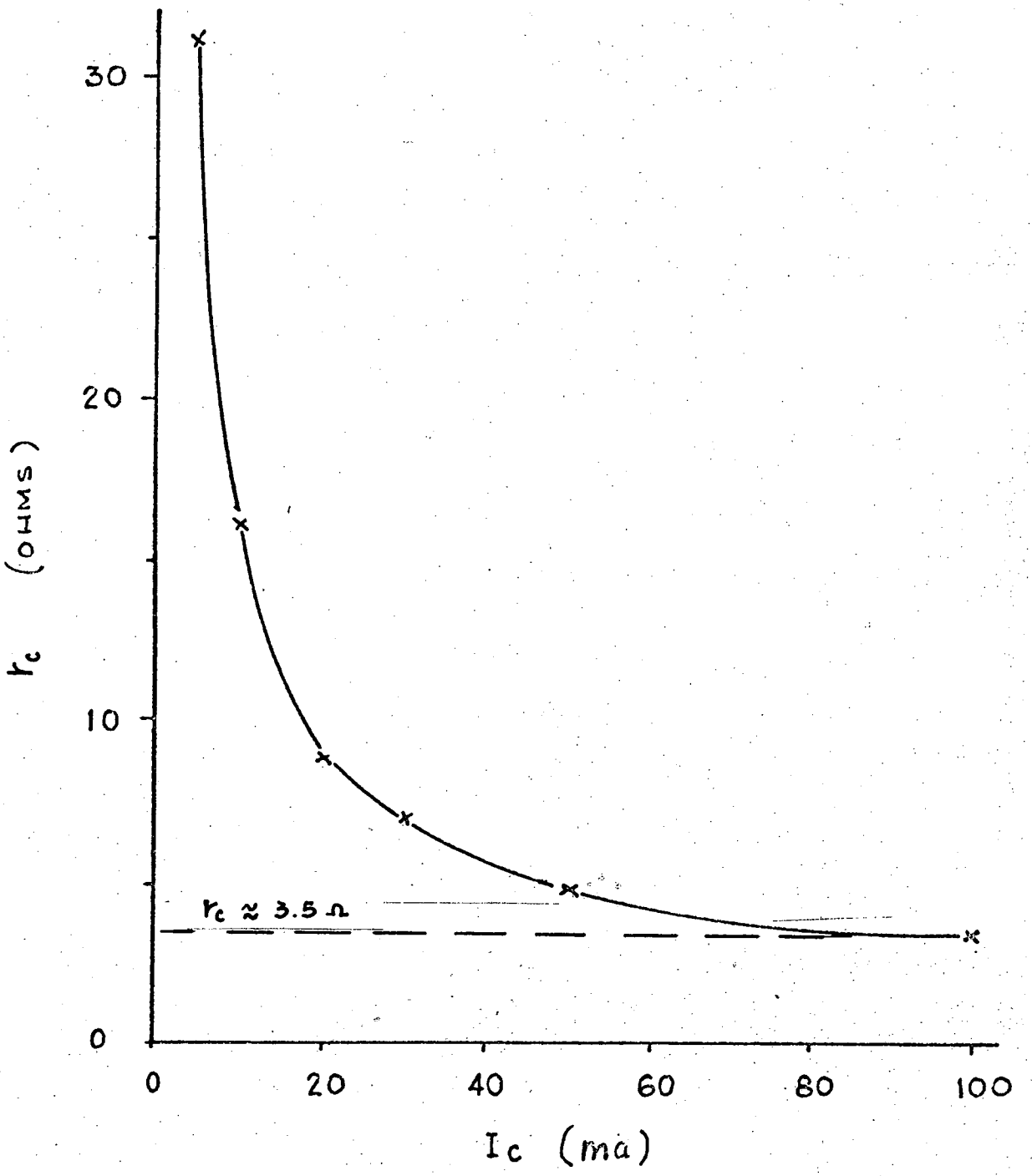


Fig. 4-23, r_c of 2N2369A.

Eq. (4-19) is but just one such equation and therefore, seemingly inadequate to solve the three parameters. However, as many measurements as desired can be made on C_T and suitable numerical techniques (least-square fit and some basic statistics)[20] can be used to extract the desired parameters from the measurements.

In the present case, the method has been tried to extract the three parameters from the depletion capacitance measurement. However, the numerical nature of the method tends to force the solution into a smaller contact potential than realistic. Therefore, it is modified so that a best fit is obtained over a range of contact potentials. This range, $\Delta\phi$, can best be selected from I_C vs. V_{BE} curves. Typical curves are shown in Fig. 4-24.

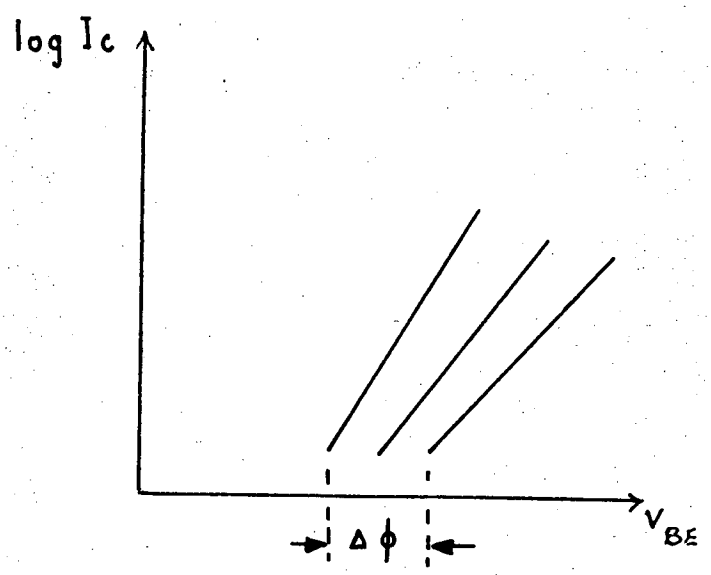


FIG. 4-24. I_C vs. V_{BE} to Select $\Delta\phi$ Range

Reasonable results are obtained from this method and are shown in Table 4-3 and Figs. 4-25, 4-26. (See Appendix B for detail discussion of the numerical programs.)

TRANSISTOR	a_1	n_1	ϕ_1	a_2	n_2	ϕ_2
2N2369A	5×10^{-12}	.30	.9	3.7×10^{-11}	.22	.9
2N709	9.6×10^{-13}	.38	.9	1.9×10^{-12}	.18	.9

TABLE 4-3. Junction Capacitance Parameters.

e. β_N, β_I

β_N (at 1 KHz) can be measured with the commercial instruments like the Baird Atomic BETA TESTER. To measure β_I a simple dc test circuit can be used, Fig. 4-27.

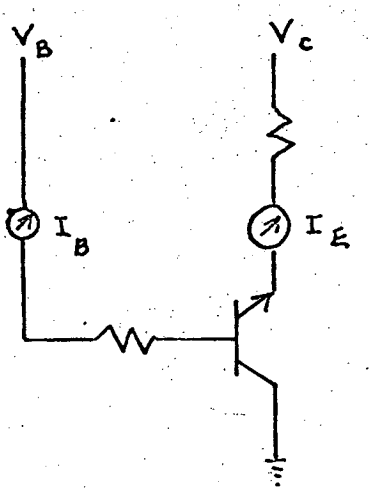


FIG. 4-27. β_I Measurement.

Results are shown in Figs. 4-28 through 4-31.

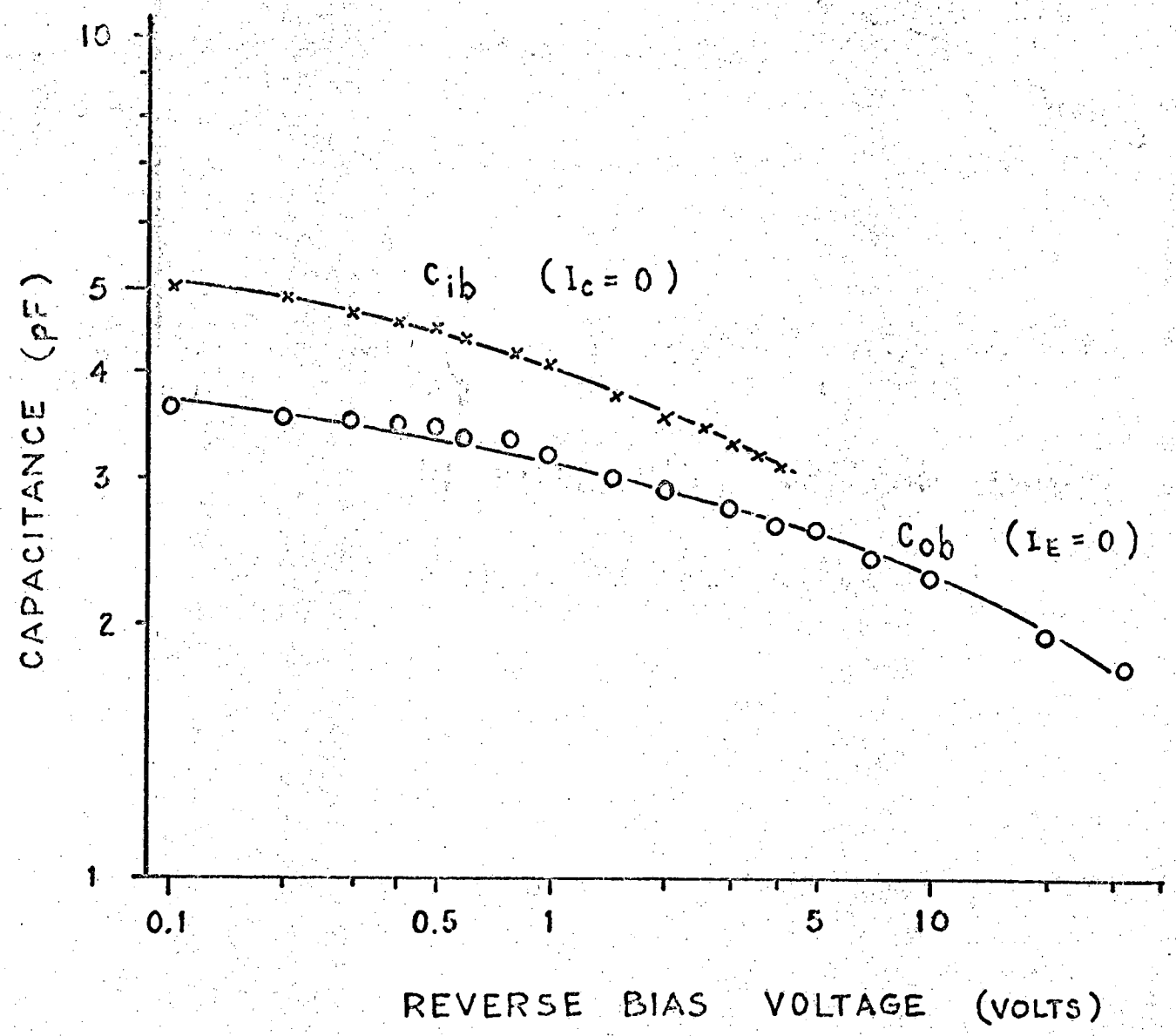


Fig. 4-25. Capacitances of 2N2369A.

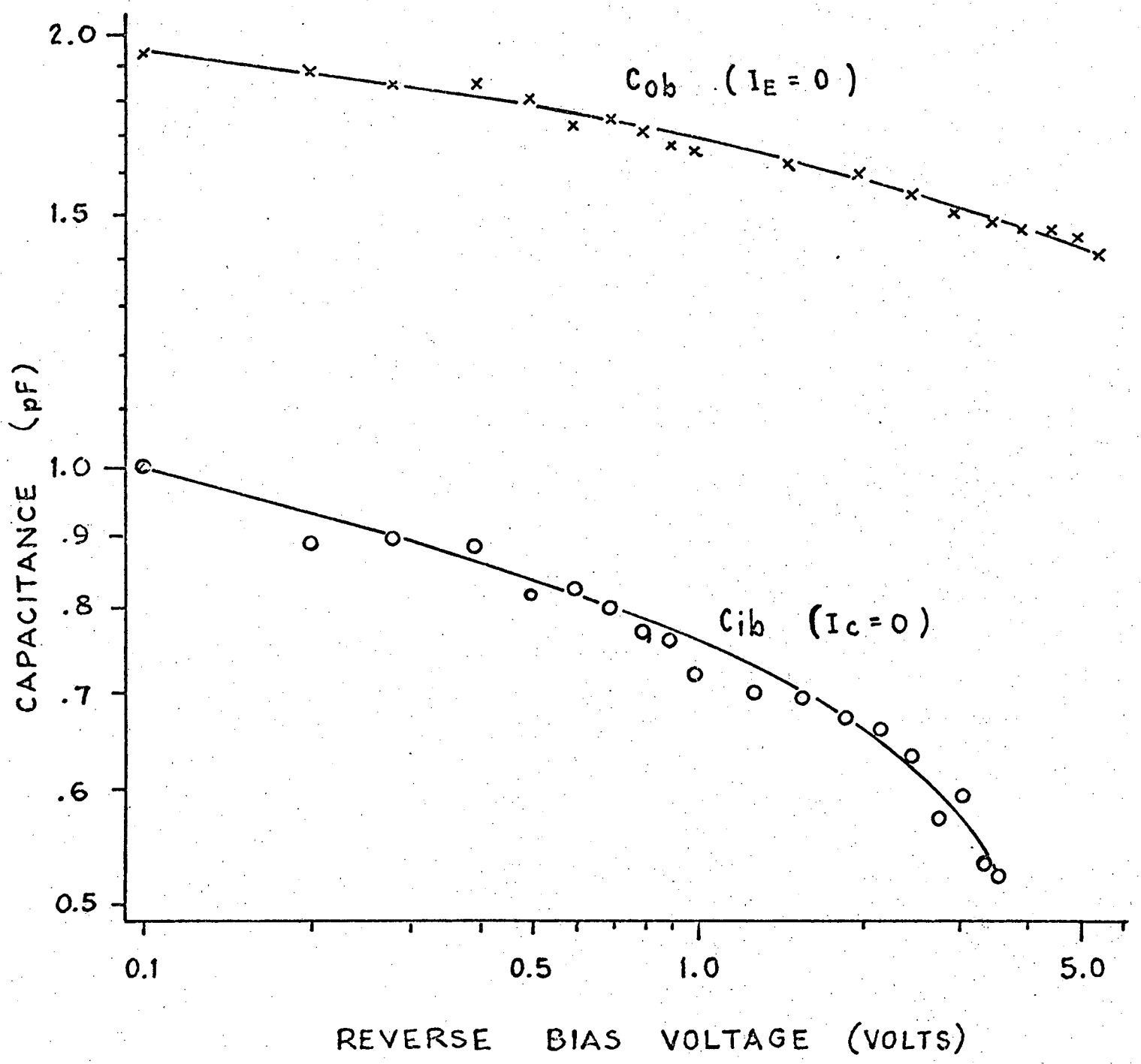


Fig. 4-26. Capacitances of 2N709.

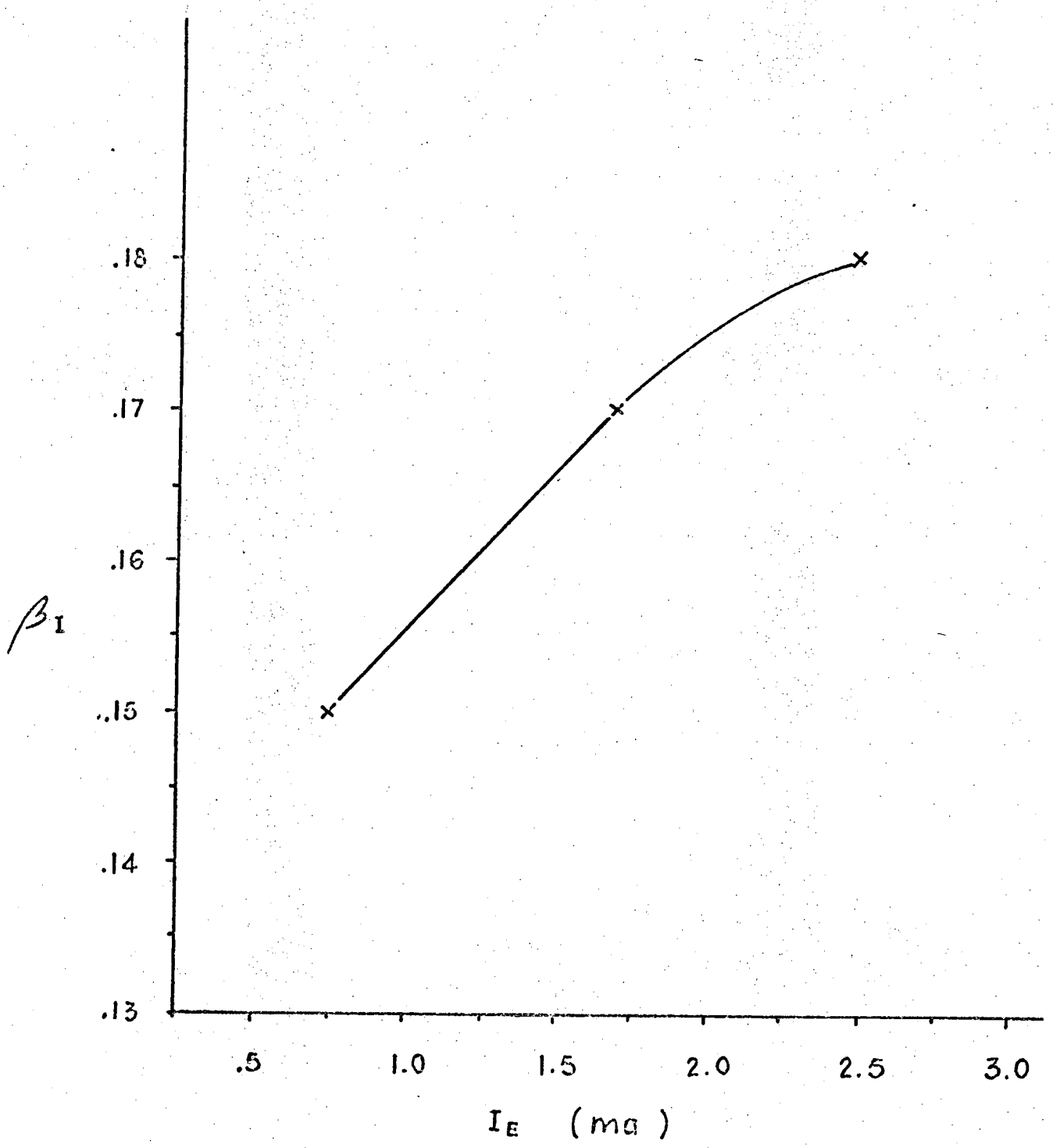


Fig. 4-28. β_I of 2N2369A.

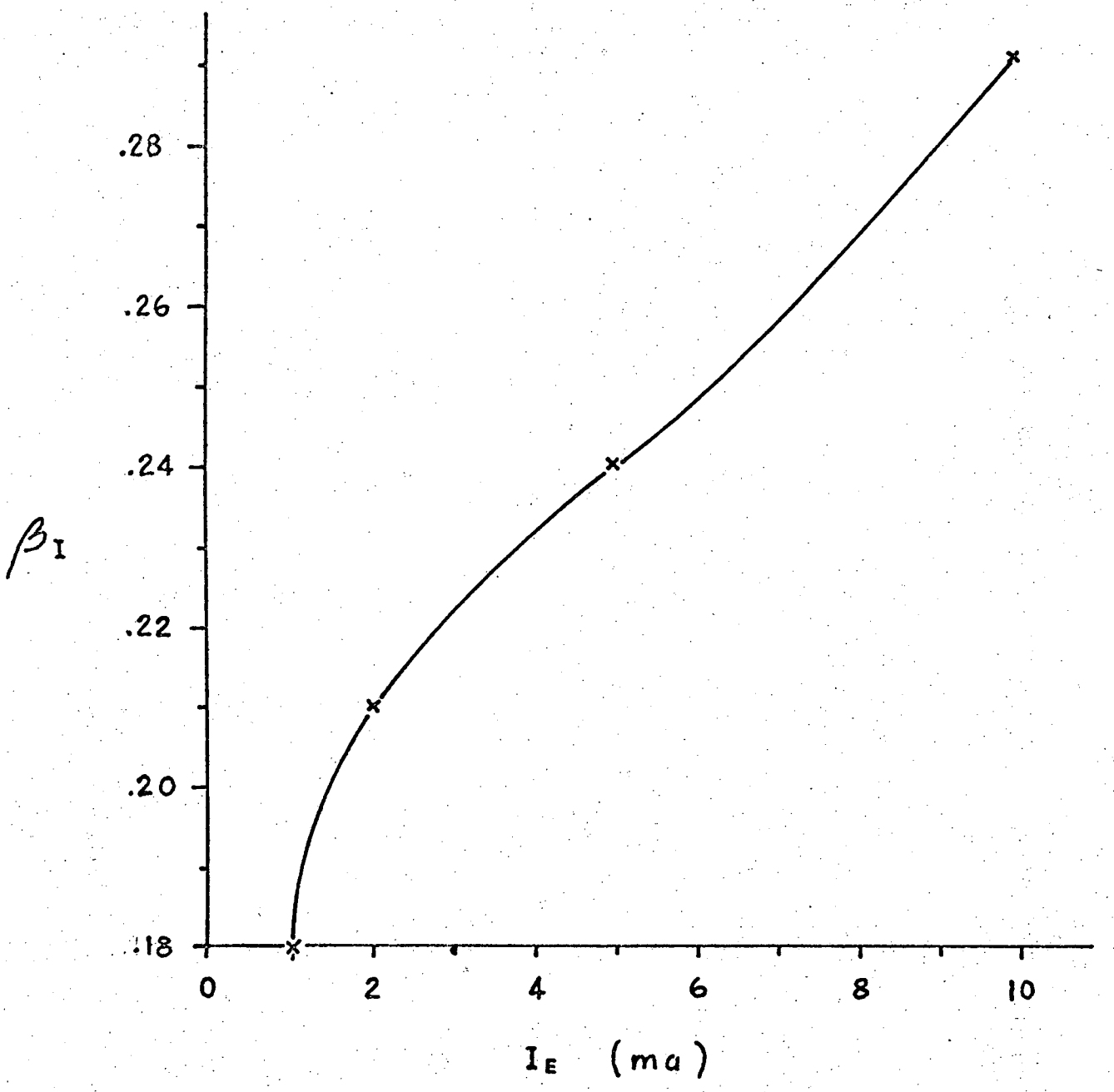


Fig. 4-29. B_I of 2N709.

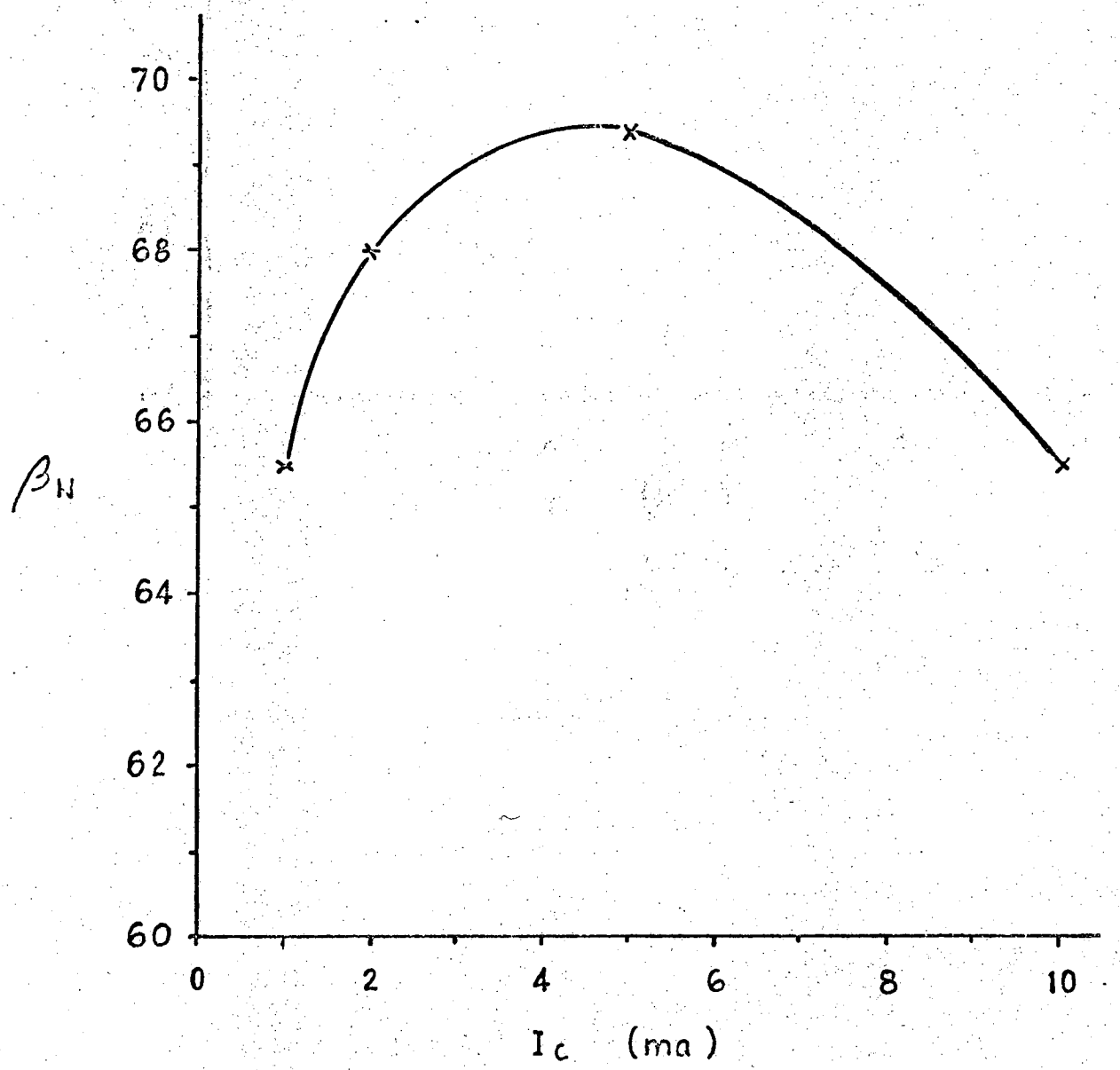


Fig. 4-30. B_N of 2N2369A.

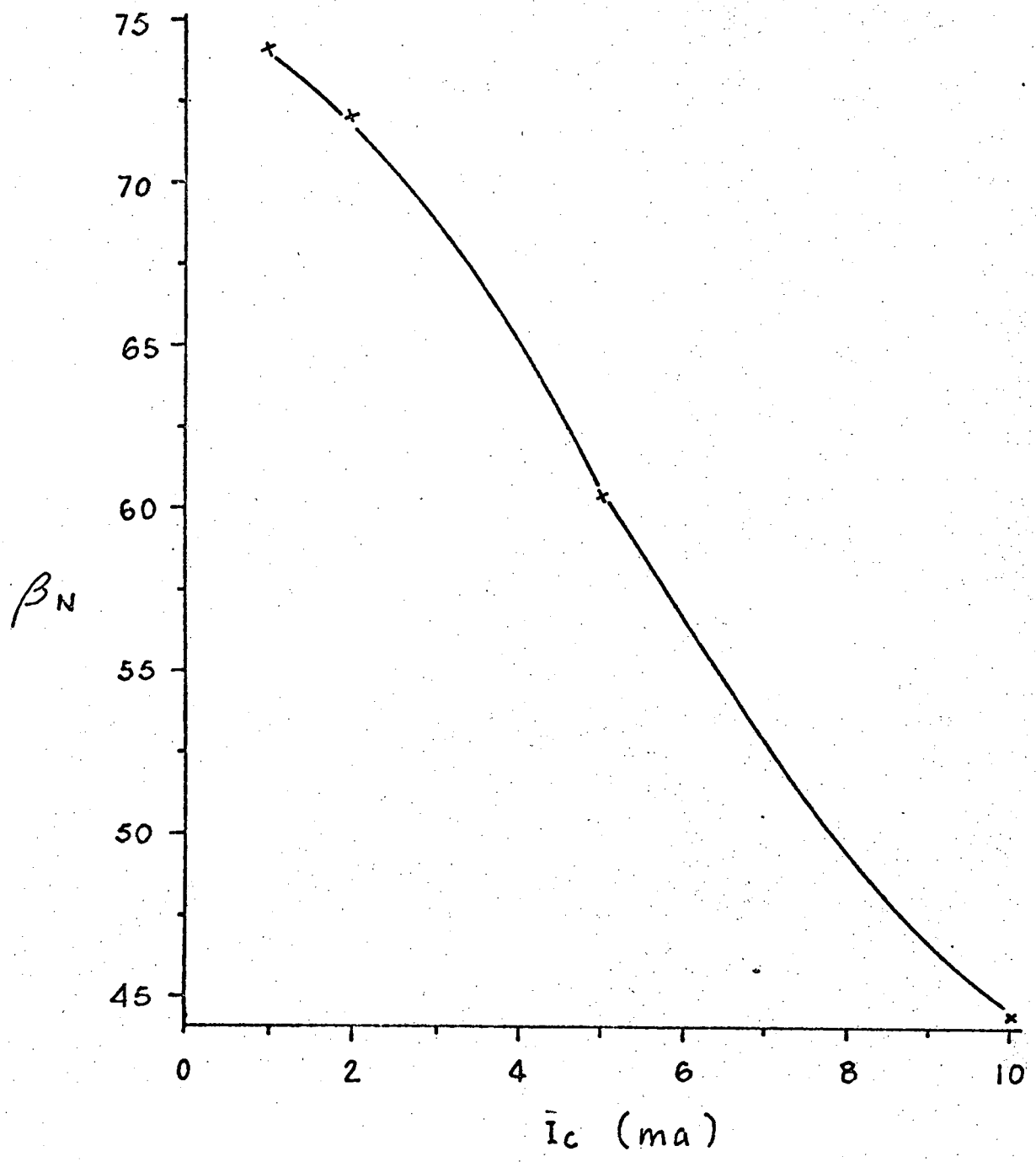


Fig. 4-31. B_N of 2N709.

B. DIODE PARAMETERS

Most of the diode parameters are similar to the transistor parameters and, therefore, identical procedures can be used.

R_S can be measured by reverse biasing the diode with a voltage V_R. Then the current which flows follows

$$I_R = \frac{V_R}{R_S}, \tag{4-31}$$

Knowing V_R and I_R, R_S is known. K can be obtained by the reverse recovery time measurement. The difference in recovery times between a zero biased and a forward biased gives the diffusion capacitance. Since

$$C_{Diff} = K\, i_D, \tag{4-32}$$

Knowing C_{Diff} and i_D, K is known.

C. TUNNEL DIODE PARAMETERS

Because of the instability of the tunnel diodes, device measurements can be extremely difficult. For instance, the junction capacitance can best be measured around the valley point V_v (Fig. 4-32). At other points, measurements are difficult to perform. For this reason, although the junction capacitance follows the equation

$$C_T = \frac{C_o}{(V + \phi)^n}, \tag{4-33}$$

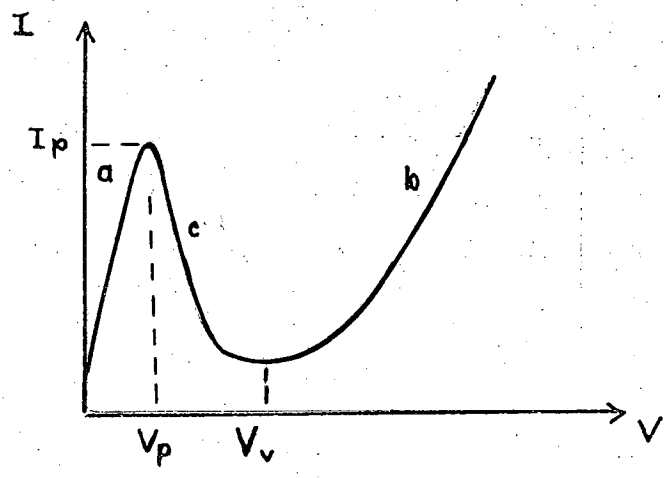


FIG. 4-32. I-V Characteristic of Tunnel Diode.

insufficient measurement forces one to model the junction capacitance as a constant and ignore the depletion capacitance.

The I-V Characteristic (Fig. 4-32) can be modeled by (see Fig. 3-15)

$$I = A_A V e^{-AV} + B_B\left(e^{B_1 V} - e^{-B_2 V}\right) + C_C\left(e^{CV} - 1\right). \qquad (4\text{-}34)$$

In order to extract the seven parameters from one equation (4-34), numerical techniques have to be used again. Ideally, the least-square method mentioned in detail for the transistor parameter measurements (Appendix B) can be used with no problem. However, in practice, unless the seven-dimensional solution space of the parameters are known, stability of the solution is hard to achieve.

To solve for the parameters in Eq. (4-34), the equation has to be broken into three regions of operation[21]:

(a) $V \leq V_p$,

$$I \approx A_A V e^{-AV}, \tag{4-35}$$

(b) $I > 2I_p$,

$$I \approx C_C e^{CV}, \tag{4-36}$$

(c) region between (a) and (b).

In region (a), plotting ln (I/V) vs. V will give a straight line with intercept ln A_A and slope -A. Similarly in region (b), plotting ln (I) vs. V will give ln C_C as intercept and C as slope. Knowing A_A, A, C_C, C, a difference curve g(V) can be constructed for region (c):

$$g(V) = I(V) - A_A V e^{-AV} - C_C e^{CV} = B_B\left(e^{B_1 V} - e^{-B_2 V}\right). \tag{4-37}$$

The B_B, B_1, B_2 can then be solved using the least-square fit method. The program used to solve B_B, B_1, and B_2 is shown in Appendix B.

D. JFET PARAMETERS

All the single-valued parameters of a JFET (see Table 4-1) can be measured in the identical fashion used for bipolar transistor parameter measurements (see part A of this chapter) and therefore will not be repeated here. The Θ_X and I_{SY} can be obtained from I_D - V_{SD} characteristic (Fig. 4-31).

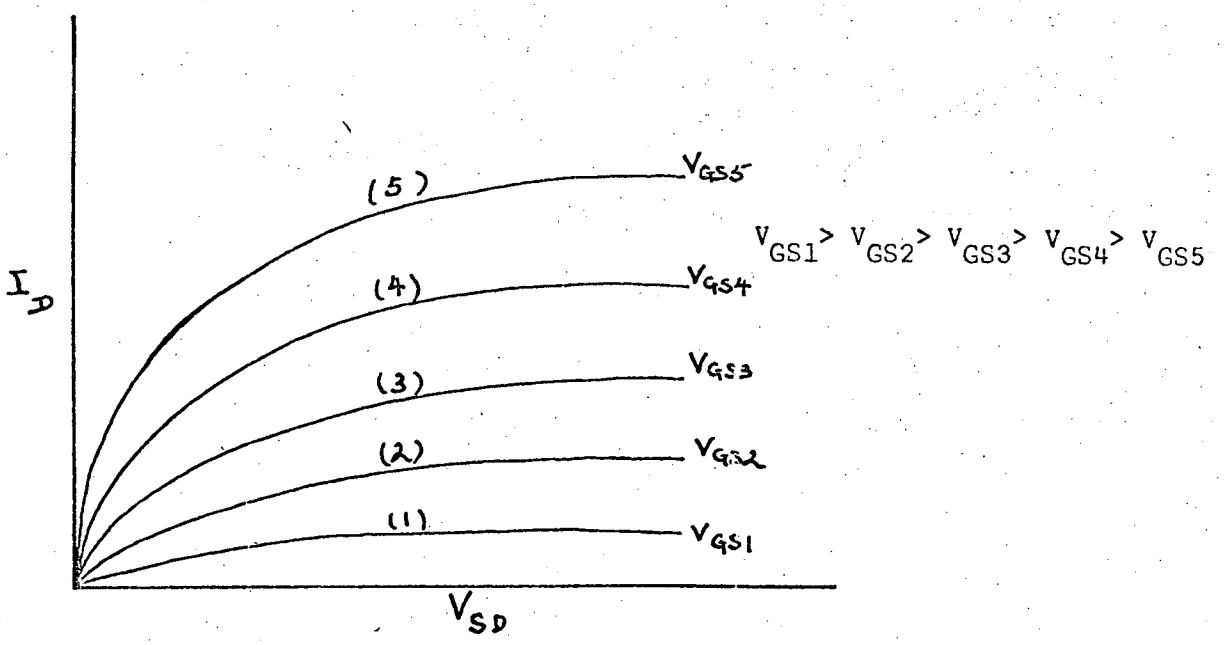


FIG. 4-33. Typical I_D -V_{SD} Characteristic of JFET.

For every V_{GS}, there is a distinct characteristic curve (e.g., for V_{GS1} it is curve 1). Associated with this curve is the equation

$$I_D = I_{SY} \left(1 - e^{-\Theta_X V_{SD}}\right). \tag{4-38}$$

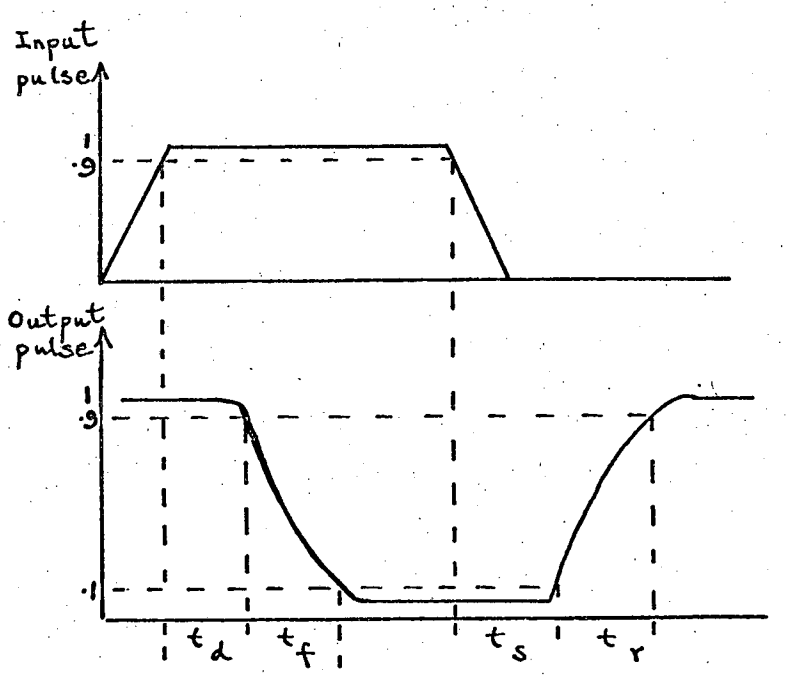
For large V_{SD},

$$I_D \approx I_{SY} , \tag{4-39}$$

Therefore, I_{SY} can be determined immediately for the V_{GS} of interest. Θ_X can be obtained from the slope of $\ln\ 1 - \frac{I_D}{I_{SY}}$ vs. V_{SD} curve. For a series of curves (Fig. 4-33), a series of I_{SY} and Θ_X can be obtained and tables of I_{SY} vs. V_{GS} as well as Θ_X vs. V_{GS} can be constructed.

CHAPTER 5. EXAMPLES AND CONCLUSIONS

In this chapter, the results of an inverter circuit, a monostable multivibrator circuit, an astable multivibrator circuit, and an amplifier circuit are presented. Comparisons between the experimental and the computer-predicted results are shown. The significance of the device parameters are further illustrated by examples of the inverter circuit and the amplifier circuit. Wherever applicable, the usual definitions of rise time, fall time, delay time, and storage time (see Fig. 5-1) are adopted in this chapter.



t_d = turn-on delay time,

t_f = fall time,

t_s = turn-off storage time,

t_r = rise time.

FIG. 5-1. The Definitions of Switching Times.

A. INVERTER CIRCUIT

The CIRCUS input statements of the inverter, Fig. 5-2, are shown in Fig. 5-3 . The comparison between the experimental and the computer-predicted switching times are tabulated in Table 5-1a. The output waveforms of the two responses are shown in Fig. 5-4. As seen from Fig. 5-4 , good agreements between the experimental and computer-predicted times are obtained.

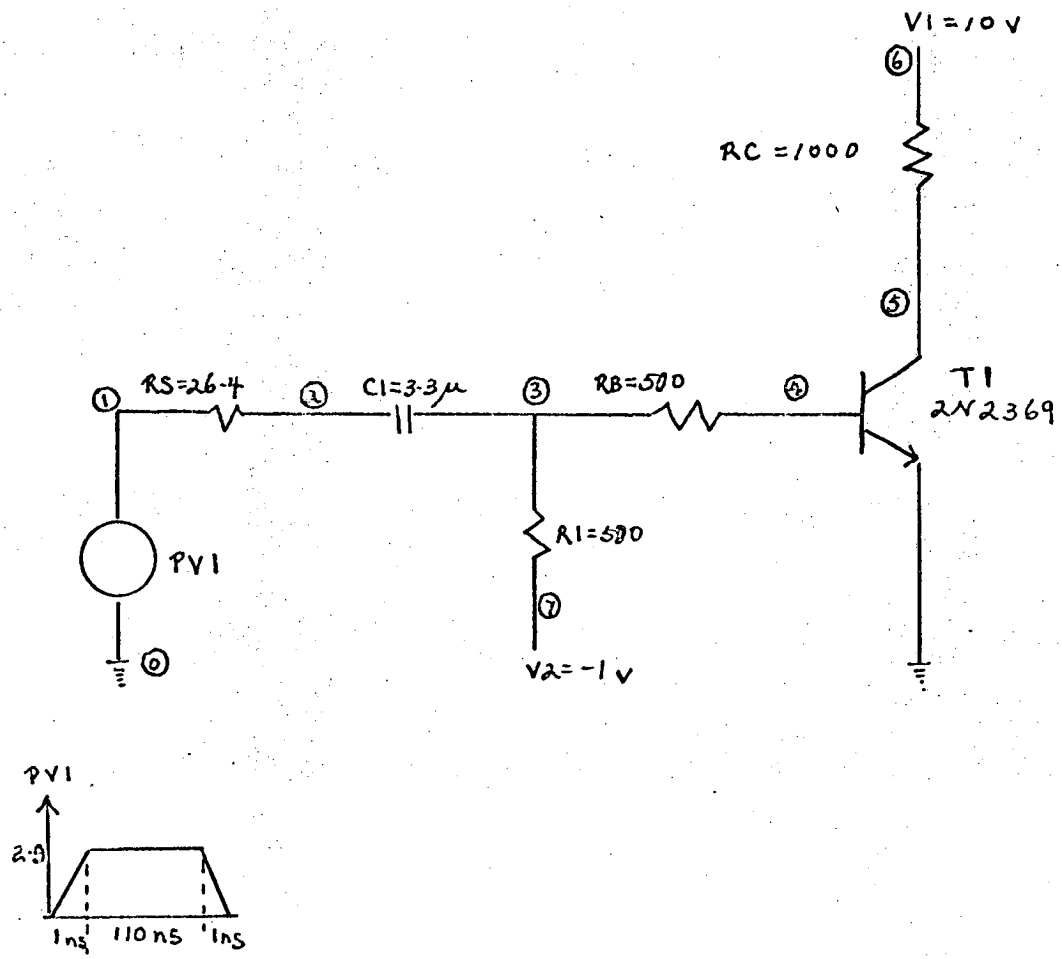


FIG. 5-2. Inverter Circuit.

```
"INVERTER CIRCUIT"
DEVICE PARAMETERS
TRANSISTOR,2N2369,NPN,RB,25.,RC,5.,RE,.66,A1,5.E-12,PHI1,.9,N1,.30,
A2,3.7E-12,PHI2,.9,N2,.22,IES,1.8E-14,THETAN,37.2,ICS,5.75E-14,
THETAI,34.5
BN,.001,.002,.005,.01,.02,.05,65.5,68.,69.4,65.5,27.4,27.8
BI, .00075, .0017, .0025, .15, .17, .18
TCN, .001, .002, .005, .01, 3.6E-10, 3.9E-10, 3.9E-10, 4.E-10
TCI, .001, .002, .005, 6.4E-8, 4.85E-8, 6.2E-8
END
RS,1,2,26.4
C1,2,3,3.3E-6
C1,3,7,500.
RB,3,4,500.
RC,5,6,1000.
V1,6,0,10.
V2,7,0,-1.
T1,4,5,0,2N2369,OFF
PV1,1,0,0.,2.9,0.,1.E-9,1.1E-7,1.E-9,2.E-7
INTERVALS, 1.E-9, 2.E-8, 1.E-8, 1.1E-7, 5.E-9, 1.6E-7, 1.E-8,2.E-7
PRINT,VN5,PV1,
PLOT,VN5
DIAGNOSTICS
EXECUTE
END OF JOB
```

FIG. 5-3. Input Statements of the Inverter Circuit.

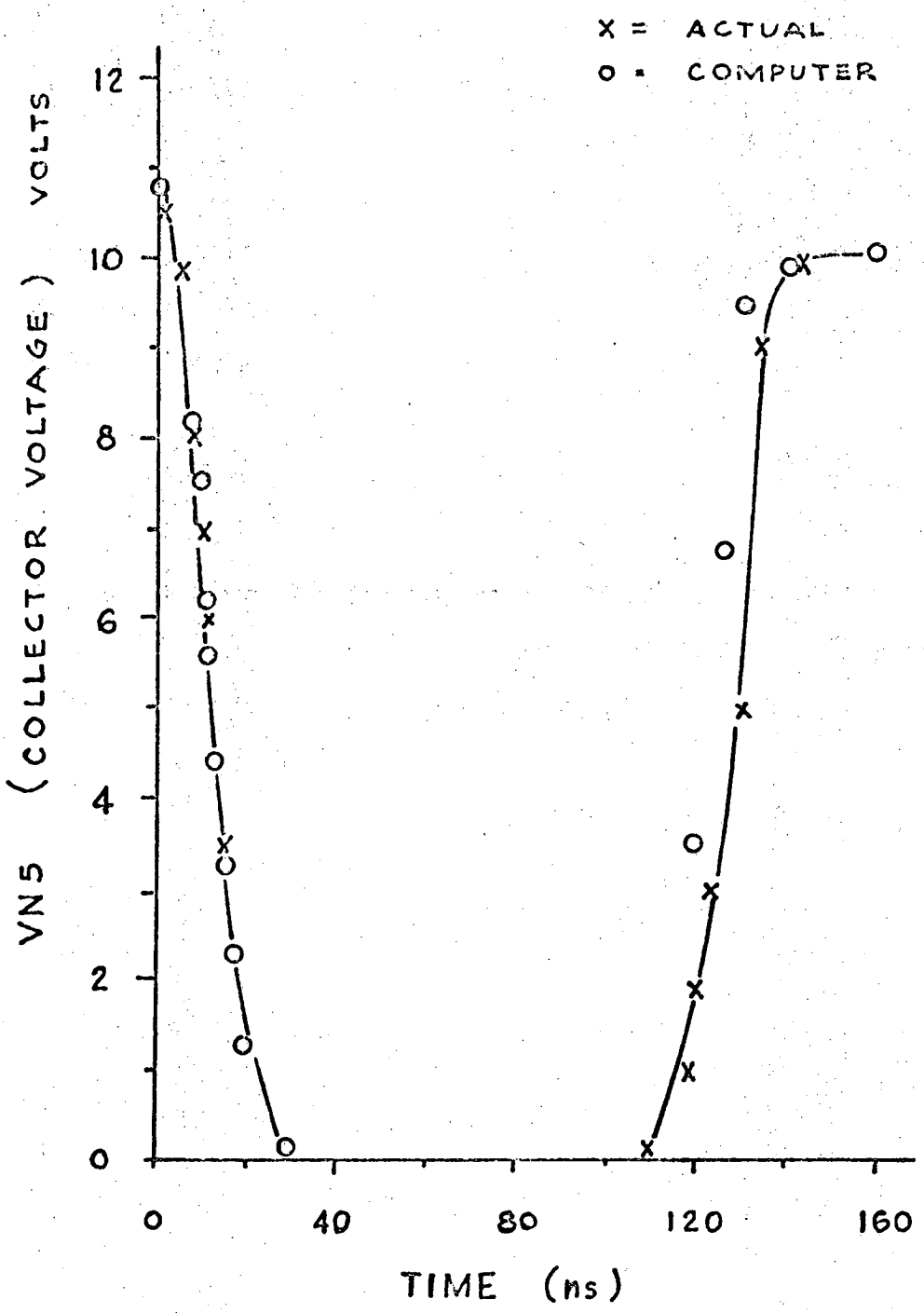


Fig.5-4. Inverter response.

	t_d,ns	t_f,ns	t_s,ns	t_r,ns
EXPERIMENTAL	6.3	12	≈ 0	19
COMPUTER-PREDICTED	6.6	14.9	≈ 0	14.9

TABLE 5-1a. Comparison between the Experimental and Computer Results of the Inverter.

The significance of the bipolar transistor parameters can best be illustrated by observing the effects of changing each parameter on the performance of the inverter circuit. Each transistor parameter (except the unimportant r_e and r_c) is changed by 10% and the corresponding percentage changes of the switching times are compared in Table 5-1b.

PARAMETER WHICH IS CHANGED BY +10%	% CHANGE			
	t_d	t_f	t_s	t_r
IES	1	- .2		4.6
ICS	1.3	≈ 0		5.3
BI	1.3	-22.9		5.5
BN	1.2	- .7		4.2
TCI	1.9	- 1.6	No Observable Change	5.4
TCN	1.3	- .7		8.5
THETAI	1.1	≈ 0		3.2
THETAN	-4.9	- 1.8		-11.3
N2	-1.1	- .5		- 5.0
N1	1.7	- .1		5.8
PHI1	- .4	- .1		3.7
PHI2	1.2	≈ 0		4.3
A2	5.8	≈ 0		20.1
A1	5.4	- .2		8.3
RB	1.4	- .2		6.0

Table 5-1b. Relative Change of the Switching Times of the Inverter when each Transistor Parameter is Changed by +10%.

B. EMITTER COUPLED ASTABLE MULTIVIBRATOR CIRCUIT

The input statements of the circuit are shown in Fig. 5-4.

```
"EMITTER COUPLED ASTABLE MULTIVIBRATOR"
DEVICE PARAMETERS
TRANSISTOR,2N2369,NPN,RB,25.,RC,5.,RE,.66,A1,5.E-12,
PHI1,.9,N1,.30,A2,3.7E-12,PHI2,.9,N2,.22,IES,1.8E-14,
THETAN,37.2,ICS,5.75E-14,THETAI,34.5
BN,.001,.002,.005,.01,.02,.05,65.5,68.,69.4,65.5,27.4,27.8
BI,.00075,.0017,.0025,.15,.17,.18
TCN,.001,.002,.005,.01,3.6E-10,3.9E-10,3.9E-10,4.E-10
TCI,.001,.002,.005,6.4E-8,4.85E-8,6.2E-8
END
RB2,1,0,20.
RB1,6,1,10.
RF,2,1,1000.
RC1,6,2,400.
RE1,3,0,600.
RC2,6,5,50.
RE2,4,0,600.
C1,4,3,5.E-10
T1,1,2,3,2N2369
T2,2,5,4,2N2369,OFF
V1,6,0,10.
INTERVALS,4.E-9,4.E-8,2.E-9,6.E-8,1.E-8,1.4E-7,2.E-9
1.6E-7,1.E-8,2.E-7
PRINT,VN2
PLOT,VN2
EXECUTE
END OF JOB
```

FIG. 5-4. Input Statements for the Astable Circuit.

The astable multivibrator circuit is shown in Fig. 5-5 and the responses are shown in Fig. 5-6 .

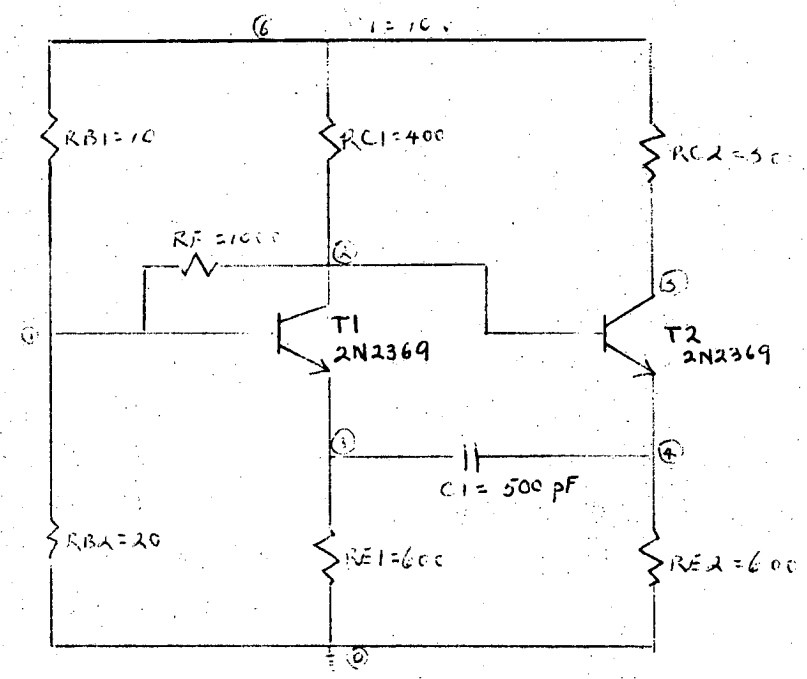


FIG. 5-5. Emitter-Coupled Astable Multivibrator.

Although the 50% pulse widths of the two waveforms (Fig. 5-6) are both approximately 25 nsec, there are some apparent discrepancies. This is because the experimental waveform is the steady-state waveform observed on the oscilloscope, whereas the computer solution is the third waveform of the transient solution. If the true steady-state solution from CIRCUS is compared with the experimental waveform, a smaller discrepancy should be expected.

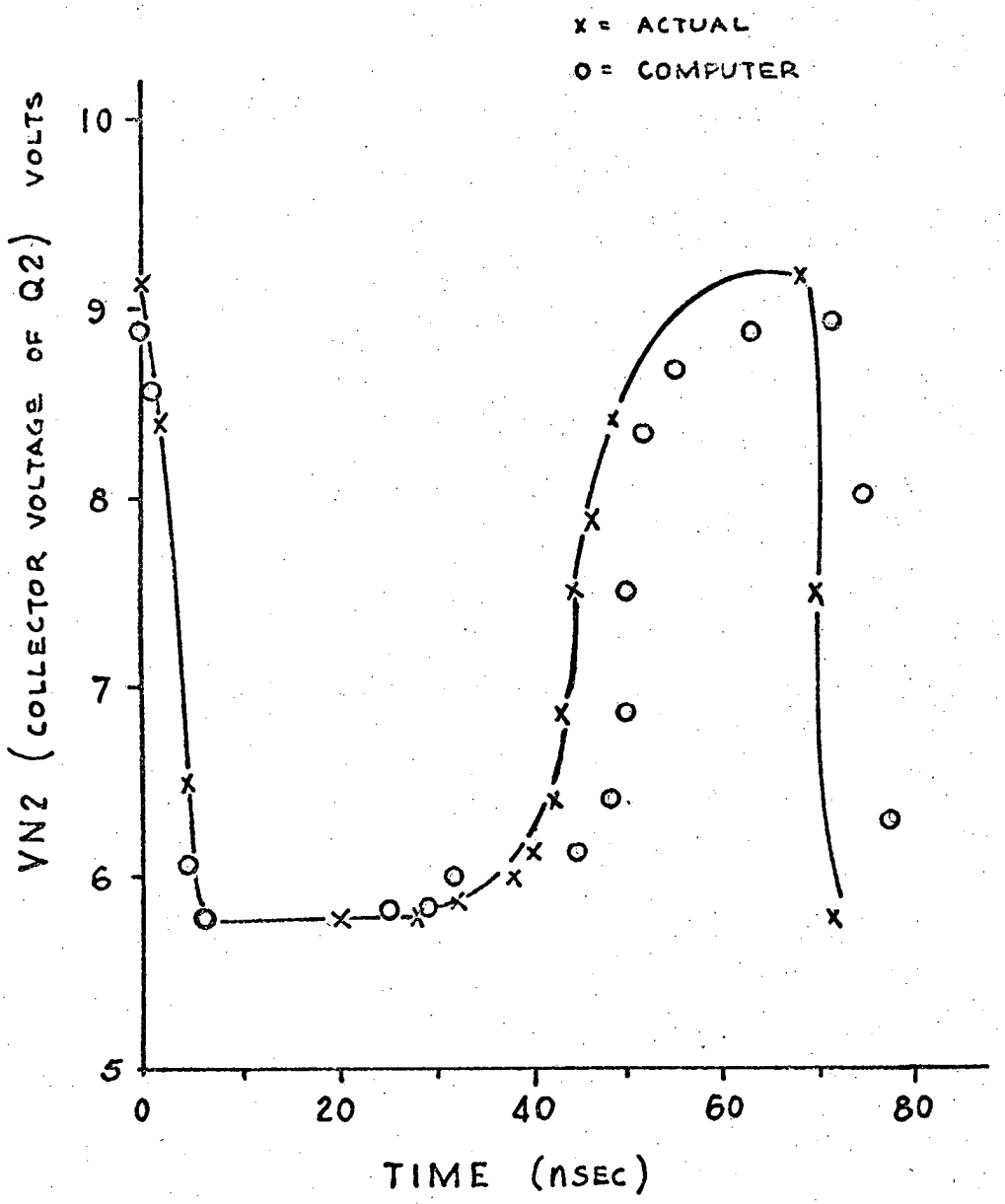


Fig 5-6. Emitter-coupled astable multivibrator response.

C. AMPLIFIER CIRCUIT

Though the device models in CIRCUS are nonlinear, they obviously apply equally well to linear circuits. Therefore, for completeness, the performance of an amplifier circuit (Fig. 5-7) is also checked. The experimental and computer-predicted results are tabulated in Table 5-2a. The response is shown in Fig. 5-8.

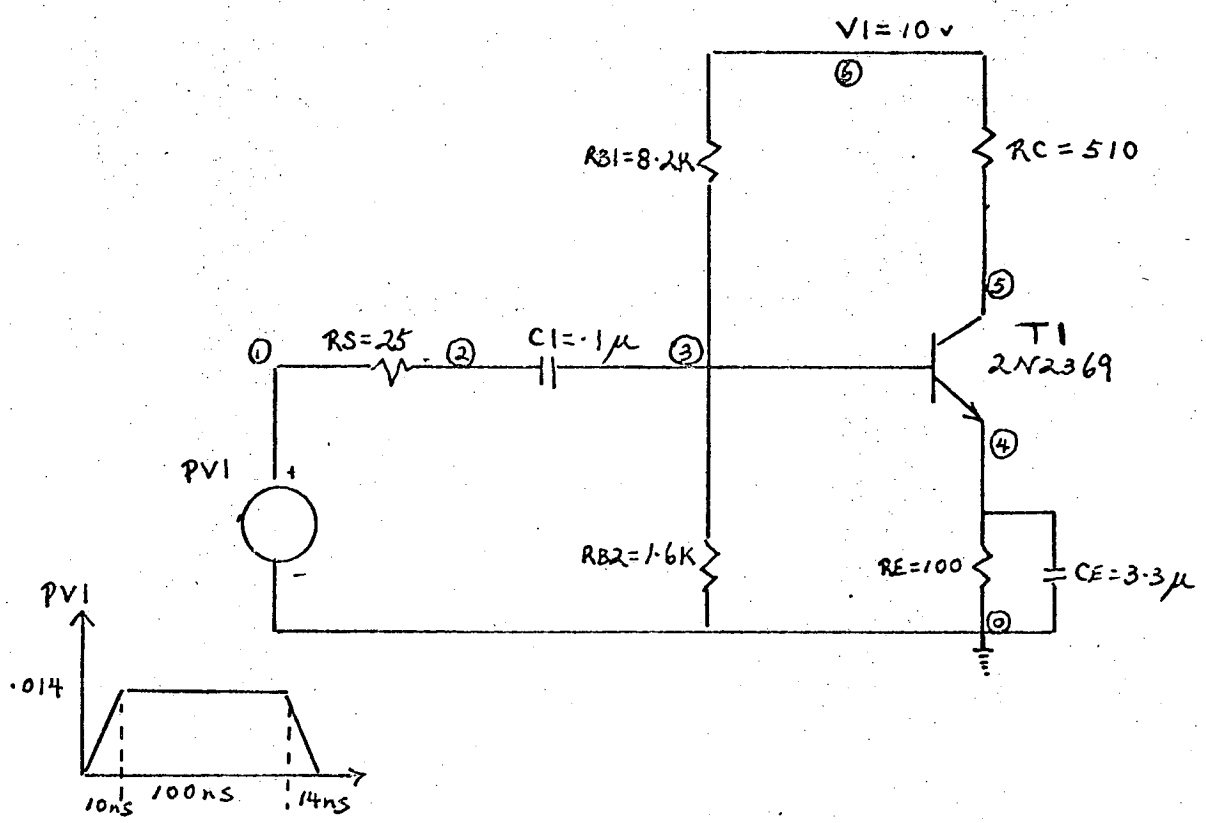


FIG. 5-7. Amplifier Circuit.

```
"AMPLIFIER"
TRANSISTOR,2N2369,NPN,RB,25.,RC,5.,RE,.66,A1,5.E-12,PHI1,.9,
N1,.30,A2,3.7E-12,PHI2,.9,N2,.22,IES,1.8E-14,THETAN,37.2,ICS,
5.75E-14,THETAI,34.5
BN,.001,.002,.005,.01,.02,.05,65.5,68.,69.4,65.5,27.4,27.8
BI,.00075,.0017,.0025,.15,.17,.18
TCN,.001,.002,.005,.01,3.6E-10,3.9E-10,3.9E-10,4.E-10
TCI,.001,.002,.005,6.4E-8,4.85E-8,6.2E-8
END
RS,1,2,25.
C1,2,3,1.E-7
RB2,3,0,1.6E 3
RB1,3,6,8.2E 3
RE,5,0,100.
CE,5,0,3.3E-6
RC,4,6,510.
V1,6,0,10.
PV1,1,0,0.,.014,0.,1.E-8,1.00E-7,1.4E-8,2.E-7
T1,3,4,5,2N2369
INTERVALS,2.E-9,8.E-9,5.E-9,4.E-8,1.E-8,1.E-7,2.E-9,1.3E-7,1.E-8,2.E-7
PLOT,VN4
PRINT,VN4,PV1,ICT1,IBT1
EXECUTE
END OF JOB .
```

FIG. 5-9. Input Statements for the Amplifier.

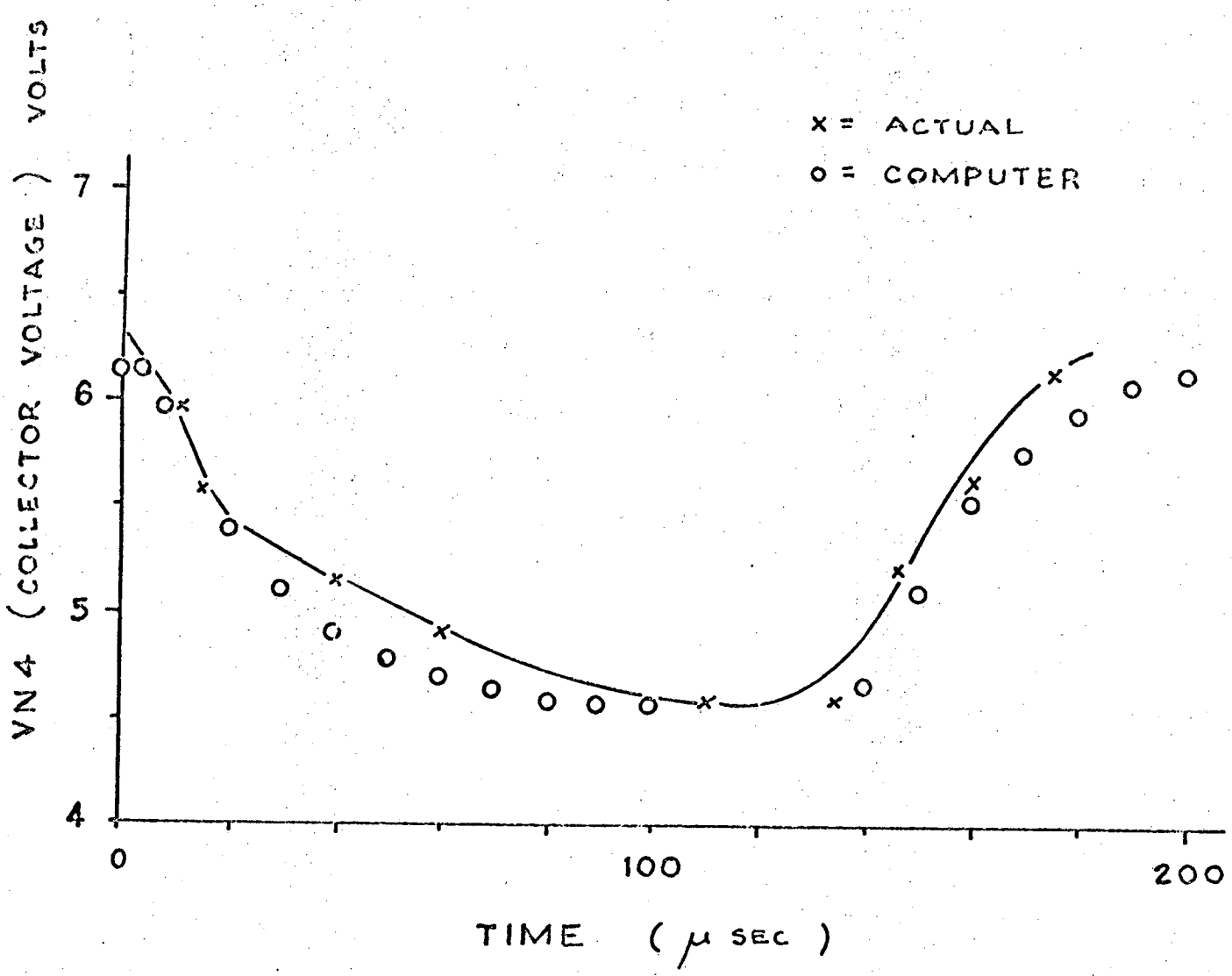


Fig 5-8. Amplifier response.

	Voltage Gain A_{VO}	dc Collector Current, mA	dc Collector Voltage, Volts	t_r,ns	t_f,ns
EXPERIMENTAL	≈ 110	7.4	6.33	38	44
COMPUTER-PREDICTED	110	7.48	6.18	46	45.5

TABLE 5-2 a. Comparison Between the Computer-Predicted and the Experimental Results of the Amplifier.

As seen from the table, CIRCUS prediction is good for both dc and transient response. The input statements for the amplifier circuit are shown in fig. 5-9.

Although the relative significance of the bipolar transistor parameters are compared with each other in the inverter circuit, it may be illuminating to examine the same effects on an amplifier circuit which is in the active region all the time. Each transistor parameter is changed again by 10% and the relative change of the output is compared in Table 5-2b.

PARAMETER WHICH IS CHANGED BY +10%	% CHANGE			
	VOLTAGE GAIN	dc COLLECTOR CURRENT	t_r	t_f
IES	.2	.1	- .1	-6.6
ICS	.2	- .2	- .1	-6.8
BI	.5	- .2	- .1	-6.8
BN	-1.8	1.5	2.2	-4.6
TCI	≈ 0	≈ 0	- .1	-6.8
TCN	≈ 0	≈ 0	2.1	-5.2
THETAN	-7.8	6.7	5.2	1.0
THETAI	↑	↑	- .1	-6.0
N2			-2.8	-9.1
N1	No	No	≈ 0	-6.7
PHI1	Observable	Observable	- .2	-6.9
PHI2	change	change	- .4	-7.1
A2	↓	↓	7.4	- .9
A1			≈ 0	-6.7
RB	-6.9	6.7	8.3	4.5

Table 5-2b. Relative Change of the Output of the Amplifier when each Transistor Parameter is Changed by +10%.

D. MONOSTABLE MULTIVIBRATOR CIRCUIT

The input statements for the monostable multivibrator circuit are shown in fig. 5-10.

```
"MONOSTABLE MULTIVIBRATOR"
DEVICE PARAMETERS
TRANSISTOR,2N709,NPN,RB,48.,RC,7.,RE,.8,A1,9.6E-13,N1,.38,
PHI1,.9,A2,1.9E-12,N2,.18,PHI2,.9,IES,3.55E-14,THETAN,33.5,ICS,
8.7E-14,THETAI,30.8
BN,.001,.002,.005,.01,.02,74.1,72.,60.3,44.3,21.8
BI,.0057,.0097,.02,.18,.21,.24
TCN,.001,.002,.005,.01,1.05E-10,9.88E-11,1.27E-10,1.42E-10
TCI,.001,.002,.005,.01,3.14E-8,3.04E-8,3.14E-8,2.85E-8
END
RF,1,4,9.1E3
RC1,2,5,1.E3
RB2,3,5,1.E4
RB,1,6,1.E4
RC2,4,5,1.E3
C1,2,3,3.3E-11
T1,1,2,0,2N709,OFF
T2,3,4,0,2N709
V1,5,0,10.
PV1,6,0,0.,3.,0.,1.E-9,1.E-7,1.E-9,4.E-7
INTERVALS,2.E-9,5.E-8,1.E-8,3.E-7,2.E-9,4.E-7
PRINT,VN4
PLOT,VN4
EXECUTE
END OF JOB
```

FIG. 5-10. Input Statements for the Monostable Multivibrator Circuit.

The monostable circuit is shown in Fig. 5-11.

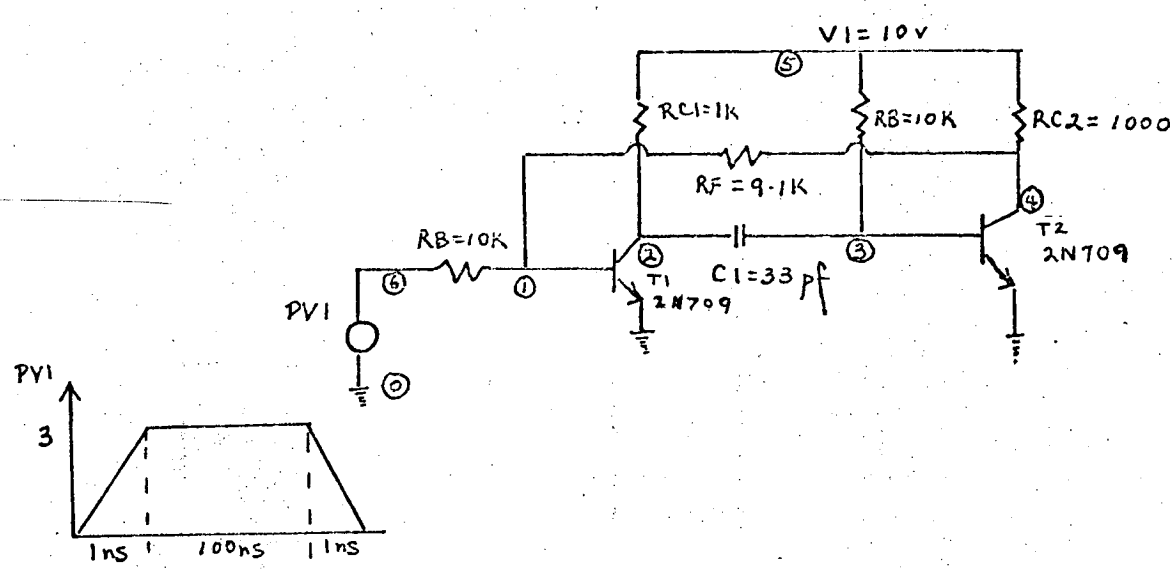


FIG. 5-11. Monostable Multivibrator Circuit.

The responses of the experimental and computer predicted are compared in Fig. 5-12 and Table 5-3.

	t_r,ns	t_f,ns	50% Pulse Width,ns
EXPERIMENTAL	20.5	16	240
COMPUTER-PREDICTED	14.8	19.2	241

TABLE 5-3. Comparison Between the Computer-Predicted and Experimental Results of the Monostable Multivibrator.

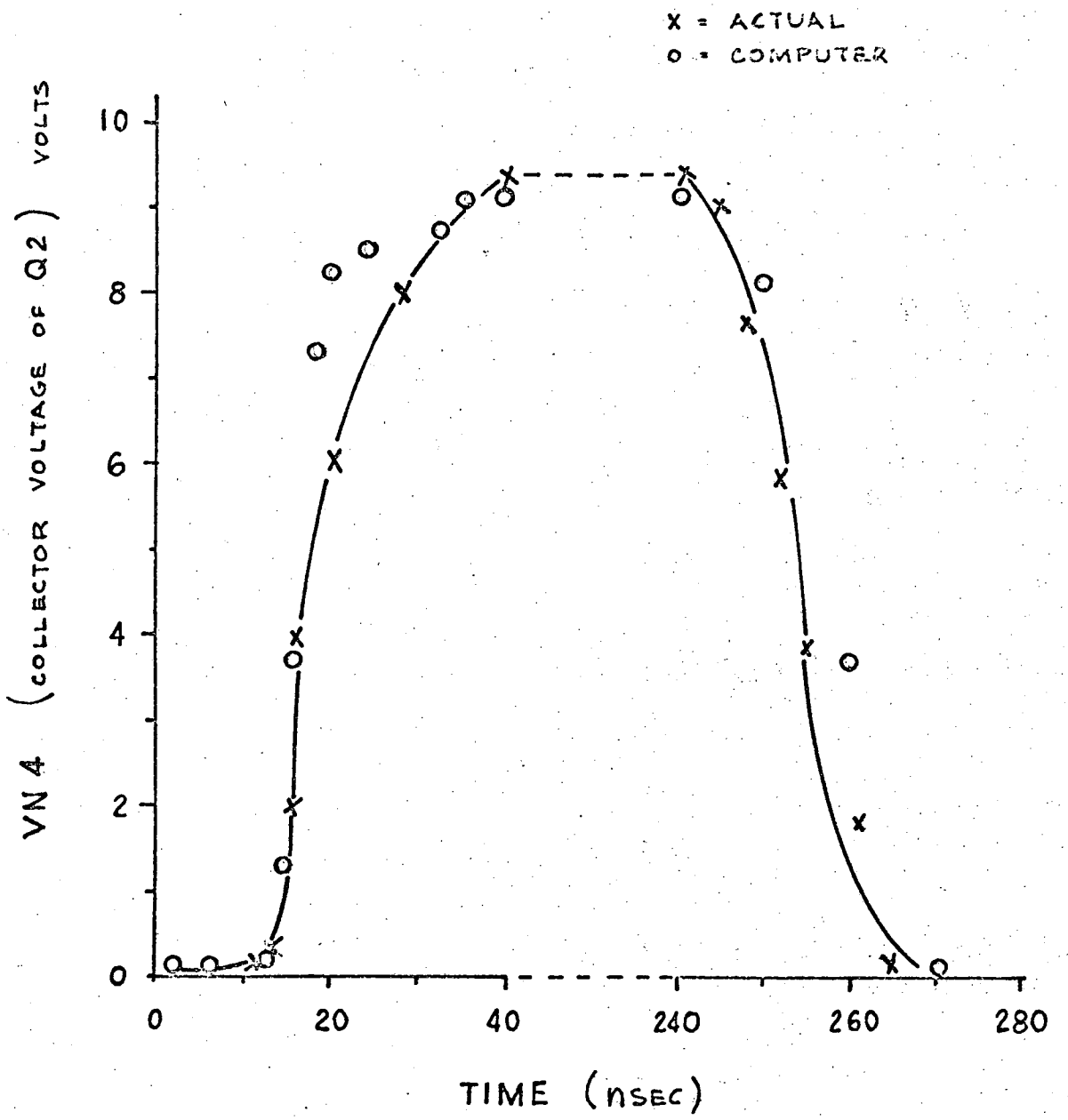


Fig 5-12. Monostable multivibrator response.

E. SUMMARY AND CONCLUSION

CIRCUS-computed results can generally be separated into two categories. The dc and steady-state results are in one category and the transient results are in the other (see Table 5-1b and 5-2b for the effects of transistor parameters on the dc and transient results).

The dc and steady-state results are usually in good agreement with the experimental results. This is because the important parameters for this category (for instance $B_N, B_I, I_{cs}, I_{es}, r_e, r_c, \theta_N, \theta_I$ for bipolar transistor) are easy to measure and therefore are relatively accurate.

The transient results are comparatively less accurate. The CIRCUS switching-time predictions are very often higher than their actual values. This is because the important parameters (for instance $T_{CN}, T_{CI}, a_1, a_2, \phi_1, \phi_2, n_1, n_2$ for bipolar transistor) are not only subject to probable measurement errors, but also they are either approximations of more accurate formulas or numerically solved quantities. For instance, the T_{CN} obtained from Eq. (4-15) is actually approximation of Eq. (4-14). Therefore T_{CN} is larger than what it should be. Furthermore, the a's, n's, and ϕ's in the capacitance parameters are obtained from numerical methods and may not be their true values. As seen from Table 5-1b, deviations of these parameters (especially the a_1, a_2, T_{CN}, T_{CI}) do cause some appreciable changes in the switching times.

In conclusion, CIRCUS is a very general and useful computer-aided design program for circuits with junction devices only. It does not require too much computer time (see Table 5-4). The models are good under most operations, and the accuracy of the simulation is mostly limited by the accuracy of device parameters. Its power lies in its nonlinear models, making CIRCUS most ideal to analyze circuits where nonlinearities are important. The flexibility of its format and the inclusion of the model library makes CIRCUS one of the easiest program to use.

	Inverter	Emitter-Coupled Astable Multivibrator	Amplfier	Monostable Multivibrator
COMPUTER CP TIME IN SECONDS	2	8	2	15

TABLE 5-4. COMPUTER TIME REQUIRED TO ANALYZE VARIOUS CIRCUITS DESCRIBED IN CHAPTER 5.

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FOOTNOTE AND REFERENCES

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1. F. H. Branin, Jr., DC and Transient Analysis of Network Using a Digital Computer, IRE International Conv. Rec. pt. 2, pp 236-256, 1962.

2. A. F. Malmberg, F. L. Cornwell, and F. N. Hofer, NET-1 Network Analysis Program, Report No. LA-3119, Los Alamos Scientific Laboratory, August 1964, 7090/94 version.

3. P. R. Bryant, The Explicity Form of Bashkow's A Matrix, IRE Transactions on Circuit Theory Vol. CT-9, pp. 303-306, Sept. 1962.

4. R. L. Wilson and W. A. Massena, An Extension of Bryant-Bashkow A Matrix, IEEE Transactions on Circuit Theory Vol. CT-12, pp. 120-122, March 1965.

5. D. A. Pope, An Exponential Method of Numerical Integration of Ordinary Differential Equations, Communications of ACM, Vol. 6 pp. 491-493, August 1963.

6. D. O. Pederson, Electronic Circuits, McGraw Hill, Inc., pp. 5-58, 1966.

7. P. L. Lee, A Large-Signal Transistor Model for Computer-Aided Analysis, U. of Calif., M.S. Thesis, 1968.

8. R. Beaufoy and J. J. Sparkes, The Junction Transistor as a Charge-Controlled Device, Automatic Telephone and Electric Company Journal Vol. 13, pp. 310-327, Oct. 1957.

9. J. J. Sparkes, A Study of Charge-Controlled Parameters, Proc. IRE Vol. 48, pp. 1696-1705, Oct. 1960.

10. J. J. Ebers and J. L. Moll, Large-Signal Behavior of Junction Transistors, Proc. IRE Vol. 42, pp. 1761-1772, Dec. 1954.

11. P. E. Gray, D. DeWitt, A. R. Boothroyd and J. F. Gibbons, Physical Electronics and Circuit Models of Transistors, SEEC Vol. 2, John Wiley and Sons, Inc. pp. 33-54, 78-96, 174-196, 1964.

12. M. H. Norwood and E. Shatz, Voltage Variable Capacitor Tuning - A review, Proc. IEEE Vol. 56, pp. 788-797, May 1968.

13. J. L. Wirth and S. C. Rogers, The Transient Response of Transistors and Diodes to Ionizing Radiation, IEEE Trans. on Nuclear Science Vol. 11, pp. 24-38, Nov. 1964.

14. R. D. Thornton, D. DeWitt, E. R. Chenette, and P. E. Gray, Characteristics and Limitations of Transistors, SEEC Vol. 4, John Wiley and Sons, Inc. pp. 1-62, 1966.

15. S. L. Miller, Avalanche Breakdown in Germanium, Physical Review Vol. 99, pp. 1234-1241, Aug. 1955.

16. A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc., pp. 243-259, 1967.

17. E. L. Steele, A UJT Model for use in Computer Simulation of Electronic Circuits, Autonetics Rept. X7-1935/501, August 1967.

18. D. A. Hodges, Synthesis and Realization of Counting Bistable Circuits, ERL Report No. 65-33, pp. 29-32, University of California, Berkeley, August 1965.

19. Data Book for Circuit Analysis and Design Tree, Vol. II, AFWL-TDR-64-60, July 1964.

20. R. H. Pennington, Introductory Computer Methods and Numerical Analysis, Macmillan Co., pp. 361-387, 1965.

21. Analytical Methods and Fundamental Parameters for Predicting Responses of Electronic Circuits to Transient Nuclear Radiation, with Application to Hardened Circuit Design, AFWL-TR-65-105, pp. 1-8, July 1965.

22. CIRCUS - A Digital Computer Program for Transient Analysis of Electronic Circuits, Vol. 1 - user's guide, Vol. 2 program guide, Harry Diamond Laboratories 346-1 and 346-2, January 1967.

APPENDIX A. CIRCUS USER'S MANUAL[21)]

This chapter describes the input format, the output options, and the program restrictions of CIRCUS. The various device models used in CIRCUS were described in Chapter 3. Examples together with experimental verification of the examples were presented in Chapter 6.

A. BERKELEY SYSTEM CONTROL CARDS

(i) For no plotting, no library models:

```
CIRCUS, 5, 100, 127000.427104, CHEN  (User's account, user's name)
REQUEST T. INPUT, LIB 7353, CIRCUS
COPY BF (T, CIRCUS)
UNLOAD (T)
RETURN (T)
REWIND (CIRCUS)
CIRCUS.
7-8-9
```

(ii) Using library tape, no plotting:

```
CIRCUS, 5, 100, 12700.427104, CHEN  (User's account, user's name)
REQUEST T. INPUT, LIB 7353, CIRCUS
COPY BF (T, CIRCUS)
UNLOAD (T)
RETURN (T)
REQUEST T1. INPUT, LIB 6222, MODLIB
COPY BF (T1, TAPE 11)
UNLOAD (T1)
RETURN (T1)
REWIND (CIRCUS)
REWIND (TAPE 11)
CIRCUS.
7-8-9
```

(iii) for SAVE option (see sec. F of this chapter):
In addition to either(i) or(ii), one more card:

REQUEST TAPE3. OUTPUT, SAVE
should be put in front of CIRCUS. card.

(iv) for RESTART option (see sec. F of this chapter)
In addition to either(i) or(ii), one more card:

REQUEST TAPE3. INPUT, SAVE
should be put in front of CIRCUS. card.

(v) for CRT plotting:
In addition to either(i) or(ii), the following:

EXIT.
DMP.
FIN.
SFL(50000)
CIRCUS.
should be inserted between the CIRCUS. card and the 7-8-9 card.

(vi) for CalComp plotting:
In addition to either(i) or(ii), the following:

EXIT.
DMP.
FIN.
SFL(50000)
COPY BR (CIRCUS,NULL)
should be inserted between the CIRCUS. card and the 7-8-9 card.

B. GENERAL CONVENTIONS

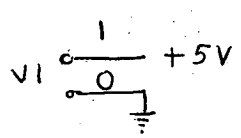
(i) Maximum Elements:

Resistors	200
Capacitors	200
Inductors	200
Mutual Inductances	200
Pulsed Current Sources	165
Sinusoidal Current Sources	0
Pulse Voltage Sources	75
Sinusoidal Voltage Sources	75
dc Voltage Sources	100
Transistors	40
Diodes	100
Zener Diodes	100
Tunnel Diodes	25
Four Region Devices	10
Field Effect Transistor	9
dc Current Sources	0

(ii) The nodes of the circuit are numbered consecutively from 0 to N with 0 assigned to ground. N should be less than 200.

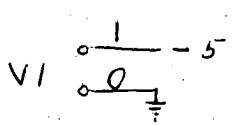
(iii) The higher node number is assumed to have higher voltage than the lower node number

e.g., (a) V1, 0, 1, 5. means



Following the voltage convention, node 1 is + 5 V with respect to node 0.

(b) V1, 0, 1, -5 means



In this case although the convention dictates node 1 to have a higher potential, a minus sign achieves the desired result of node 0 more positive than node 1.

(iv) Currents are assumed to flow from higher potential to lower potential.

(v) For PNP transistors, positive currents are flowing out of the transistors, and for NPN transistors, positive currents into the transistors. Diode currents are flowing from anode to cathode. FET currents are positive going into device and the voltage convention is $V_G > V_D > V_S$.

(vi) The input data can appear anywhere within the 80 columns of an IBM card. The exact column location is immaterial (i.e., format free).

(vii) The order of the input cards is also immaterial except the PHOTO CURRENT and CHANGE card should follow all the other cards.

(viii) The number format is very flexible. Shown below are some allowable and equivalent statements:

```
R1, 1, 2, 1230
R1, 1, 2, 1230.
R1, 1, 2, 1.23E3
```

However, no decimal point is allowed for the exponent.

(ix) The units used are second, ohm, farad, henry, volt, ampere. Scaling is usually unnecessary and, if the model library is used, is unadvisable.

(x) Each node must have a dc path to ground.

(xi) Zero element values are not allowed.

C. INPUT STATEMENTS

(i) Title Card. This card does not have to appear in the data. However, if it does, it must be the first card with the title enclosed in quotation marks (e.g. "TRIAL RUN").

(ii) Use Model Library:

If USE MODEL LIBRARY statement is used, no device parameters are needed for input data, but the system control cards must be those of A (ii). If the parameters for the particular device used in the problem do not appear on the model library, they must be provided accordingly (see J). Also, if several circuits are run as one job and if the first circuit does not use the model library, subsequent circuits cannot use the model library either.

D. ELEMENTS CARD

(i) Resistors, capacitors, inductors, and dc voltage sources are described by the format

Xname, m, n, v,

e.g., C1, 2, 3, 1.E-9

where X is R, L, C, or V,

name $\leq$ 3 alphameric characters,

m, n = element nodes,

v = element value.

for mutual inductance, the format is

K, L_1, L_2, u,

e.g., K12, L1, L2, .991

where K = coupling coefficient label,

name $\leq$ 3 alphameric characters,

L_1, L_2 = inductor labels,

u = coupling coefficient, always smaller than 1.

(ii) Transistors:

Tname, n_b, n_c, n_e, label,

e. g., T10, 1, 2, 0, TI3333

where n_b, n_c, n_e are base, collector, and emitter node number respectively,

name $\leq$ 2 alphameric characters,

label $\leq$ 6 alphameric characters.

(iii) Switching diodes, zener diodes, and tunnel diodes are described by the format

Yname, n_c, n_a, label,

e.g., D5, 3, 0, HP2300

ZD2, 2, 1, 1N2310

TD1, 3, 0, GE101

where Y = D for switching diodes.

= ZD for zener diodes

= TD for tunnel diodes,

name $\leq$ 3 alphameric characters,

n_c, n_a = cathode and anode node number respectively,

label $\leq$ 6 alphameric characters.

(iv) Four-Region Devices:

MTname, n_b, n_c, n_e, n_s, label,

e.g., MT1, 1, 2, 3, 4, ERL103

where MT = prefix for 4-region devices,

name $\leq$ 2 alphameric characters,

n_b, n_c, n_e, n_s = base, collector, emitter, and substrate node number respectively,

label $\leq$ 6 alphameric characters.

(v) JFET:

FT name, n_G, n_D, n_S, label,

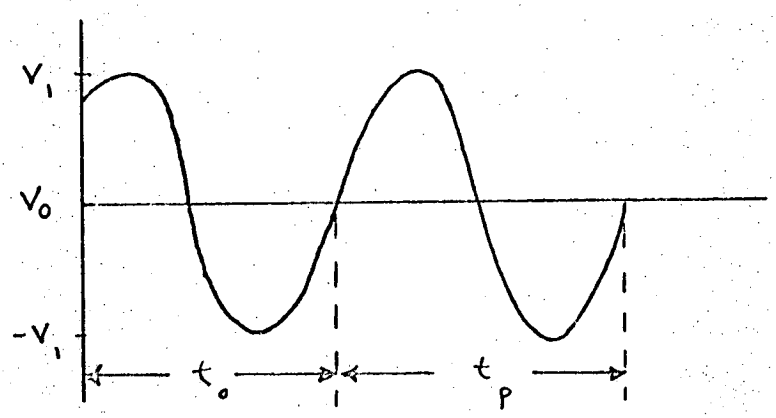
e.g., FT 1, 1, 2, 3, 3N1304

where name = 1 alphameric character,

n_G, n_D, n_S are gate, drain, source node number respectively,

label $\leq$ 6 alphameric characters.

(vi) Sinusoidal Voltage Sources:



SV name, n_1, n_2, V_0, V_1, t_o, t_p,

e.g., SV1, 3, 4, 0., 5., 0., 1.E-6

where name $\leq$ 3 alphameric characters,

n_1, n_2 = node numbers,

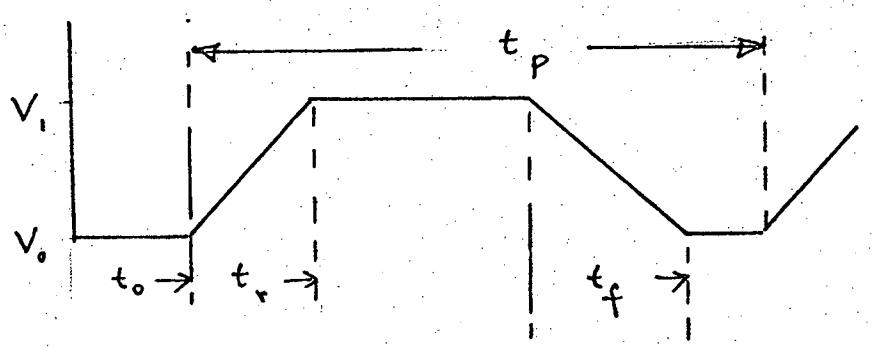
V_0 = average voltage,

V_1 = amplitude,

t_o = delay in seconds,

t_p = period in seconds.

(vii) Pulsed Sources:



PV name, n_1, n_2, V_0, V_1, t_o, t_r, t_d, t_f, t_p.

or PJ name, n_1, n_2, I_0, I_1, t_o, t_r, t_d, t_f, t_p,

e.g., PJ1, 3, 4, 0., 5.E-3, 0., 0., 1.E-9, 0., 1.E-7

where PV = voltage prefix,
PJ = current prefix,
n_1, n_2 = node numbers,
V_1, V_0 = voltage levels,
I_1, I_0 = current levels,
t_o = delay time,
t_r = rise time,
t_d = duration of pulse,
t_f = fall time,
t_p = period of pulse.

With appropriate t_r, t_d, t_f, triangular, rectangular, etc., waves can be obtained.

E. OUTPUT STATEMENTS

Any variables in Table A-1 can be printed and plotted.

TABLE A-1.

Variable	Description
(i) Linear elements:	
Resistor voltage	VR name
Resistor Current	IR name
Resistor power dissipation	PR name
Capacitor voltage	VC name
Capacitor current	IC name
Inductor voltage	VL name
Inductor current	IL name
Pulsed voltage	PV name
Sine-wave voltage	SV name
Pulsed current	PJ name
Voltage across current source	VPJ name
(ii) Transistor:	
Base-collector voltage	VCT name
Base-emitter voltage	VET name
Collector current	ICT name
Emitter current	IET name
Base current	IBT name
Collector-base capacitor current	JCT name
Emitter-base capacitor current	JET name
Collector-base dependent generator current	SCT name
Emitter-base dependent generator current	SET name
Power dissipated in transistor	PT name

Variable	Description
(iii) Diodes and Zener Diodes:	
Junction voltage	VD name
Junction current	ID name
Junction capacity current	JD name
Junction generator current	SD name
Power dissipated in diode	PD name
(iv) Tunnel Diodes:	
Junction voltage	VTD name
current	ITD name
(v) 4-Layer Devices:	
Base current	IBMT name
Collector current	ICMT name
Emitter current	IEMT name
Substrate current	ISMT name
Base-emitter voltage	VEMT name
Base-collector voltage	VCMT name
Collector-substrate voltage	VSMT name
Base-emitter capacitor current	JEMT name
Base-collector capacitor current	JCMT name
Collector-substrate capacitor current	JSMT name
Emitter junction generator current	SEMT name
Collector junction generator current	SCMT name
Substrate junction generator current	SSMT name

Variable	Description
(vi) JFET:	
Gate current	IGFT name
Source current	ISFT name
Drain current	IDFT name
Gate-source voltage	VSFT name
Gate-drain voltage	VDFT name
Gate-source capacitor current	JSFT name
Gate-drain capacitor current	JDFT name
Gate-source junction generator current	SSFT name
Source-drain channel current	SCFT name
FET power dissipation	PFT name
(vii) General Purpose:	
Node voltage	VN node no.
Difference or sum of two node voltages	D $n_1 \pm n_2$
Any variable minus its initial value	*variable name
Integration interval	DT

Statements:

(a) Print Statement:

This statement must appear in every circuit run. Its format is: PRINT, $name_1$, ... $name_n$,

where $name_i$ = any of those in Table A-1,

e.g., PRINT, VN3, IBT2, PT1, IRC, SD1

(b) Plot Statement:

Any parameter(s) in the PRINT statement can be plotted on a graph if the following card is provided: PLOT, $name_1$,..... $name_m$,

where $name_i$ = any of those in Table A-1,

e.g., PLOT, VN3, IRC.

(c) Monitoring maximum ratings:

Any parameter(s) appearing in the PRINT statement can be closely watched so that its value does not exceed the specified maximum. Then during the output printing, an asterisk will be placed beside those values in excess of the maximum.

MAXIMUM RATINGS, $name_1$, max $value_1$, ... $name_i$, max $value_i$,

where $name_i$ = any of those in Table A-1,

e.g., MAXIMUM RATINGS, PT1, .3, 1BT2, 1.E-2.

(d) Intervals Statement:

INTERVALS, Δt_1, t, ... Δt_i, t_i,

where Δt_i = print interval during period i,

t_i = time at the end of period i,

e.g., INTERVALS, 1.E-9, 1.5E-8, 5.E-7, 6.E-6.

(e) END Statement:

If the electronic device parameters are entered in as data, END tells the program that all the parameters have been entered in. In a run where several circuits are submitted, END tells the program that there are more circuits following to be executed.

(f) EXECUTE Statement:

EXECUTE signals the beginning of execution.

(g) **Circuit Parameter Variations:**

Except for the ohmic resistances of junction devices, all parameters can be varied one at a time or all at once. A typical input configuration might look like

(normal circuit input)

EXECUTE

(parameter changes)

EXECUTE

(more changes)

EXECUTE

END OF JOB

Between the EXECUTE cards, the following can be changed:

(i) Any fixed component value

*X name, V:

where * = parameter change prefix,

X = R, L, C or V,

V = new value,

e.g., *R3, 1.2E3.

(ii) Any pulsed and sinusoidal sources:

*PV name, V_0, V_1, t_o, t_r, t_d, t_f, t_p,

*PJ name, J_0, J_1, t_o, t_r, t_d, t_f, t_p,

*SV name, V_0, V_1, t_o, t_p

(see D(vi) and (vii) for the meanings of the symbols),

e.g., *SV1, 0., 2.3, 0., 1.E-7 .

(iii) To change the coupling coefficient, photocurrent, peak rate, title, or intervals, the user simply supplies an appropriate new card.

(iv) Fixed value device parameter changes:

CHANGE, label, p_1, $v(p_1)$, ..., p_n, $v(p_n)$,

and for parameter tables,

CHANGE, label t, values,

where label = model number,

p_i = fixed-value parameter name,

$v(p_i)$ = value of p_i,

t = table parameter name,

e.g., CHANGE, 2N2368, 1ES, 1.E-16, N2, .3

CHANGE, 2N2368, BN, .001, .002, 50., 70.

If the model library is used, any parameter(s) of the device of interest can be altered temporarily during the run by supplying CHANGE card(s) at the end of the data (i.e., before the EXECUTE card).

F. SAVE AND RESTART OPTION

Either for post-run recovery when time limit is exceeded or because the user desires the analysis to be stopped at one particular time instant, the results of analysis up to that point can be saved on a magnetic tape by the command

SAVE .

In a separate run, the analysis can be resumed with the saved tape mounted by the command

RESTART ,

followed by new INTERVALS card,

e.g., if the program was stopped at 1μs instant, the response after 1μs and up to 6μs can be obtained by the following cards in a separate run:

```
RESTART
"RESTART RUN"
INTERVALS, 1.E-7, 6.E-6
```

Only title and INTERVALS card are allowed for a RESTART execution.

G. HOLD FINAL CONDITIONS OPTION

If the user wants to change certain components of the circuit at a particular time during the analysis, he should use HOLD FINAL CONDITIONS instead of RESTART. Right after the changes, the analysis will continue with a new INTERVALS and EXECUTE card,

e.g., (circuit and intervals description)

HOLD FINAL CONDITION
EXECUTE
(changes and a new INTERVALS CARD)
EXECUTE
END OF JOB .

H. DIAGNOSTICS

The [Z] and [S] (see chapter 2) matrix plus the initial conditions of the circuit can be obtained by this card.

I. FINISH CARD

END OF JOB.

J. DEVICE PARAMETERS AND PHOTOCURRENT

(i) Device parameters format:
If the parameters of a device are not on the MODEL LIBRARY, they must be provided (see Table 4-1 for the number of parameters required for each device).

(a) Transistor

$$C_{be} = \frac{a_1}{(\phi_1 + V_{be})^{n_1}} + \Theta_N T_{CN} e^{\Theta_N V_{be}},$$

$$C_{bc} = \frac{a_2}{(\phi_2 + V_{bc})^{n_2}} + \Theta_I T_{CI} e^{\Theta_I V_{bc}},$$

$$I_{be} = (1 + \frac{1}{\beta_N}) I_{es}\left(e^{\Theta_N V_{be}} - 1\right) - I_{cs}\left(e^{\Theta_I V_{bc}} - 1\right),$$

$$I_{bc} = (1 + \frac{1}{\beta_I}) I_{cs}\left(e^{\Theta_I V_{bc}} - 1\right) - I_{es}\left(e^{\Theta_N V_{be}} - 1\right),$$

$$\beta_N = f_1 (I_N),$$

$$\beta_I = f_2 (I_I),$$

$$T_{CN} = f_3 (I_N),$$

$$T_{CI} = f_4 (I_I).$$

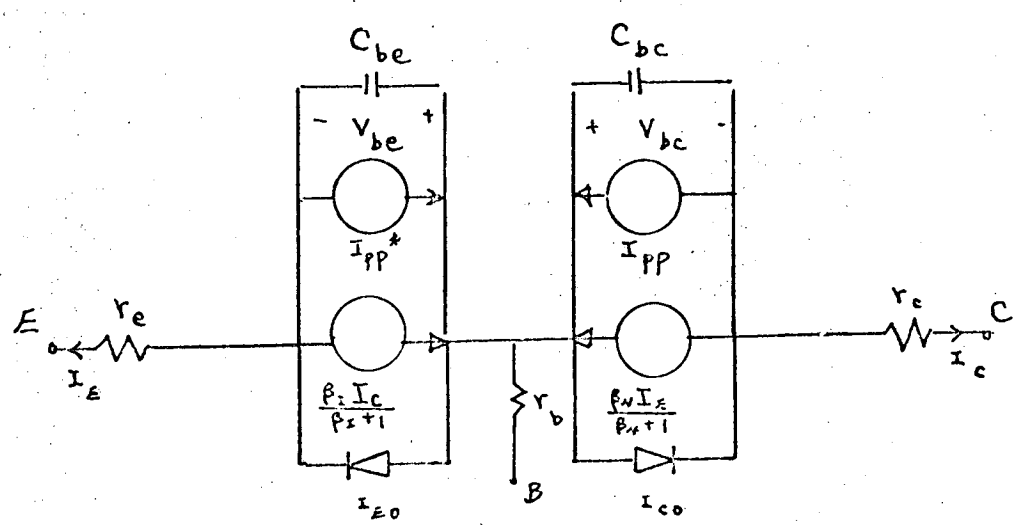


FIG. A-1. NPN Transistor.

The format is:

DEVICE PARAMETERS

TRANSISTOR, label, type, p_i, $v(p_i)$, ... p_n, $v(p_n)$,

table value, i_1, ... i_n, y_1, ... y_n,

⋮

END

where label = model number ≤ 6 alphameric characters,

type = NPN or PNP,

p_i = name of single-valued parameter,

$v(p_i)$ = value of parameter,

table label = any of BN, BI, TCN, TCI.

Single-valued parameters

Mathematical Symbol (Fig. A-1)	Input Symbol
r_b	RB
r_c	RC
r_e	RE
a_1	A_1
ϕ_1	PHI1
n_1	N1

Mathematical Symbol (fig. A-1)	Input Symbol
Θ_N	THETAN
a_2	A2
ϕ_2	PHI2
n_2	N2
Θ_I	THETAI
I_{es}	IES
I_{cs}	ICS

Table parameters: BN, BI, TCN, TCI - all functions of current;

e.g., DEVICE PARAMETERS
TRANSISTOR, 2N2368, NPN, RB, 62., RC, 20, RE, .01,
A1, 4.9E-12, PHI1, 1, N1, .29, A2, 5.E-12,
PHI2, 1, N2, .23, IES, 5.E-16, ICS, 2.9E-14,
THETAN, 39.6, THETAI, 32.2
BN, .001, 30
BI, .001, .05
TCN, .001, 1.E-7
TCI, .001, 1.E-7

A word of caution should be given here: Whenever a table is used for the device parameter, it must be arranged in ascending order with respect to the variable.

(b) Diode and Zener Diode

$$C_D = \frac{a}{(\phi + V_D)^n} + K_D I_S e^{\Theta V_D},$$

$$I_D = I_S\left(e^{\Theta V_D} - 1\right);$$

for zener diode $I_R = \dfrac{I_S}{\left(1 - \dfrac{V}{BV}\right)^m}$.

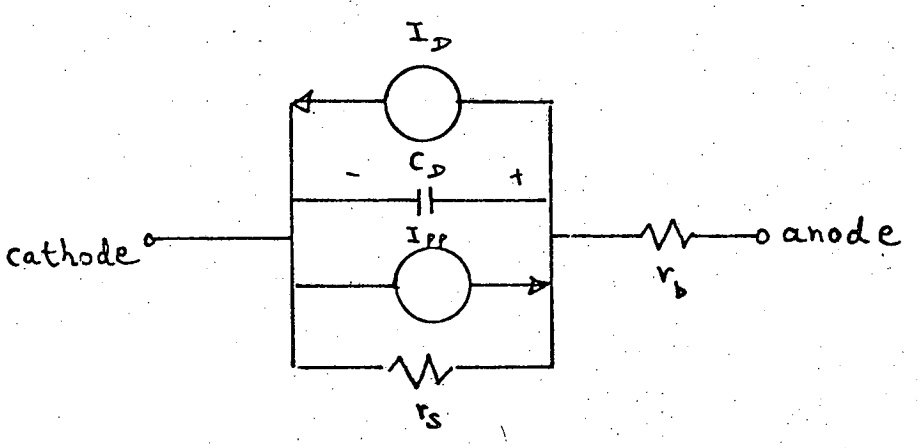


FIG. A-2. Diode and Zener Diode Model.

The format is

DIODE, label, p_i, $v(p_i)$, ... p_n, $v(p_n)$

or ZENER DIODE, label, p_i, $v(p_i)$, ... p_n, $v(p_n)$,

where label = model number ≤ 6 alphameric characters,

p_i = parameter name (see below),

$v(p_i)$ = parameter value.

PARAMETER NAMES

Mathematical Symbol (Fig. A-2)	Input Symbol
r_b	RB
r_s	RS
a	A
Ø	PHI
n	N
I_S	IS
Θ	THETA
K_D	KD
BV	BV
m	M

(c) Tunnel Diode

$$I_{TD} = A_A V e^{-AV} + B_B\left(e^{B_1 V} - e^{B_2 V}\right) + C_C\left(e^{CV} - 1\right).$$

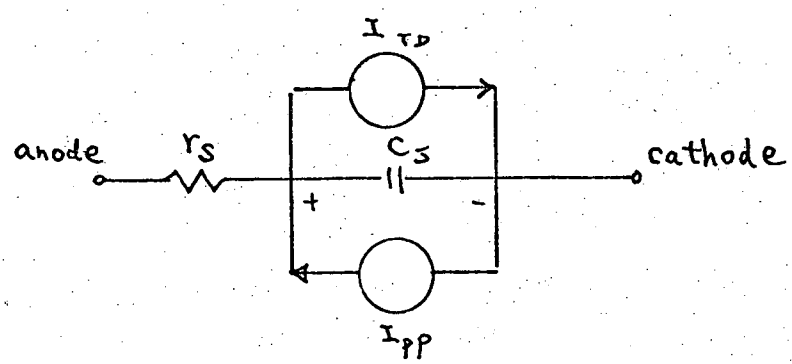


FIG. A-3. Tunnel Diode Model.

The format is

TUNNEL DIODE, label, p_i $v(p_i)$, ... p_n, $v(p_n)$,

where label = model number $\leq$ 6 alphameric characters,

p_i = parameter name (any of RS, AA, A, BB, B1, B2, CC, C, CJ of Fig. A-3),

$v(p_i)$ = parameter value.

(d) Four-Layer Device

$$C_{be} = \frac{a_1}{(\phi_1 + V_{be})^{n_1}} + \theta_{N_1} T_{CN_1} I_{EC} e^{\theta_{N_1} V_{be}}$$

$$C_{bc} = \frac{a_2}{(\phi_2 + V_{bc})^{n_2}} + \theta_{I_1} T_{CI_1} I_{CE} e^{\theta_{I_1} V_{bc}} + \theta_{N_2} T_{CN_2} I_{BS} e^{\theta_{N_2} V_{bc}}$$

$$C_{cs} = \frac{a_3}{(\phi_3 + V_{cs})^{n_3}} + \theta_{I_2} T_{CI_2} I_{SB} e^{\theta_{I_2} V_{cs}}$$

$$I_{be} = \left(1 + \frac{1}{\beta_{N_1}}\right) I_{EC}\left(e^{\theta_{N_1} V_{be}} - 1\right) - I_{CE}\left(e^{\theta_{I_1} V_{bc}} - 1\right)$$

$$I_{bc} = \left(1 + \frac{1}{\beta_{N_2}}\right) I_{BS}\left(e^{\theta_{N_2} V_{bc}} - 1\right) + \left(1 + \frac{1}{\beta_{I_1}}\right) I_{CE}\left(e^{\theta_{I_1} V_{bc}} - 1\right) - I_{EC}\left(e^{\theta_{N_1} V_{be}} - 1\right) - I_{SB}\left(e^{\theta_{I_2} V_{cs}} - 1\right)$$

$$I_{cs} = \left(1 + \frac{1}{\beta_{I_2}}\right) I_{SB}\left(e^{\theta_{I_2} V_{cs}} - 1\right) - I_{BS}\left(e^{\theta_{N_2} V_{bc}} - 1\right)$$

$$\beta_{N_1} = f_1(I_{N_1}),\ \beta_{N_2} = f_2(I_{N_2}),\ \beta_{I_1} = f_3(I_{I_1}),\ \beta_{I_2} = f_4(I_{I_2})$$

$$T_{CN_1} = f_5(I_{N_1}),\ T_{CN_2} = f_6(I_{N_2}),\ T_{CI_1} = f_7(I_{I_1}),\ T_{CI_2} = f_8(I_{I_2})$$

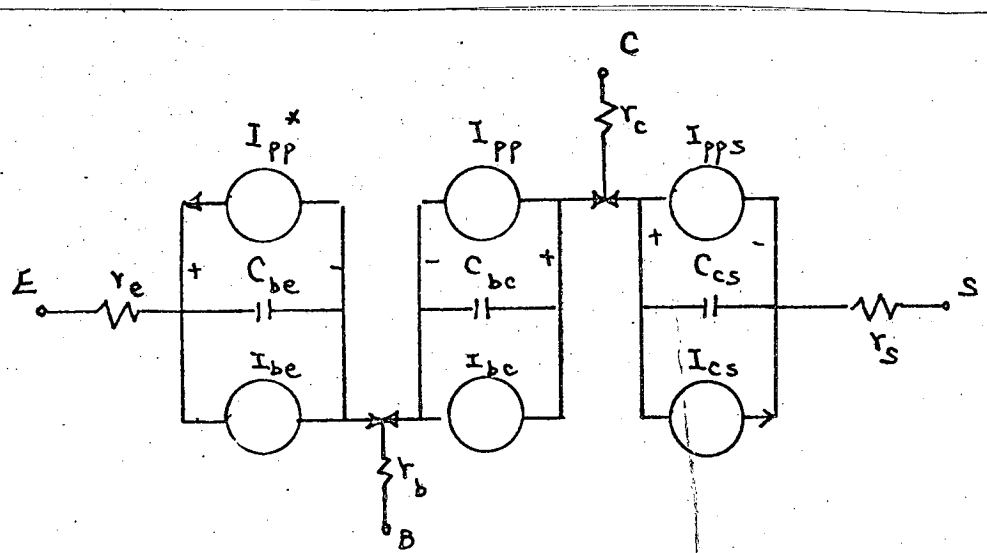


FIG. A-4. Four-Layer Device Model.

The format is

MICROTRANSISTOR, label, p_i, $v(p_i)$, ... p_n, $v(p_n)$,
table label, i_1, ... i_n, y_1, ... y_n,

where label = model number $\leq$ 6 alphameric characters,
p_i = single-valued parameter name,
$v(p_i)$ = value of parameter,
table label = any of BN1, BN2, BI1, BI2, TCN1, TCN2, TCI1, TCI2.

SINGLE-VALUED PARAMETERS

Mathematical Symbol (fig. A-4)	Input Symbol
r_e	RE
r_b	RB
r_c	RC
r_s	RS
a_1	A1
ϕ_1	PHI1
n_1	N1
a_2	A2
ϕ_2	PHI2
n_2	N2
a_3	A3
ϕ_3	PHI3
n_3	N3
I_{EC}	ISN1
I_{CE}	ISI1
I_{BS}	ISN2
I_{SB}	ISI2
Θ_{N_1}	THETN1
Θ_{N_2}	THETN2
Θ_{I_1}	THETI1
Θ_{I_2}	THETI2

Table Parameters: BN1, BN2, BI1, BI2, TCN1, TCN2, TCI1, TCI2, all functions of current.

(e) JFET

$$C_{gs} = \frac{C_{os}}{(V_s + V_{gs})^{n_s}}, \qquad I_{sd} = I_{sy}\left(1 - e^{-\Theta_x V_{sd}}\right),$$

$$C_{gd} = \frac{C_{od}}{(V_d + V_{gd})^{n_d}}, \qquad \Theta_x = f_1\,(V_{gs}),$$

$$I_{gd} = I_{sd}\left(e^{\Theta_d V_{gd}} - 1\right), \qquad I_{sy} = f_2\,(V_{gs}),$$

$$I_{gs} = I_{ss}\left(e^{\Theta_s V_{gs}} - 1\right).$$

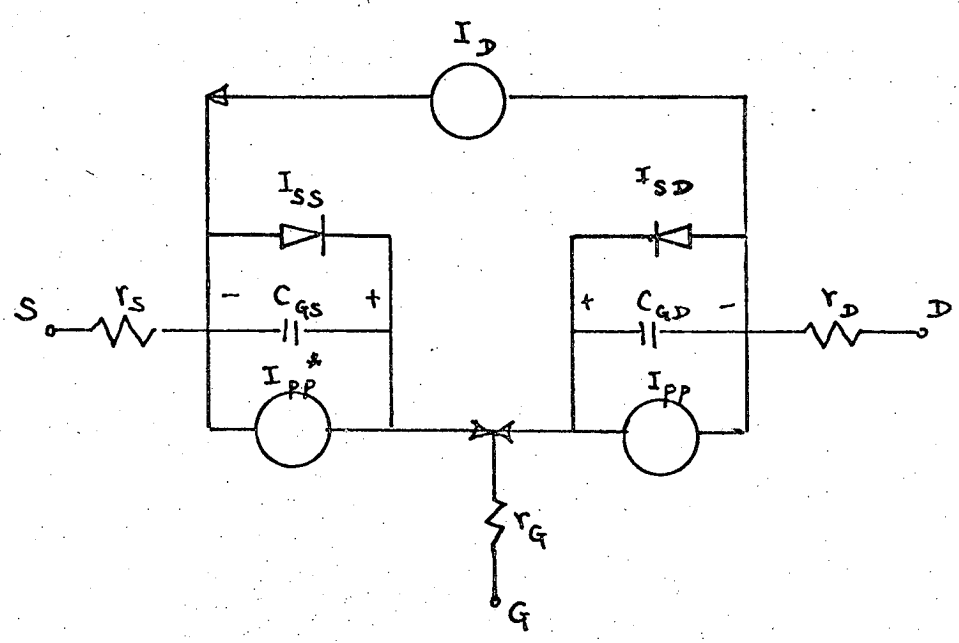


FIG. A-5. JFET Model.

The format is:

FIELD EFFECT TRANSISTOR, label, type, p_1, $v(p_1)$, . . . p_n, $v(p_n)$ table label, i_1, ... i_n, y_1, ... y_n,

where label = model number $\leq$ 6 alphameric characters,

p_i = single-valued parameter name (see below),

$v(p_i)$ = parameter value,

table label = any of ISY, THETAX,

type = NCHANNEL or PCHANNEL.

SINGLE-VALUED PARAMETERS FOR FET

Mathematical Symbol(Fig. A-5)	Input Symbol
R_s	RS
R_d	RD
R_g	RG
C_{os}	COS
V_s	VS
n_s	NS
θ_s	THETAS
I_{ss}	ISS
C_{od}	COD
V_d	VD
n_d	ND
θ_d	THETAD
I_{sd}	ISD

Table parameters: THETAX, ISY all functions of V_{gs}.

(ii) Photocurrent

All the photocurrent generators of the devices have the following format:

PHOTOCURRENT, label, ID, γ_b, t_s, t_1, ... t_n, i_1, ... i_n,

where label = model name,

$$ID = \begin{cases} \text{IPP for transistor base to collector generator} \\ \text{IPP* for transistor base to emitter generator} \\ \text{IPPD for diode photocurrent} \\ \text{IPP for FET drain to gate generator} \\ \text{IPP* for FET source to gate generator,} \end{cases}$$

γ_b = nominal curve peak radiation per second,

t_s = time at which radiation starts,

t_j = j^{th} time of radiation rate,

i_j = j^{th} value at j^{th} time (amp).

APPENDIX B. LEAST-SQUARE FIT METHOD[17)]

There are occasions when it is necessary to find m variables from one equation plus large amount of experimental data. It is easy to see one equation is insufficient to solve for m unknowns. The trick is to generate m linearly independent equations using Taylor's expansion and n experimental data ($m \leq n$).

As is well known, any function g can be expanded in Taylor's series,

$$g(x, e_1, e_2, \ldots e_m) = g\,(x, e_1^{\circ}, \ldots e_m^{\circ}) + \frac{\partial g}{\partial e_1} de_1 + \ldots + \frac{\partial g}{\partial e_m} de_m, \quad \text{(B-1)}$$

where e's are the unknowns,

x is the point where measurement is made.

Suppose the approximate values of e's are known and equal to e°'s, then

$$\begin{aligned} e_1 &= e_1^{\circ} + c_1 \\ &\vdots \\ e_m &= e_1^{\circ} + c_m, \end{aligned} \quad \text{(B-2)}$$

where c's are small constants. Combining Eqs. (B-1) and (B-2) gives

$$g(x, e_1, \ldots e_m) = g\,(x, e_1^{\circ}, \ldots e_m^{\circ}) + \frac{\partial g}{\partial e_1} c_1 + \ldots + \frac{\partial g}{\partial e_m} c_m,$$

evaluated at $(e_1^{\circ}, \ldots e_m^{\circ})$. (B-3)

Because there are experimental errors in the gathered data and there are neglected higher-order terms in the Taylor expansion, Eq. (B-3) will not be exactly the same as the experimental data point z. However, if the guesses (e^o's) are good, the difference, ε , between the measured and the predicted can be made small. Therefore, the idea is to make this difference go to zero.

In general, for n measurements there correspond n equations:

$$\begin{bmatrix} \frac{\partial g}{\partial e_1}(x_1) & \cdots & \frac{\partial g}{\partial e_m}(x_1) \\ \vdots & & \vdots \\ \frac{\partial g}{\partial e_1}(x_n) & \cdots & \frac{\partial g}{\partial e_m}(x_n) \end{bmatrix} \begin{bmatrix} C_1 \\ \vdots \\ C_m \end{bmatrix} + \begin{bmatrix} g(x_1, e_1^o \ldots e_m^o) - z_1 \\ \vdots \\ g(x_n, e_1^o \ldots e_m^o) - z_n \end{bmatrix} = \begin{bmatrix} \varepsilon_1 \\ \vdots \\ \varepsilon_n \end{bmatrix}. \qquad \text{(B-4)}$$

Now it is reasonable to assume that errors introduced during the measurements follow the normal Gaussian distribution. Therefore, to minimize the difference between the measured and the guessed values, one would want to minimize the sum of the errors:

$$\frac{\partial}{\partial C_k}\left[\sum_{j=1}^{n} \varepsilon_j^2\right] = 2\sum_{j=1}^{n} \varepsilon_j \frac{\partial \varepsilon_j}{\partial C_k} = 0 \quad \text{for } K = 1 \ldots m. \tag{B-5}$$

From Eq. (B-4),

$$\frac{\partial \varepsilon_j}{\partial C_k} = \frac{\partial g}{\partial e_k}. \tag{B-6}$$

Using Eq. (B-4) for ε and Eq. (B-6), Eq. (B-5) becomes

$$\sum_{i=1}^{m} C_i \left[\sum_{j=1}^{n} \frac{\partial g(x_j)}{\partial e_k} \frac{\partial g(x_j)}{\partial e_k}\right] = \sum_{j=1}^{n} \left[z_j - g(x_j)\right] \frac{\partial g}{\partial e_k}(x_j) \text{ for } K = 1 \ldots m. \tag{B-7}$$

To put (B-7) into a more concise form,

let

$$A = \begin{bmatrix} a_{11} & \cdots\cdots & a_{1m} \\ \vdots & & \vdots \\ a_{m1} & \cdots\cdots & a_{mm} \end{bmatrix},$$

$$C = \begin{bmatrix} C_1 \\ \vdots \\ C_m \end{bmatrix}, \quad b = \begin{bmatrix} b_1 \\ \vdots \\ b_m \end{bmatrix}, \quad y = \begin{bmatrix} y_1 \\ \vdots \\ y_n \end{bmatrix},$$

$$F = \begin{bmatrix} f_{11} & \cdots\cdots & f_{1m} \\ \vdots & & \vdots \\ f_{n1} & \cdots\cdots & f_{nm} \end{bmatrix},$$

where

$$a_{ki} = \sum_{j=1}^{n} \frac{\partial g}{\partial e_i} \frac{\partial g}{\partial e_k},$$

$$b_k = \sum_{j=1} \left(z_j - g(x_j)\right) \frac{\partial g}{\partial e_k},$$

for $k = 1 \ldots m$, $j = 1 \ldots n$, $i = 1 \ldots m$,

$$f_{jk} = \frac{\partial g(xj)}{\partial e_k},$$

$$y_j = z_j - g(x_j).$$

Then (B-7) becomes

$$[A]\,[C] = [b], \tag{B-8}$$

where $[A] = [F]'\,[F]$,

$[b] = [F]'\,[Y]$;

' implies transpose.

Gauss elimination is then used to solve for the c's in Eq. (B-8). With each iteration, better guesses of e^{o}'s can be found. Ideally, with infinite number of iterations, exact values for e's can be found, although in practice this is not done. Usually, criteria are set up such that once the e^{o}'s produced after several iterations meet these criteria, the iterations would stop. One of the possible criteria involves using elementary knowledge of statistics.

If the standard deviation σ is defined as

$$\sigma_y = \sqrt{\frac{1}{n} \sum_{j=1}^{n} (y_j - \mu_y)^2}\,, \tag{B-9}$$

where y = measured value ,

μ_y = mean value $= \frac{1}{n} \sum_{j=1}^{n} y_j$,

then the index of correlation, r, between the data and the predication can be defined as

$$r = \frac{\sigma_f}{\sigma_y} = \sqrt{1 - \frac{\varepsilon^2}{n\sigma_y^{\,2}}}\,, \tag{B-10}$$

where σ_f is the standard deviation of the prediction.

Using Eq. (B-9), Eq. (B-10) becomes

$$r = \sqrt{1 - \frac{\varepsilon^2}{\sum_{j=1}^{n} (y_j - \mu_y)^2}} \quad . \qquad \text{(B-11)}$$

With r so defined, a meaningful comparison between the various iterations can be made because r = 1 signifies the exact coincidence of measurement and prediction. Usually for a small number of variables, say three, convergence towards r = .98 is very fast.

Each of the two following programs consists of a main routine to set up the matrices (F, A, b, C), a subroutine to solve the matrices, a subroutine to calculate the correlation index, and a subroutine to plot the measured and predicted values to give visual appreciation of the proximity of the results. In the first program, the three parameters of the junction capacitance, a, n, Ø, are extracted from n capacitance measurements. In the second program, B, B_1, B_2 are found from the partial I-V curve of the tunnel diode.

```
CAPAC,7,20,42000.427104,CHEN
RUN(S,13300)
CAPAC.
EXIT.
DMP.
DMP(1000)
-
      PROGRAM CAPAC(INPUT,OUTPUT)
C     ***********************************************************************
C
C     LEAST SQUARE METHOD FOR CALCULATING COEFFICIENTS OF THE JUNCTION
C     CAPACITOR
C
C     ***********************************************************************
      DIMENSION X(25),Y(25),C(2),B(2),E(2),A(2,2),F(25,2),FT(2,25),Z(25)
     1,YFIT(25),WORD(8),PHI(2),G(2),GG(2),ZFIT(25)
      COMMON PHI
      DATA END /3HEND/
C
C     X, Y= MEASURED VALUES
C     E=ESTIMATED VALUES
C     F=ARRAYS OF THE PARTIAL DERIVATIVES EVALUATED AT VARIOUS X
C     FT=TRANSPOSE OF F
C     C=RESULTANT MATRIX FROM FT*F
C     B=RESULTANT VECTOR FROM FT*Y
C     WORD=TITLE
C     G,GG,COMP,ZFIT = DUMMY VARIABLES

    1 READ 5,WORD
    5 FORMAT(8A10)
      PRINT 9, WORD
    9 FORMAT(1H1,81H ***********************************************************
     1*************************//8A10//81H ************************************
     2*************************************************************)
      IF (WORD(1).EQ.END)STOP
    4 READ 10,I,G,PHI,NSTEP
   10 FORMAT(I2,8X,4F10.5,I1)
      DIV=(PHI(2)-PHI(1))/FLOAT(NSTEP)
      READ 20,(X(J),Z(J),J=1,I)
   20 FORMAT(2F10.5)
      V=FIT(I,X,Z,G)
      PRINT 21,G,V
   21 FORMAT(     * INITIAL GUESS E(I)= *,2E10.2/* FITNESS = *,F8.4)
      II=0
      COMP=0
   22 L=0
      E(1)=G(1)
      E(2)=G(2)
C
C     PARTIAL DERIVATIVE ARRAYS ARE SET UP
C
   30 DO 2 K=1,I
      O=PHI-X(K)
      F(K,1)=1./(O**E(2))
      F(K,2)=-E(1)*ALOG(O)*F(K,1)
      YFIT(K)=E(1)*F(K,1)
      Y(K)=Z(K)
    2 Y(K)=Y(K)-YFIT(K)
C
```

```
C     B COLUMN VECTOR IS SET UP
      DO 8 J=1,2
      B(J)=0
C
C     THE TRANSPOSE MATRIX FT IS SET UP
C
      DO 8 K=1,I
      FT(J,K)=F(K,J)
    8 B(J)=B(J)+FT(J,K)*Y(K)
C
C     A MATRIX IS SET UP
C
      DO 3 J=1,2
      DO 3 M=1,2
      A(M,J)=0
      DO 3 N=1,I
    3 A(M,J)=A(M,J)+FT(M,N)*F(N,J)
C
C     SUBROUTINE GAUSS CALLED TO SOLVE FOR C
C
      L=L+1
      CALL GAUSS(A,B,C)
      DO 6 K=1,2
    6 E(K)=E(K)+C(K)
C
C     FITNESS TEST
      V=FIT(I,X,Z,E)
      IF(L.GT.30)GO TO 11
      GO TO 30
   11 II=II+1
   40 FORMAT(* PHI= *,F8.3,* FITNESS= *,F12.7)
      PRINT 40,PHI(1),V
      IF(COMP.LT.V)12,13
   12 COMP=V
      PHI(2)=PHI(1)
      GG(1)=E(1)
      GG(2)=E(2)
      DO 14 K=1,I
   14 ZFIT(K)=YFIT(K)
   13 PHI=PHI+DIV
      IF(II.EQ.NSTEP)GO TO 16
      GO TO 22
   16 PRINT 60,PHI(2),COMP,GG
   60 FORMAT(*0BEST  PHI= *,F8.3,* FITNESS= *,F8.4,* A= *,E12.4,*N= *,
     1E12.4)
      CALL YGRAPH(I,X,Z,ZFIT)
      GO TO 1
      END
      FUNCTION FIT(I,X,Y,C)
C     ***********************************************************
C
C     TO TEST HOW CLOSE THE CALCULATED RESULTS FIT THE MEASURED RESULTS
C
C     ***********************************************************
      DIMENSION X(25),Y(25),C(2)
      COMMON PHI
      SUM=0
```

```
      IF(C(1).GT.5000.)C(1)=20.
      IF(C(2).GT.20.)C(2)=1.
      ERROR=0
      DO 1 J=1,I
      SUM=SUM+Y(J)
    1 ERROR=ERROR+(Y(J)-C(1)/(PHI-X(J))**C(2))**2
      AVE=SUM/FLOAT(I)
      SIGMA=0
      DO 2 K=1,I
    2 SIGMA=SIGMA+(Y(K)-AVE)**2
C
C     FIT=INDICATION OF THE EXACTNESS OF THE RESULTS
C     FIT=1 IMPLIES PERFECT
C
      W=ERROR/SIGMA
      IF (W.GE.1.)3,4
    3 FIT=0
      PRINT 901
  901 FORMAT(*0THE FIT=0 *)
      RETURN
    4 FIT=SQRT(1.-W)
      RETURN
      END
      SUBROUTINE GAUSS(A,B,C)
C     ***********************************************************************
C
C     GAUSSIAN ELIMINATION WITHOUT PIVOTING
C
C     ***********************************************************************
      DIMENSION A(2,2),B(2),C(2),AA(2,3)
C
C     ARRAY AA IS BEING FILLED
C
      DO 1 I=1,2
      AA(I,3)=B(I)
      DO 1 J=1,2
      AA(I,J)=A(I,J)
    1 CONTINUE
C
C     D=NORMALIZING FACTOR
C
      DO 2 K=1,1
      D=AA(K,K)
      DO 3 L=K,3
      AA(K,L)=AA(K,L)/D
    3 CONTINUE
      M=K+1
      DO 2 N=M,2
      D=AA(N,K)
C
C     DIAGONALIZING THE ARRAY A
C
      DO 2 I=K,3
      AA(N,I)=AA(N,I)-D*AA(K,I)
    2 CONTINUE
C
C     C=DESIRED RESULTS
C
      C(2)=AA(2,3)/AA(2,2)
```

```
      C(1)=(AA(1,3)-AA(1,2)*C(2))/AA(1,1)
      RETURN
      END
      SUBROUTINE YGRAPH(M,X,Y,YFIT)
      DIMENSION X(25),Y(25),YFIT(25)
      DATA IFFF,IBBB,IOOO,IPPP/1HF,1H ,1H*,1HI/
      YMIN=Y(1)
      YMAX=Y(1)
      DO 3 I=1,M
      IF(YMIN .GT .  Y(I))  YMIN=Y(I)
      IF(YMAX .LT. Y(I))  YMAX=Y(I)
      IF (YMIN .GT. YFIT(I)) YMIN=YFIT(I)
      IF (YMAX .LT. YFIT(I)) YMAX=YFIT(I)
    3 CONTINUE
      PRINT 1005,YMIN,YMAX
 1005 FORMAT (1H0,15X,E13.5,87X,E13.5/19X,101H----------
     1---
     2---------    )
      DO 1100 I=1,M
      IO=1.0+100.0*(Y(I)-YMIN)/(YMAX-YMIN)
      IO=MAX0(MIN0(IO,100),1)
      IP=1.0+100.0*(YFIT(I)-YMIN)/(YMAX-YMIN)
      IP=MAX0(MIN0(IP,100),1)
      IF (IO .NE. IP) GO TO 1030
 1008 IF (IO .NE. 1) GO TO 1020
      PRINT 1010,X(I),IFFF
 1010 FORMAT (1X,E13.5,6H      -,100A1)
      GO TO 1100
 1020 K=IO-1
      PRINT 1010,X(I),(IBBB,J=1,K),IFFF
      GO TO 1100
 1030 IPP=IPPP
      IOO=IOOO
      IF (IP .GT. IO) GO TO 1040
      IPP=IOOO
      IOO=IPPP
      IDUMMY=IO
      IO=IP
      IP=IDUMMY
 1040 IF (IO .GT. 1) GO TO 1060
      K=IP-IO-1
      IF (K .GT. 0) GO TO 1050
      PRINT 1010,X(I),IOO,IPP
      GO TO 1100
 1050 CONTINUE
      PRINT 1010,X(I),IOO,(IBBB,J=1,K),IPP
      GO TO 1100
 1060 K1=IO-1
      K2=IP-IO-1
      IF (K2 .GT. 0) GO TO 1070
      PRINT 1010,X(I),(IBBB,J=1,K1),IOO,IPP
      GO TO 1100
 1070 CONTINUE
      PRINT 1010,X(I),(IBBB,J=1,K1),IOO,(IBBB,J=1,K2),IPP
 1100 CONTINUE
      PRINT 1110,YMIN,YMAX
 1110 FORMAT (19X,101H-----------------------------------------------------
     1-----------------------------------------------  /16X,E13.5,87
     2X,E13.5)
```

```
      PRINT 1120
 1120 FORMAT (33H0I REPRESENTS THE PREDICTED POINT/28H0* REPRESENTS THE
     1DATA POINT/73H0F REPRESENTS BOTH THE DATA AND THE PREDICTED POINTS
     2 IF THEY LIE TOGETHER/1H1)
      RETURN
      END
C IB OF 2N2369
16          3.6       .2        .9        1.1    9
  -4.      3.12
  -3.5      3.23
  -3.      3.29
  -2.5     3.48
  -2.       3.63
  -1.5      3.82
  -1.      4.12
  -.9      4.17
  -.8     4.26
  -.6      4.38
  -.5       4.46
  -.4      4.55
  -.3       4.68
  -.2      4.91
  -.1      5.02
 0.        5.24
END
```

```
DIODE,7,25,42000.427104,CHEN
RUN(S,13500)
DIODE.
      PROGRAM DIODE(INPUT,OUTPUT)
C     ***********************************************************************
C
C     LEAST SQUARE METHOD FOR CALCULATING COEFFICIENTS OF THE PARTIAL
C     TUNNEL DIODE CHARACTERISTICS
C
C     ***********************************************************************
      DIMENSION X(25),Y(25),C(3),B(3),E(3),A(3,3),F(25,3),FT(3,25),Z(25)
     *,YFIT(25),WORD(8)
      DATA END /3HEND/
C
C     X, Z= MEASURED VALUES
C     E=ESTIMATED VALUES
C     F=ARRAYS OF THE PARTIAL DERIVATIVES EVALUATED AT VARIOUS X
C     FT=TRANSPOSE OF F
C     C=RESULTANT MATRIX FROM FT*F
C     B=RESULTANT VECTOR FROM FT*Y
C     WORD=TITLE
C
    1 READ 30,WORD
   30 FORMAT(8A10)
      PRINT 31,WORD
   31 FORMAT(1H1,81H*********************************************************
     1*************************//8A10//81H*************************************
     2*************************************************************)
      IF (WORD(1).EQ.END)STOP
      READ 10,I,E
   10 FORMAT(I2,8X,3F10.5)
      READ 20,(X(J),Z(J),J=1,I)
   20 FORMAT(2F10.5)
      L=0
      PRINT 21,E
   21 FORMAT(*0INITIAL GUESS E(I) =  *,3F10.5)
      W=0.
C
C     PARTIAL DERIVATIVE ARRAYS ARE SET UP
C
    2 DO 3 K=1,I
      O1=EXP(E(2)*X(K))
      O2=EXP(-E(3)*X(K))
      F(K,1)=O1-O2
      F(K,2)=E(1)*X(K)*O1
      F(K,3)=E(1)*X(K)*O2
      Y(K)=Z(K)
      YFIT(K)=E(1)*(O1-O2)
    3 Y(K)=Y(K)-YFIT(K)
      CALL YGRAPH(I,X,Z,YFIT)
C
C     B COLUMN VECTOR IS SET UP
C
      DO 4 J=1,3
      B(J)=0
C
C     THE TRANSPOSE MATRIX FT IS SET UP
C
```

```
      DO 4 K=1,I
      FT(J,K)=F(K,J)
    4 B(J)=B(J)+FT(J,K)*Y(K)
C
C     MATRIX A IS SET UP
C
      DO 5 J=1,3
      DO 5 M=1,3
      A(M,J)=0
      DO 5 N=1,I
      A(M,J)=A(M,J)+FT(M,N)*F(N,J)
    5 CONTINUE
C
C     SUBROUTINE GAUSS CALLED TO SOLVE FOR C
C
      L=L+1
      CALL GAUSS(A,B,C)
      IF(L.GT.100)GO TO 9
      DO 6 K=1,3
      E(K)=E(K)+C(K)
    6 CONTINUE
      PRINT 51,E
   51 FORMAT(*0NEW E(I)= *,3E14.5)
C
C     FITNESS TEST
C
      V=FIT(I,X,Z,E)
      PRINT 40 ,L,V
   40 FORMAT(*0L= *,I2,* FIT= *,F11.6)
C
C     CONVERGENT TEST
C
      IF (V.GT.(.995))7,8
    7 IF(V.LT.(W+.001))GO TO 9
    8 W=V
      GO TO 2
    9 PRINT 50,L,V,(E(K),K=1,3)
   50 FORMAT(*0AFTER *,I3,* TRIES ,FITNESS= *,F11.7,*,PERFECT IMPLIES
     1 FITNESS =1. */*0THE E ARE *,3E12.4)
      CALL YGRAPH(I,X,Z,YFIT)
      GO TO 1
      STOP
      END
      FUNCTION FIT(I,X,Y,C)
C     ***********************************************************************
C
C     TO TEST HOW CLOSE THE CALCULATED RESULTS FIT THE MEASURED RESULTS
C
C     ***********************************************************************
      DIMENSION X(25),Y(25),C(3)
      SUM=0
C
      CONSTRAINTS TO AVOID DIVERGENCE
C
      IF(ABS(C(1)).GT.500.)C(1)=10.
      IF(ABS(C(2)).GT.500.)C(2)=50.
      IF(ABS(C(3)).GT.50.)C(3)=5.
      ERROR=0
      DO 1 J=1,I
```

```
      SUM=SUM+Y(J)
    1 ERROR=ERROR+(Y(J)-C(1)*(EXP(C(2)*X(J))-EXP(-C(3)*X(J))))
      AVE=SUM/FLOAT(I)
      SIGMA=0
      DO 2 K=1,I
    2 SIGMA=SIGMA+(Y(K)-AVE)**2
C
C     FIT=INDICATION OF THE EXACTNESS OF THE RESULTS
C     FIT=1 IMPLIES PERFECT
C     FIT=0 INDICATES SINGULAR POINT
C
      W=ABS(ERROR)/SIGMA
      IF(W.GE.1.)3,4
    3 FIT=0
      PRINT 901
  901 FORMAT(*0THE FIT=0 *)
      RETURN
    4 FIT=SQRT(1.-W)
      RETURN
      END
      SUBROUTINE GAUSS(A,B,C)
C     ***********************************************************
C
C     GAUSSIAN ELIMINATION WITHOUT PIVOTING
C
C     ***********************************************************
      DIMENSION A(3,3),B(3),C(3),AA(3,4)
C
C     ARRAY AA IS BEING FILLED
C
      DO 1 I=1,3
      AA(I,4)=B(I)
      DO 1 J=1,3
      AA(I,J)=A(I,J)
    1 CONTINUE
C
C     B=NORMALIZING FACTOR
C
      DO 2 K=1,2
      B=AA(K,K)
      DO 3 L=K,4
      AA(K,L)=AA(K,L)/B
    3 CONTINUE
      M=K+1
      DO 2 N=M,3
      B=AA(N,K)
C
C     DIAGONALIZING THE ARRAY A
C
      DO 2 I=K,4
      AA(N,I)=AA(N,I)-B*AA(K,I)
    2 CONTINUE
C
C     C=DESIRED RESULTS
C
      C(3)=AA(3,4)/AA(3,3)
      C(2)=(AA(2,4)-AA(2,3)*C(3))/AA(2,2)
      C(1)=(AA(1,4)-(AA(1,2)*C(2)+AA(1,3)*C(3)))/AA(1,1)
      RETURN
```

```
      END
      SUBROUTINE YGRAPH(M,X,Y,YFIT)
      DIMENSION X(25),Y(25),YFIT(25)
      DATA IFFF,IBBB,IOOO,IPPP/1HF,1H ,1H*,1HI/
      YMIN=Y(1)
      YMAX=Y(1)
      DO 3 I=1,M
      IF(YMIN .GT .  Y(I))  YMIN=Y(I)
      IF(YMAX .LT. Y(I))  YMAX=Y(I)
      IF (YMIN .GT. YFIT(I)) YMIN=YFIT(I)
      IF (YMAX .LT. YFIT(I)) YMAX=YFIT(I)
    3 CONTINUE
      PRINT 1005,YMIN,YMAX
 1005 FORMAT (1H0,15X,E13.5,87X,E13.5/19X,101H----------------------------
     1---                                                    -
     2---------    )
      DO 1100 I=1,M
      IO=1.0+100.0*(Y(I)-YMIN)/(YMAX-YMIN)
      IO=MAX0(MIN0(IO,100),1)
      IP=1.0+100.0*(YFIT(I)-YMIN)/(YMAX-YMIN)
      IP=MAX0(MIN0(IP,100),1)
      IF (IO .NE. IP) GO TO 1030
 1008 IF (IO .NE. 1) GO TO 1020
      PRINT 1010,X(I),IFFF
 1010 FORMAT (1X,E13.5,6H      -,100A1)
      GO TO 1100
 1020 K=IO-1
      PRINT 1010,X(I),(IBBB,J=1,K),IFFF
      GO TO 1100
 1030 IPP=IPPP
      IOO=IOOO
      IF (IP .GT. IO) GO TO 1040
      IPP=IOOO
      IOO=IPPP
      IDUMMY=IO
      IO=IP
      IP=IDUMMY
 1040 IF (IO .GT. 1) GO TO 1060
      K=IP-IO-1
      IF (K .GT. 0) GO TO 1050
      PRINT 1010,X(I),IOO,IPP
      GO TO 1100
 1050 CONTINUE
      PRINT 1010,X(I),IOO,(IBBB,J=1,K),IPP
      GO TO 1100
 1060 K1=IO-1
      K2=IP-IO-1
      IF (K2 .GT. 0) GO TO 1070
      PRINT 1010,X(I),(IBBB,J=1,K1),IOO,IPP
      GO TO 1100
 1070 CONTINUE
      PRINT 1010,X(I),(IBBB,J=1,K1),IOO,(IBBB,J=1,K2),IPP
 1100 CONTINUE
      PRINT 1110,YMIN,YMAX
 1110 FORMAT (19X,101H-----------------------------------------------------
     1-----------------------------------------------  /16X,E13.5,87
     2X,E13.5)
      PRINT 1120
 1120 FORMAT (33H0I REPRESENTS THE PREDICTED POINT/28H0* REPRESENTS THE
```

```
1DATA POINT/73HOF REPRESENTS BOTH THE DATA AND THE PREDICTED POINTS
2 IF THEY LIE TOGETHER/1H1)
 RETURN
 END
```

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