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INTRODUCTORY REMARKS FOR THE PANEL DISCUSSION ON COMPUTER CONTROL

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Introductory Remarks for the Panel Discussion on

COMPUTER CONTROL*

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Summary

The control environment of the Bevatron is divided into a system of well-defined tasks, each capable of being treated individually but not separately. To maintain the individual aspect, but integrate all of the component tasks into a system structure, ours is the "multi-processor" concept of system organization. It was recognized that bulk-storage elements could not be provided separately for each processor, and in fact, advantage could be gained by utilizing the moderate speed disc-storage as a common-memory element thereby allowing the main-frame memory of each mini-computer to act as "cache" memory for each arm of the quasi-multi-processor. This allows the use of overlay techniques to provide an apparent vastly expanded software capability.

System Evolution

For reasons of economy, mixed with caution, the original inroads toward digital control were taken with mini-computers. It has become evident that the integration of these into a multi-faceted operating control system has resulted in what we now recognize as a multi-processor. As computer-control gained proponents throughout the accelerator world, the major contest was between "processor-per-task" installations and the "super-monitor" variety of multi-task large computers.

Our evidence and experience indicates that the evolution of the many small processor installations to the multi-processor organization was smooth and inevitable in retrospect. Our recommendation continues to be based upon a healthy experience of actual control, expanded over virtually every aspect of accelerator operation.

It must be emphasized that this growth in itself was not inevitable, but has occurred solely because certain advantages and flexibilities have been achieved through digital practices.

One particular advantage in multi-processors is the much larger task complexity capable of being undertaken within a finite time period. The transfer of data between processor and environment, and the calculation and bookkeeping time required in task accomplishment, determine the ratio of complexity versus number of elements controlled. This is trimmed and juggled until a point of equilibrium is reached, and the ratio becomes a constant. This is the limiting factor. By providing a separate processor arm for each task classification, we then achieve a linear increase in the value of the constant with each addition of an arm. This concept overcomes the ultimate saturation of system capability inherent with large single processors.

At the outset of digital systems evolution, a valid objection was raised as to the clumsiness of intercommunication between processor mainframe memories. An enormous duplication of data cells existed in each of the memories. With current techniques of associative cache memory blocks, made possible through the increase of throughput of contemporary memories, access of data and sub-routine blocks appears to the individual processor as though they existed for it alone.

A restraining note must be sounded here. Some control closed-loop servo systems require consistent real-time responses, thereby making untenable the inevitable interference in access of main-store by several competing processing arms. Because of the nature of these control tasks, a small amount of fully committed memory must exist for each of the individual processors.

System Organization

Since the inception of this multi-processor system, tasks have been added to overall system responsibility, by specifying task implementation by area-responsibility. Control of main-magnet pole-face windings is therefore handled by the processor responsible for guide-field control. Data-acquisition aimed toward beam-oriented problem diagnostics is the responsibility of the processor dedicated to the control of the rf system.

In order to provide maximum utilization of processor time, two avenues have been explored. First, many tasks originally performed by software have been implemented in hardware, with particular emphasis upon those tasks requiring iterative attention. Field and time related events relying upon comparisons made in real-time have been handled this way to greatly improve resolution as well as to free processors for an expanded task repertiore. An analysis of the computational aspects of control tasks resulted in the creation of a general-form arithmetic unit to provide a "firm-ware" approach to the solution of control algorithms. The second avenue led to almost complete elimination of software implemented input-output of data or commands. Essentially all transfers are performed through the direct memory access channels of the several mini-computers.

System Development

Initial work on the Bevatron's digital facility was undertaken in response to a complex control requirement. All available effort was directed toward implementing the task at hand. Creation of control hardware and establishing control algorithm left little effort directed toward interfacing the system to the accelerator operator. Early communication relied upon storage display units with software character-generation and the ubiquitous teletype. Only recently has a significant proportion of total effort been directed to a better understanding of human-machine interfacing problems, resulting in the creation of video-oriented text and graphic display devices. The pursuit of this area of critical importance in the overall field of automation will continue to be paramount among the tasks undertaken by the digital facility at the Bevatron.

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