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VARIABLE-TIME-DELAY CIRCUIT

Alfred A. Windsor

September 1958

Printed for the U.S. Atomic Energy Commission

VARIABLE-TIME-DELAY CIRCUIT

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Berkeley, California

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ABSTRACT

A variable-time-delay circuit combining maximum reliability and stability with minimum cost is presented. This circuit uses a high-Q series inductor-capacitor and diode. Delay times ranging from 5 microseconds to 5 milliseconds with a typical stability of better than 0.1% of the delay time are characteristic of this circuit.

VARIABLE-TIME-DELAY CIRCUIT*

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September 1958

A variable-time-delay circuit combining maximum reliability and stability with minimum cost can be approached by the use of passive elements.

A high-Q series LC diode circuit will ring one-half cycle in a very jitter-free way following an impulse charge on the capacitor.

In Fig. 1a, L_1 is made much smaller than L_2 in order to charge C_1 rapidly enough to consider t_1 the beginning of the time delay. C_1 is made large in order to give C_2 first order control and to keep a back voltage across diode 1. The design equations then become simply the half period of a series-resonant circuit consisting of C_1, C_2, and L_2:

$$\tau = \pi \sqrt{\frac{L_2 C_1 C_2}{C_1 + C_2}} = t_2 - t_1 .$$

As the current through the circuit approaches zero, the resistance of diode 2 becomes high and the voltage across C_1 plus the voltage across C_2 appears across R_2 with a rise time of L_2/R_2 seconds. C_1 is discharged by R_1 in R_1C_1 seconds.

Delay units have been built with delay times ranging from 5 microseconds to 5 milliseconds. These units have a stability of better than 0.1% of the delay time in the presence of environmental temperature, humidity, and magnetic-field changes.

Note the change in polarity and amplitude of the output pulse which could be restored to the same value as the input with a pulse transformer.

*Work done under auspices of the U. S. Atomic Energy Commission.

FIGURE LEGEND

Fig. 1. (a) circuit schematic; (b) waveforms.

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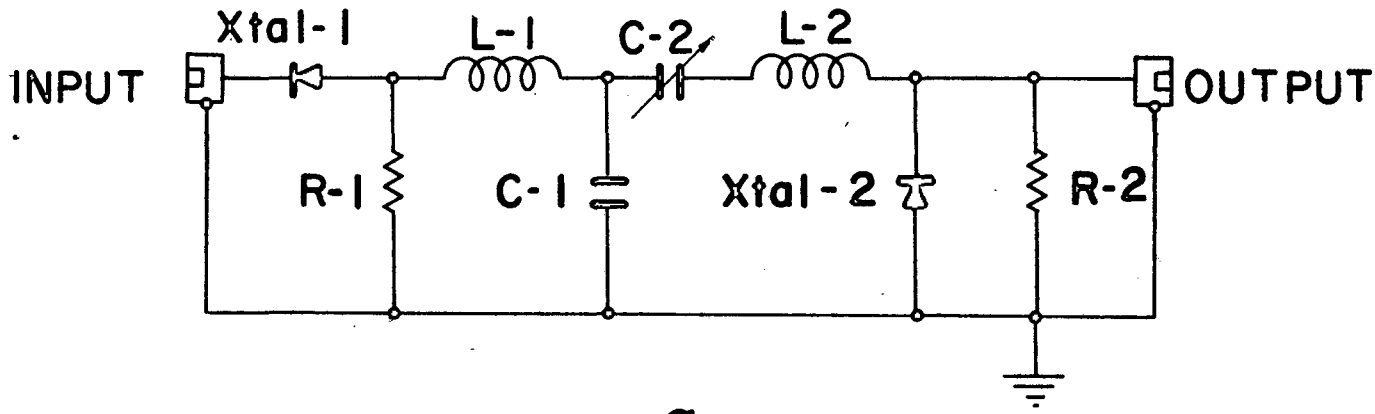
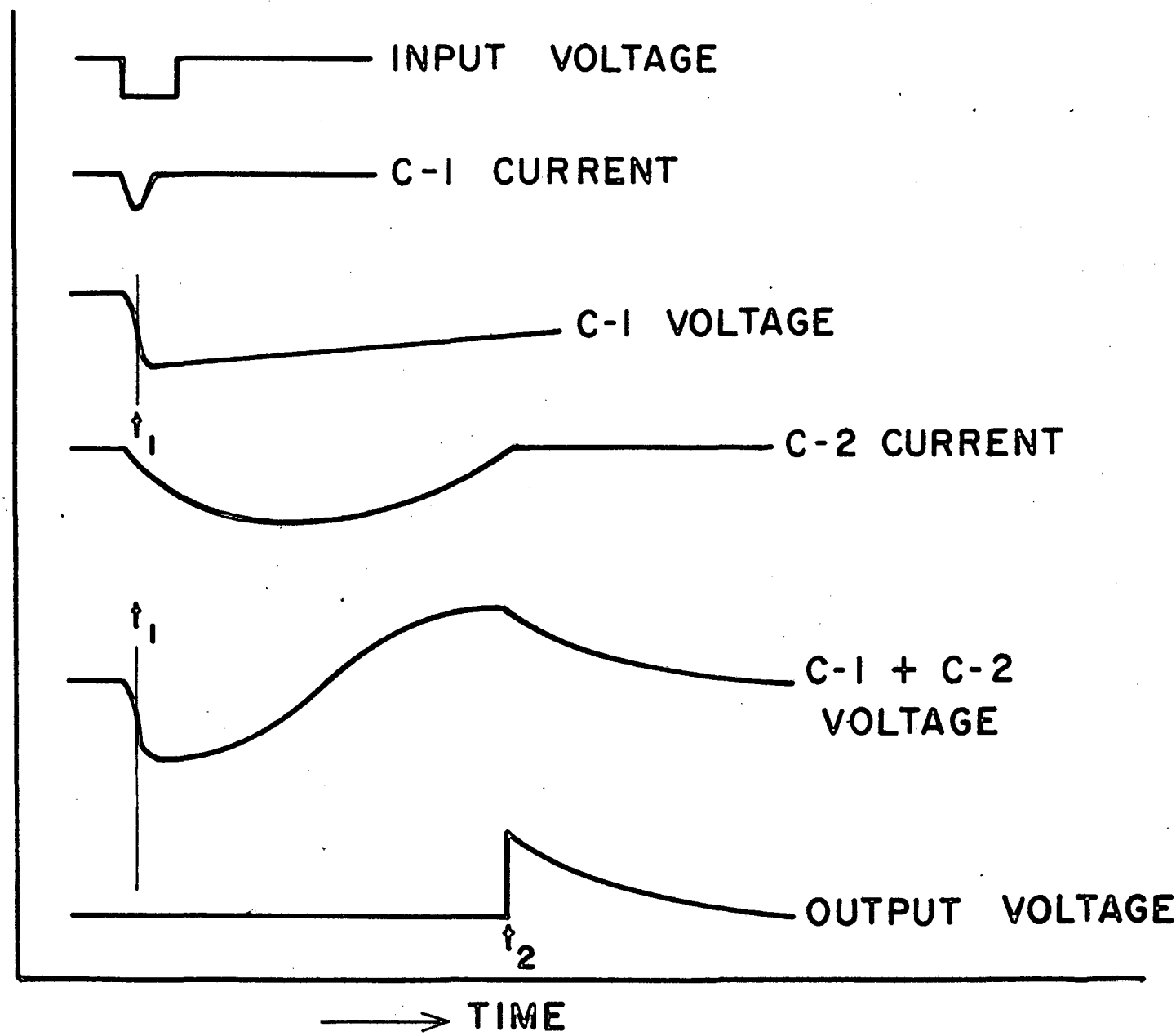

INPUT
Xtal-1
L-1
C-2
L-2
OUTPUT
R-1
C-1
Xtal-2
R-2

a


INPUT VOLTAGE
C-1 CURRENT
C-1 VOLTAGE
t_1
C-2 CURRENT
t_1
C-1 + C-2
VOLTAGE
OUTPUT VOLTAGE
t_2
TIME

b