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# CURRENT-SWITCHING CIRCUITRY

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Jack Gilbert Salvador

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## Abstract

This paper discusses a group of high-speed switching circuits using the basic current-switching mode of operation. Existing literature has described the steady-state analysis of the basic current-switching mode in performing numerous logical combinations. The first part of this paper presents a dynamic analysis of the basic current-switching mode. In previous work the assumption has been made that the dynamic switching characteristic of the circuit is that of a common-base amplifier with a current step applied to the emitter. When linear analysis techniques are used to find the natural frequencies present in the circuit, such an assumption argues that the gain-bandwidth product is the dominant natural frequency and therefore determines the switching time.

This paper shows that the basic current-switching mode is really an overdriven amplifier in a common-emitter configuration. Therefore the dominant natural frequency, which determines the switching time, is actually $f_\beta$, the short-circuit cutoff frequency in the common-emitter configuration. The comparison of switching-time estimates and experimental measurements, considering only the gain-bandwidth product, often shows agreement within less than a factor of two. The paper presents the reasons for this conformity but describes the errors introduced by considering the gain-bandwidth product alone.

The second part of this paper is the dynamic and steady-state analysis of a current-switching flip-flop. Authors of existing literature have assumed that the effect of the regenerative loop is negligible during switching and that the circuit switches in the basic current-switching mode. This paper shows that the natural frequency of the regenerative loop lies in the right-hand plane of the complex frequency plane, and is dominant during switching.

A conventional saturated Eccles-Jordan circuit is compared analytically and experimentally with the current-switching flip-flop. Switching time, pulse pair resolution, and repetition rate describe each circuit's operation.

## Part I: Dynamic Analysis of Basic Current-Switching Mode

The basic current-switching circuit is shown in Fig. 1. The configuration is that of a differential amplifier with one input tied to a reference potential. If $V_b$ is greater than $V_{bb}$, $T_1$ is "on" and $T_2$ is "off." If $V_b$ is less than $V_{bb}$, $T_1$ is "off" and $T_2$ is "on." The circuit can be thought of as a current source and two current sinks with the transistors acting as directional switches. Since most transistors require only a few tenths of a volt base-to-emitter bias to be either on or off, the side to which the current is switched can be controlled by very small voltages.

Consider for a moment the transistor as a switch. The speed of response of a transitor as a switch is determined by the "alpha cutoff" frequency, where alpha cutoff is defined as the short-circuit cutoff frequency of the transistor in the common-base configuration. In any given circuit the time constant associated with the collector capacitance may limit switching speed before the alpha-cutoff limit is reached. When thinking of very fast response times one must also consider the delay due to minority-carrier storage when a transistor is in the saturated condition. In addition to these factors one must consider that for most configurations a transistor cannot be "overdriven" when switching from on to off, as it can be when switching from off to on.

Alpha cutoff and collector capacitance are marked functions of the steady-state operating point of the transistor. A curve of collector current versus alpha cutoff has a peak point as some value of collector current. Collector capacity, on the other hand, is an inverse-power function of the base-to-collector voltage. For optimum switching times, then, the transistor should operate on a load line that has a large, fairly constant base-to-collector voltage and has current swings around the optimum value of collector current.

Now look again at Fig. 1. The load resistance can be chosen such that the collector-voltage swing is the same as the

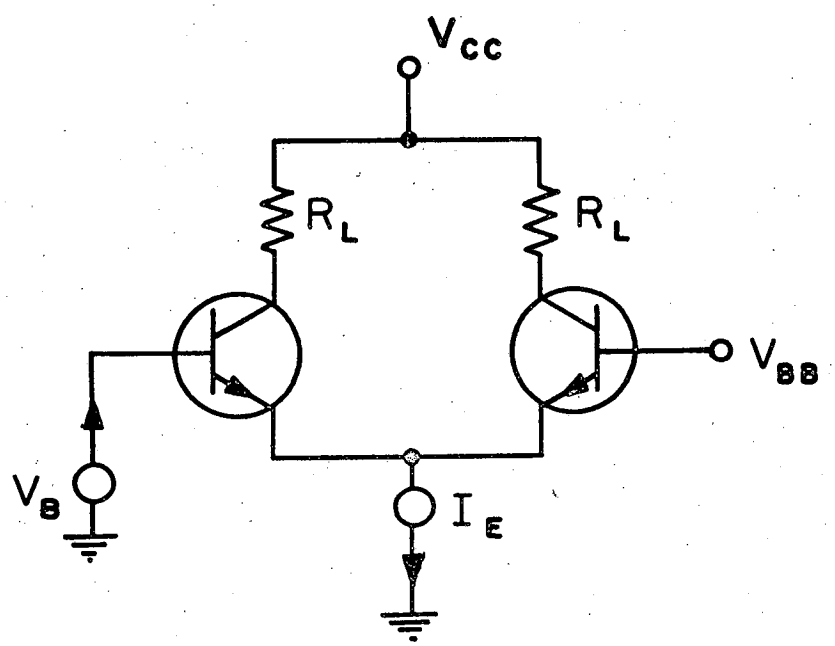


Fig. 1. Basic current-switching circuit.

base-voltage swing. If the collector-supply voltage is several times the base swing, one has a reasonably constant base-to-collector voltage. The current source in the emitter is set at the optimum value to give a maximum alpha-cutoff frequency. Since the transistor is never saturated, the delay due to minority-carrier storage is eliminated. This means that when predicting the on-to-off time for the transistor one need consider only the active-region operation of the transistor.

Figure 2 is a small-signal equivalent circuit of the basic current-switching configuration. The only energy-storage elements present in the circuit are the collector capacitances and the transistor-equivalent current generators. For a rough approximation the dominant-time-constant approach will be used to simplify the equivalent circuit. By eliminating the source of any time constant that is an order of magnitude away from the region of interest, one can obtain a rough approximation of switching times obtainable in a given circuit. This rough approximation will be called a "zero-order" approximation for the remainder of this paper.

The emitter resistors are an order of magnitude smaller than the other resistances present in the circuit, so that they can be ignored. The time constants associated with the energy-storage elements are as follows;

Collector capacitance: $$\tau_c = \left[ \frac{(R_s + r_b')r_b'}{R_s + r_o'} + R_L \right] C_c$$

Transistor-equivalent current generator: $$\tau = 1/\omega_t.$$

For very fast transistors the collector-capacitance time constant is of the same order of magnitude as the time constant associated with the transistor. The effect of collector capacitance for these cases can be accounted for by degrading the gain-bandwidth product by a degradation factor D. The degradation

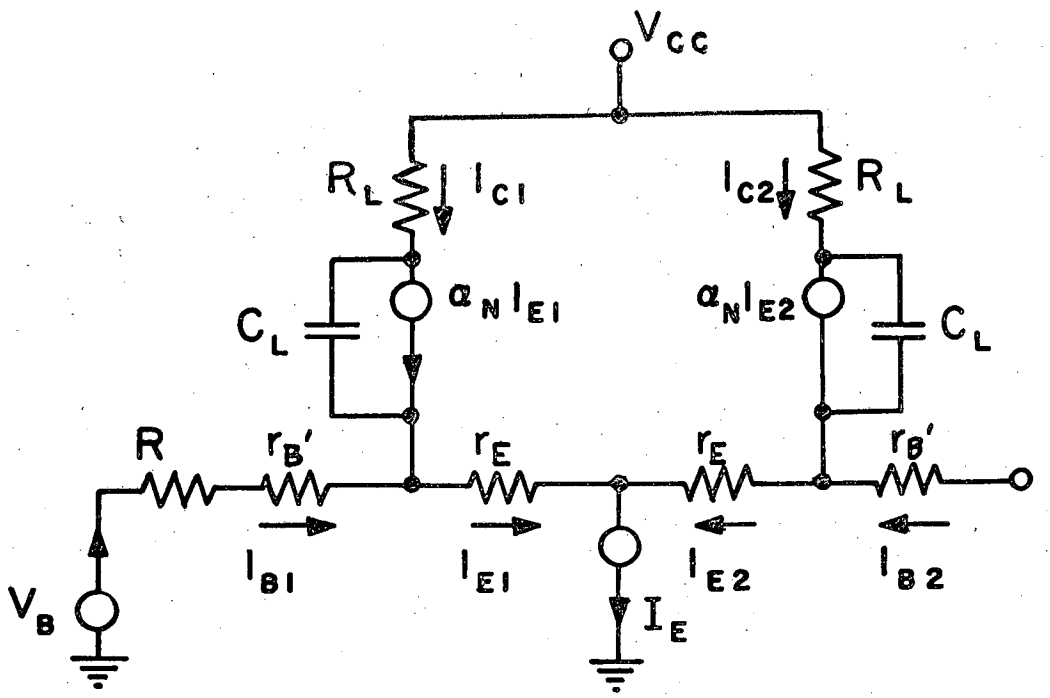


Fig. 2. Small-signal equivalent circuit.

factor is a constant determined by the circuit and transistor parameters, and is defined for the current-switching configuration as[1]

$$D = 1 + \omega_t \left[ \frac{(R_s + r_b')\, r_b'}{R_s + r_b'} + R_L \right] C_c .$$

Figure 3 is the simplified equivalent circuit for the basic current-switching configuration. This equivalent circuit neglects collector capacitance. The characteristic equation for the circuit during switching is

$$i_c(p) = \frac{\alpha_o\, \omega_t \left[ (V_b - V_{bb})(p+\omega_t) + I_e r_b'(p+\omega_\beta) \right]}{(R_s + 2r_b')(p+\omega_\beta)(p+\omega_t)} \qquad (1$$

The natural frequencies given by Eq. (1) are $\omega_t$ and $\omega_\beta$, the short-circuit gain-bandwidth product and the cutoff frequency, respectively, in the common-emitter configuration.

Equation (2) is the time-domain solution, assuming a step input, for collector current, neglecting initial conditions. It is obvious that the term containing $\omega_t$ is a good order of magnitude smaller than the term containing $\omega_\beta$, and can be neglected with little error.

$$i_c(t) = \frac{\beta_o (V_b - V_{bb})}{R_s + 2r_b'} \left[ 1 - \frac{1}{\alpha_o} \exp(-\omega_\beta t) + \frac{1}{\beta_o} \exp(-\omega_t t) \right] \qquad (2)$$

There are several conclusions to be drawn from Eqs. (1) and (2). First, it is obvious that the dominant natural frequency during switching is $\omega_\beta$. Second, the fast switching times obtainable from this circuit are a result of overdrive to the base of the transistor.

For fast switching times the quantity $\omega_\beta t$ in (2) is a small fraction. Therefore taking just the first two terms of the series

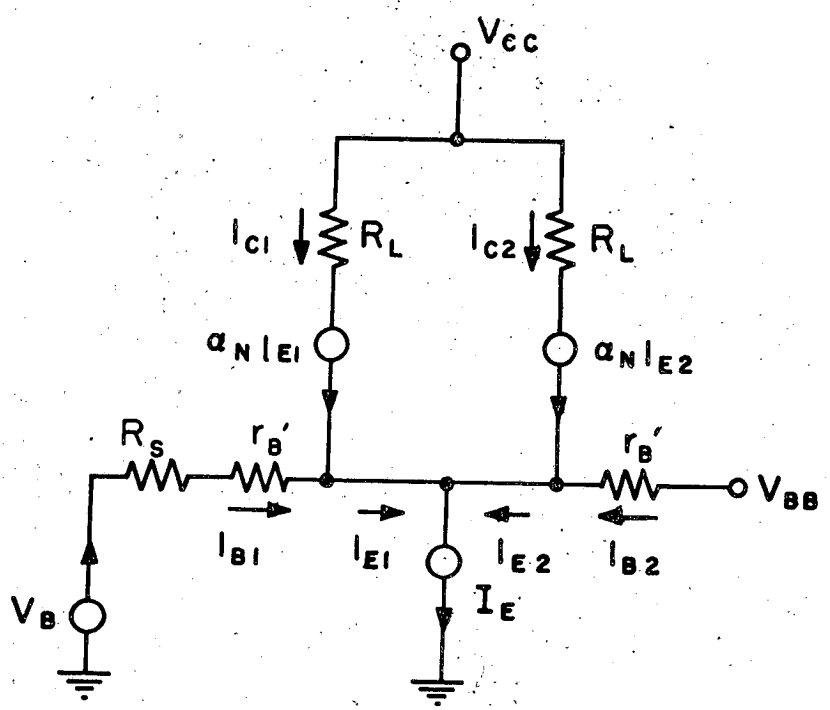


Fig. 3. Simplified equivalent circuit.

expansion of the exponential is a reasonable approximation. The result, ignoring the $\omega_t$ term, is

$$i_t(t) = \frac{\left(V_b - V_{bb}\right)}{R_s + 2r_b'} \quad \omega_\beta \beta_o t \ . \tag{3}$$

Solving this equation for t, one has

$$t = \frac{i_c(t)\,(R_s + 2r_o')}{(V_b - V_{bb})\,\omega_\beta \beta_o} \tag{4}$$

By definition the short-circuit gain-bandwidth product in the common-emitter configuration is

$$\omega_t = \beta_o \omega_\beta \ .$$

Making this substitution in Eq. (4) gives the switching time in terms of the gain-bandwidth product:

$$t = \frac{i_c(t)\,(R_s + 2r_o')}{(V_b - V_{bb})\,\omega_t} \ . \tag{5}$$

Equation (5) explains why the approach used in earlier literature of a common-base configuration with a step of current applied to the emitter gave reasonable results in terms of predicted switching times.[8] The fallacy of previous work lies in the fact that it did not show that switching times are a function of the base-spreading resistance of the transistor as well as source impedance.

Since the driven transistor switches on as the reference transistor switches off, Eqs. (6) and (7) give the turn-on and turn-off times respectively for a step input:

$$t = \frac{1}{\omega_\beta} \ln \left[ \frac{\beta_o (V_b - V_{bb})}{\left[\beta_o (V_b - V_{bb}) - 0.9\, I_e\, (R_s + 2r_b')\right] \alpha_o} \right] , \tag{6}$$

$$t = \frac{1}{\omega_\beta} \ln \left[ \frac{\beta_o \left(V_b - V_{bb} + I_e r_o' \left[1 - a_o\right]\right)}{0.1\, a_o I_e \left(R_s + 2r_o'\right) - \beta_o \left[I_e \left(R_s + r_o'\right)(1 - a_o) - (V_b - V_{bb})\right]} \right] \tag{7}$$

Table I shows predicted switching times versus experimental switching times. Because of the extremely fast switching times the basic current-switching circuit is capable of, the experimental verification was made with slow transistors so that accurate measurements could be made.

Table I

Switching times for transistors

| | Predicted (nanosec) | Experimental (nanosec) |
|---|---|---|
| Driven transistor | 110 | 120 |
| Reference transistor | 123 | 120 |

The transistors (type 2N35) used for experimental work have the following parameters:

Short-circuit cutoff frequency in the common-emitter configuration: $f_\beta = 101$ kc

Low-frequency current gain in the common-emitter configuration: $\beta_o = 40$

Short-circuit gain-bandwidth product in the common-emitter configuration: $f_t = 4$ Mc

Base-spreading resistance: $r_b' = 100$ ohms

Source impedance: $R_s = 200$ ohms

## Part II: Dynamic and Steady-State Analysis of Current-Switching Flip-Flop

Figure 4 shows a direct-coupled current-switching flip-flop. To direct couple from the collector circuit of one transistor to the base of the other transistor a level-shift is required. This particular circuit uses a so-called "zener" diode for a level-shifting device. By proper steady-state design the "zener" diode is always biased on; therefore, there is no loss of switching time or attenuation of signal in the level-shifting network, since the dynamic impedance and effective capacitance of the turned-on "zener" are approximately zero.

Figure 4 shows the dc levels present in a typical circuit, assuming the circuit has been previously "set." The values given neglect ohmic drops in a forward-biased base-to-emitter junction. Only transistor T-2 is on once the circuit is actually set.

Figure 5 gives the dc levels in the circuit with a reset signal applied to the base of T-4. As can be seen, T-2 is now biased off and T-4 is on. The point of interest in this state is that T-3, which is the lock-in transistor for the "reset" condition, has 3/8 volt reverse bias from base to emitter, so that it is still in the off condition. If the base potential of T-4 now goes negative, the emitter, which is clamped to the base potential, also goes negative. When the emitter potential has reached a point slightly more negative than the base of T-3, T-3 turns on and clamps the emitter point to its base potential. Any further negative swing on the base of T-4 causes this transistor to be back-biased and turn off. The circuit is now in its second stable state, the "reset" position.

There are two important points to understand. The first is that the circuit does not actually assume a stable state until the reset (or set) pulse is being removed. The second point is that for the purposes of dynamic analysis of switching times there are only two transistors active in the circuit at any one time.

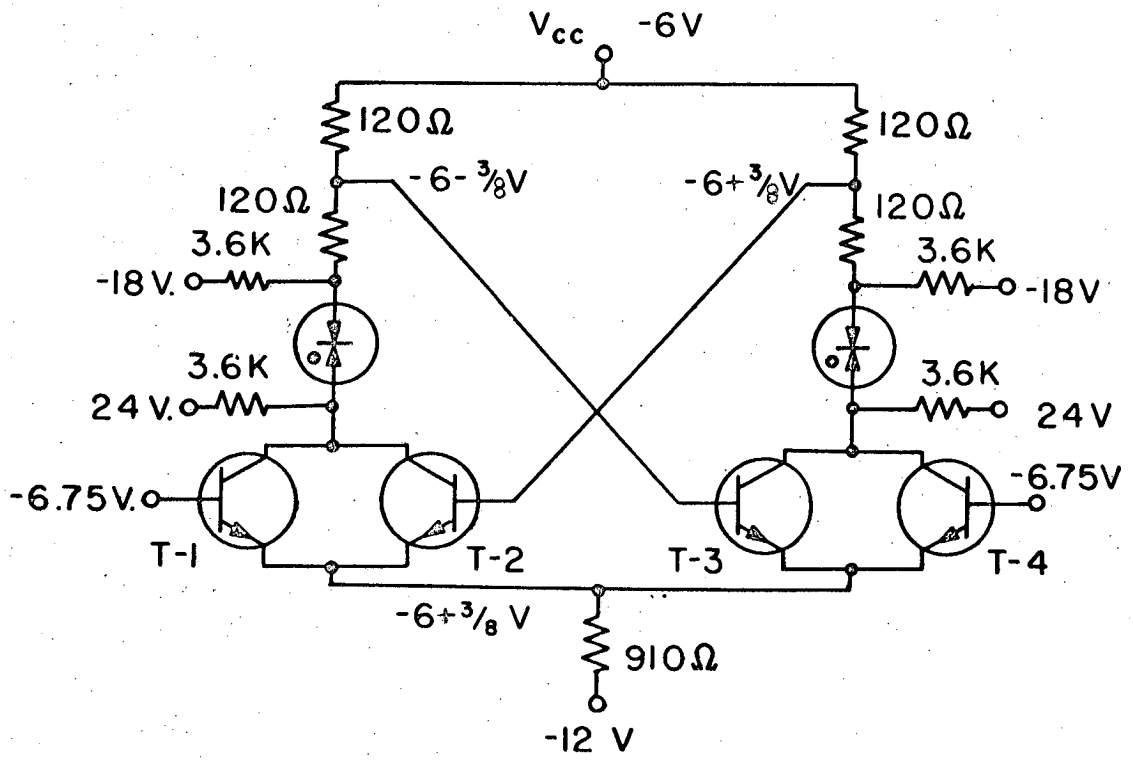


Fig. 4. Current-switching flip-flop; circuit previously set.

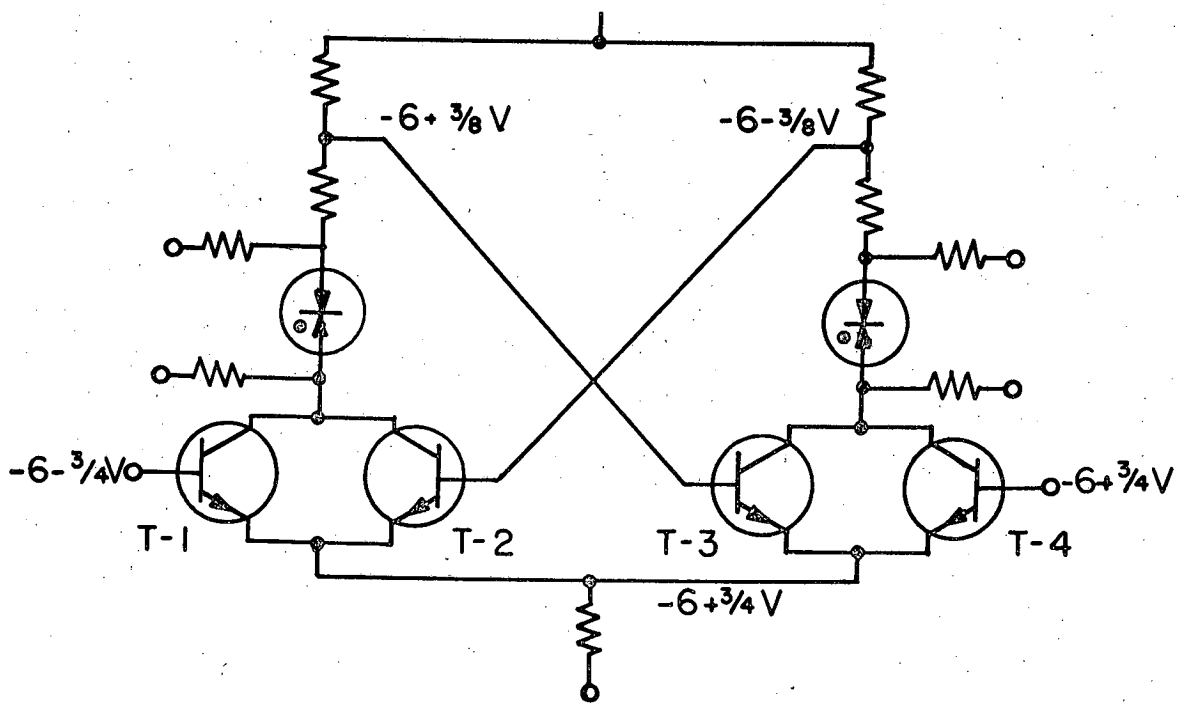


Fig. 5. Current-switching flip-flop; reset signal signal applied to base of T-4.

Figure 6 is a small-signal equivalent circuit of the flip-flop with the reset pulse applied. The assumption is made that the circuit has previously been set and that the reset pulse has brought T-4 into the active region. It must be noted that even though the analysis is presented for the reset condition, the same assumptions and results apply directly to the set condition using transistors T-1 and T-3 instead of T-2 and T-4. The equivalent circuit shown does not include the level-shifting network, since it does not contribute in any way to the dynamic response of the circuit but is present only to provide the correct dc levels.

The collector current of the driven transistor as a function of time is given by

$$i_c(t) = \frac{(1-2\alpha_o)(V_{cc}-V_b) + (1-\alpha_o)\ (1-\alpha_o)(R_s+r_b')I_e+\alpha_o I_e r_b'}{(1-\alpha_o)(R_s+2r_b') + R_L(1-2\alpha_o)} \times$$

$$\left\{1 - \frac{1}{\alpha_o\left(1+\frac{R_L}{R_L+R_s+2r_b'}\right)} \exp \omega_t \left[\alpha_o\left(1+\frac{R_L}{R_L+R_s+2r_b'}\right)-1\right] t\right\}. \tag{8}$$

The positive exponential clearly shows (a) that the circuit is regenerative during switching; and (b) that the natural frequency associated with the regenerative loop is dominant during switching. (See Appendix II.) The dominant natural frequency has a value approximately equal to the gain-bandwidth product modified by a ratio of the circuit impedances.

For transistors with small values of $r_b'$, Eq. (8) can be simplified to

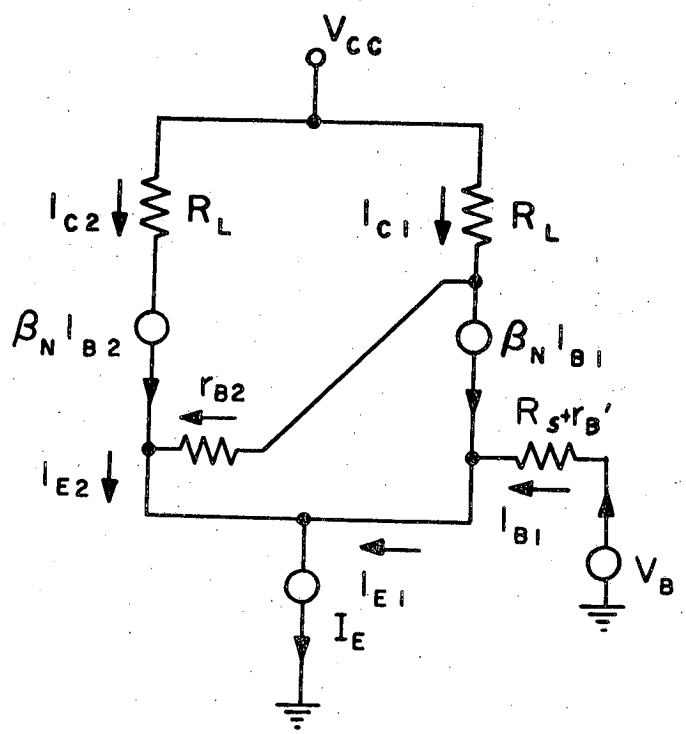


Fig. 6. Small-signal equivalent circuit of flip-flop.

$$i_c(t) = \frac{V_{cc} - V_b}{R_L} \left\{ 1 - \frac{1}{a_o\left(1 + \frac{R_L}{R_L + R_s + r_b'}\right)} \times \exp\left[ a_o \left( 1 + \frac{R_L}{R_L + R_s + 2r_b'} \right) - 1 \right] \omega_t t \right\} . \qquad (9)$$

Solving this equation for the 0-to-90% rise time, one has

$$t_{0-90\%} = \frac{1}{\left[ a_o \left( 1 + \frac{R_L}{R_L + R_s + 2r_b'} \right) - 1 \right] \omega_t} \times \ln \left( 1 - \frac{0.9 a_o I_e R_L}{V_{cc} - V_b} \right) \left( 1 + \frac{R_L}{R_L + R_s + 2r_b'} \right) a_o . \qquad (10)$$

Once the rise time of a flip-flop has been established, the criterion of usefulness of any flip-flop as an element in a system is usually given in terms of pulse pair resolution and maximum repetition rate. Because of the small voltage swings used in this circuit, a criterion had to established as to the minimum acceptable output. A collector voltage swing of 90% was established as the minimum required output.

In a conventional direct-coupled flip-flop, the "on" transistor is operated well into the saturated region. This means minority-carrier storage is a major problem in the circuit. Since a conventional Eccles-Jordan flip-flop can be designed to operate right on the edge of the saturated region, the minority-carrier storage time can be minimized. Minority-carrier storage is not a problem in the current-switching flip-flop, therefore the author felt that a comparison of the current switching flip-flop with a conventional Eccles-Jordan circuit would be more meaningful in terms of circuit capabilities.

In a conventional Eccles-Jordan flip-flop the recovery time of the coupling capacitances is normally the limiting quantity. Since the current-switching flip-flop is a direct-coupled circuit, the limiting quantity is the transistor switching time. Once the circuit has been set, the reset pulse can be applied immediately. The same reasoning leads to the conclusion that the maximum repetition rate is limited only by the switching time of the transistors. The only restriction that must be placed upon this result is that the set or reset pulse must be of the same duration as the switching time. This results from the fact that except for the "memory" of collector capacitances, there are no elements present in the circuit to remember what the state of the circuit was when the trigger pulse was removed. If the trigger pulse is removed when the circuit is only partially switched, the lock-in transistor on the driven side will try to turn on. Then the conditions exists of having both lock-in transistors in the active region with nothing to determine which way the circuit should go.

Before experimental results are given to verify the foregoing conclusions, a conventional Eccles-Jordan type of flip-flop will be presented so that a comparison may be made and the results will be more meaningful.

Figure 7 is a conventional saturated Eccles-Jordan flip-flop. The dynamic analysis of this circuit has been covered extensively in previous work so that the equations are presented without derivation.[1,5] Based on a zero-order approximation, Eq. (11) gives the 0-to-90% risetime of this circuit:

$$t_{o-90\%} = \frac{1}{\omega_t} \ln \frac{a_o}{a_o - 0.9} . \qquad (11)$$

The basic assumptions involved in the derivation of Eq. (11) are as follows:

(a) the time constant associated with the collector capacitance is negligible;

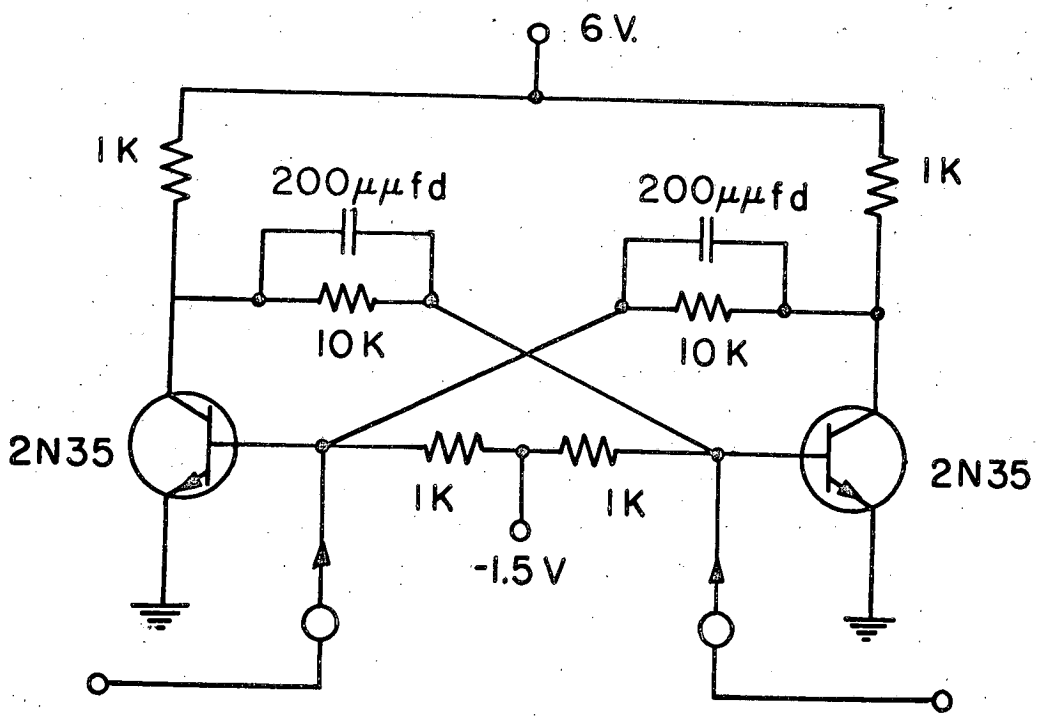


Fig. 7. Eccles-Jordan flip-flop.

(b) there is negligible change in charge on the coupling capacitors during switching;

(c) $r_b'$ and $r_e$ are negligible with respect to the other impedances present in the circuit.

For the circuit shown in Fig. 7 the circuit values were optimized experimentally. Using these values, a dominant-time-constant analysis shows that the above assumptions are valid.

To determine the minimum pulse resolution and the maximum repetition rate, the effect of the "memory" of the coupling capacitors must be considered.

The general equation for the collector current as a function of time is

$$i_{c1}(t) = K_o + K_1 \exp \omega_t t + K_2 \text{ -exp-}\omega_t t \,. \tag{12}$$

Since during switching the positive exponential is dominant, only the constant $K_1$ need be considered. From a first-order analysis which takes into account the initial conditions of the circuit, one has

$$K_1 = 1/2 \left[ i_{c2}(0+) - i_{c1}(0+) + G_t \left(V_{c2}(0+) - V_{c1}(0+)\right) + I_t \right] , \tag{13}$$

where $i_{c1}(0+)$ and $i_{c2}(0+)$ are the initial conditions of the collector currents,

$V_{c1}(0+)$ and $V_{c2}(0+)$ are the initial conditions of the coupling capacitors,

and $I_t$ is the value of the collector current when the trigger is removed.

Consider now the effect upon the circuit of applying two closely spaced pulses. Assume that the first pulse sets the circuit so that T-1 would be in the saturated condition. The second pulse then is a reset pulse which turns T-2 on and T-1 off.

Since Eq. (12) was given for T-1, after the second pulse is applied K-1 must be negative, as T-1 is now the off-going transistor. The initial conditions of the currents are fixed, since one transistor is saturated and the other transistor off. The value of the collector current when the trigger is removed is determined by the amplitude and duration of the trigger pulse. This leaves the difference in potential on the coupling capacitors as the determining factor for regeneration.

A minimum value for the difference in potential of the coupling capacitors can be determined from the conditions stated above. During recovery time, one capacitor is charging and the other is discharging. Knowing the time constants associated with each capacitor allows one to set the difference in voltage as a function of time equal to the minimum value. The circuit under consideration was designed so that the time constant associated with the capacitors is the same for both. Solving the equation described above for time, t, gives the minimum pulse pair resolution.

The minimum pulse-pair resolution as a function of the time constant of the coupling capacitors and a constant X, which is defined as the fraction of saturations current flowing when the trigger pulse is removed, are given by

$$t = T_{cc} \ln (2/\chi) . \tag{14}$$

If the second pulse were closer, in time, than the time given by Eq. (14), the constant K-1 associated with the positive exponential would be of the wrong sign for the circuit to be regenerative. Therefore Eq. (14) gives a lower bound for regeneration to exist in the circuit. The minimum pulse resolution is one-half the period of the maximum continuous repetition rate.[1]

## Experimental Verification

The values of circuit components for the respective circuits are those shown in Figs. 4 and 7. All circuit measurements were made with a Tektronix 545 oscilloscope.

The gain-bandwidth product and the short-circuit cutoff frequency in the common-emitter configuration were measured in a simple amplifier with the base-to-collector voltage and the collector current set to the same values as used in the current-switching circuits.

The values of $r_b'$ were determined by measuring the input impedance of the transistors in a common-emitter amplifier at a frequency equal to one-half the gain-bandwidth product. At this frequency or higher, the input impedance is approximately equal to the base-spreading resistance $r_b'$.

A set of four matched transistors was selected and the same transistors used in all circuits discussed.

Table II gives a comparison between experimental and predicted quantities for the Eccles-Jordan and current-switching flip-flops. All experimental results are within 20% of the predicted values. It should be noted that the predicted results are always better than the experimental results. This is as expected in view of the approximations made in deriving the equations for switching times.

Considering only the rise time of the circuit, it would appear that the Eccles-Jordan circuit would be the best circuit to use. The major differences between the circuits become obvious when the pulse-pair resolution and the maximum repetition rates are compared. In terms of pulse-pair resolution there is a factor-of-four difference in the two circuits. However, the maximum continuous repetition rate is different by a factor of seven. Basically the wide differences in the last two quantities given can be attributed to the recovery time of the coupling capacitors. In the current-switching circuit, the only energy-storage elements present are the transistors, therefore the frequency response and base spreading resistances of the transistors are the limiting quantities.

Table II

Comparison of flip-flop circuits

| | Eccles-Jordan | | Current-switching | |
|---|---|---|---|---|
| | Predicted | Experimental | Predicted | Experimental |
| Rise time, 0-90% (nanosec | 102 | 130 | 115 | 130 |
| Pulse-pair resolution (nanosec) | 460 | 500 | 115 | 135 |
| Maximum repetition rate (Mc) | 1.09 | 0.910 | 8.7 | 7.2 |

Another way of looking at the basic differences between the two circuits is as follows: in the current-switching circuit, as soon as the circuit is set, conditions are such that the circuit can become regenerative immediately if a reset pulse is applied. This is not true in the Eccles-Jordan circuit, since time must be allowed for the coupling capacitors to recover at least partially.

The main advantage of the Eccles-Jordan circuit lies in its simplicity. There are only two active devices present in the circuit. The advantage as far as transistor operation is concerned is in the low power the transistor dissipates when in the saturated condition. In the current-switching configuration the on transistor dissipates considerable power, as the collector-to-emitter voltage is about the same whether the transistor is on or off.

The advantages of the current-switching circuit from the point of view of transistor operation are: (a) the transistor never saturates; (b) collector capacitance can be minimized, since base-to-collector voltage is essentially constant; (c) only small voltage swings are required on the bases of the transistors, so that low-voltage transistors are easily used.

When a flip-flop is being considered as an element in a system, particularly a large one, the cost of the circuit must

be considered. Here the current-switching flip-flop is at an obvious disadvantage. It requires four transistors and two zener diodes, whereas the Eccles-Jordan circuit requires only two transistors. But in systems, such as large-scale computers, in which extremely fast flip-flops are required, the current-switching flip-flop is finding increasing use.

# APPENDIX I

## Derivation of Equations Presented in Part I

The simplified equivalent circuit given in Fig. 3 is assumed to be a valid representation of the basic current-switching mode during switching. The assumptions and approximations necessary to arrive at Fig. 3 are explained in Part I of the paper.

The circuit equations are:

$$i_{c1} = \alpha_n i_{e1} , \tag{A-1}$$

$$i_{c2} = \alpha_n i_{e2} , \tag{A-2}$$

$$i_{ei} + i_{e2} = I_e , \tag{A-3}$$

$$(V_b - V_{bb}) = i_{b1} (R_s + r_b') - i_{b2} r_b' , \tag{A-4}$$

$$i_{b1} + \alpha_n i_{e1} = i_{e1} , \tag{A-5}$$

$$i_{b1} + \alpha_n i_{e2} = i_{e2} . \tag{A-6}$$

In addition to the circuit equations, a one-pole approximation is assumed to be a reasonable representation of the roll-off of the transistor-equivalent current generator:

$$\alpha_n = \frac{\alpha_o \omega_t}{p + \omega_t} , \tag{A-7}$$

$$\beta_n = \frac{\alpha_n}{1 - \alpha_n} , \tag{A-8}$$

$$\beta_n = \frac{\alpha_o \omega_t}{p + \omega_\beta} \quad \text{where} \quad \omega_\beta = (1 - \alpha_o) \omega_t . \tag{A-9}$$

Solving the circuit equations for $i_{c1}$ gives

$$i_{c1} = \frac{V_b - V_{bb}}{R_s + 2 r_b'} \left( \frac{\alpha_n}{1 - \alpha_n} \right) + \frac{I_e r_b'}{R_s + 2r_b'} \alpha_n \tag{A-10}$$

Substituting (A-7) and (A-9) into (A-10) leads to

$$i_{c1} = \frac{\alpha_o \omega_t}{R_s + 2r_b'} \left[ \frac{(V_b - V_{bb}) p + (V_b - V_{bb}) \omega_t + I_e r_b' p + I_e r_b' \omega_\beta}{(p + \omega_t)(p + \omega_\beta)} \right] ; \tag{A-11}$$

is the characteristic equation.

Now, for $p = \frac{d}{dt}$, one has

$$\frac{d^2 i_{c1}}{dt^2} + \frac{d i_{c1}}{dt} (\omega_\beta + \omega_t) + i_{c1}\, \omega_\beta \omega_t$$

$$= \frac{a_o \omega_t}{R_s + 2r_b'} \left[ (V_b - V_{bb})\, \omega_t + I_e r_b'\, \omega_\beta \right] . \qquad \text{(A-12)}$$

Taking the Laplace transformation of (12) and solving again for $i_{c1}$, one obtains

$$i_{c1}(p) = \frac{\frac{a_o \omega_t}{R_s + 2r_b'} \left[ (V_b - V_{bb})\omega_t + I_e r_b' \omega_\beta \right] + \left[ p^2 + p(\omega_t + \omega_\beta) \right] i_{c1}(0+)}{p(p + \omega_\beta)(p + \omega_t)} \qquad \text{(A-13)}$$

From a partial-fraction expansion,

$$i_{c1}(p) = \frac{K_o}{p} + \frac{K_1}{p + \omega_\beta} + \frac{K_2}{p + \omega_t} , \qquad \text{(A-14)}$$

where

$$K_o = \frac{\frac{a_o \omega_t}{R_s + 2r_b'} \left[ (V_b - V_{bb})\, \omega_t + I_e\, r_b'\, \omega_\beta \right.}{\omega_\beta \omega_t} , \qquad \text{(A-15)}$$

$$K_1 = \frac{\frac{a_o \omega_t}{R_s + 2r_b'} \left[ (V_b - V_{bb})\, \omega_t + I_e r_b' \omega_\beta \right. - \omega_\beta \omega_t\, i_{c1}(0+)}{-\omega_\beta(-\omega_\beta + \omega_t)} \qquad \text{(A-16)}$$

$$K_2 = \frac{\frac{a_o \omega_t}{R_s + 2r_b'} \left[ (V_b - V_{bb})\, \omega_t + I_e r_b' \omega_\beta \right. - \omega_\beta \omega_t\, i_{c1}(0+)}{-\omega_t(-\omega_t + \omega_\beta)} . \qquad \text{(A-17)}$$

For small values of $r_b'$ the following approximation is valid:

$$(V_b - V_{bb})\, \omega_t \gg I_e r_b'\, \omega_\beta .$$

For "turn-on", $i_{c1}(0+) = 0$. Making this substitution and taking the inverse Laplace transform gives

$$i_{c1}(t) = \beta_o \frac{(V_b - V_{bb})}{R_s + 2r_b'} \left[ 1 - \frac{1}{a_o} \exp - \omega_\beta t \right] + \frac{1}{\beta_o} \exp(-\omega_t t) . \tag{A-18}$$

Looking at (18), we see that the quantity $\frac{1}{a_o}$ is much greater than $\frac{1}{\beta_o}$, therefore the exponential containing $\omega_t$ is negligible:

$$i_{c1}(t) = \beta_o \frac{(V_b - V_{bb})}{R_s + 2r_b'} \left[ 1 - \frac{1}{a_o} \exp \left[ -\omega_\beta t \right] \right] \tag{A-19}$$

To find the equation for $i_{c1}$ as the transistor is driven "off", consider the following:

$$i_{c1}(0+) = a_o I_e .$$

Equation (A-16) can be simplified to

$$K_1 = \frac{\frac{a_o}{R_s + 2r_b'} \left[ V_b - V_{bb} \right] - \left[ 1 - a_o \right] i_{c1}(0+)}{-(1 - a_o)} , \tag{A-20}$$

and

$$K_2 = \frac{\frac{a_o}{R_s + 2r_b'} \left[ V_b - V_{bb} \right] - \left[ 1 - a_o \right] i_{c1}(0+)}{\beta_o} . \tag{A-21}$$

For most circuit values, $\frac{\left[ V_b - V_{bb} \right]}{R_s + 2r_b'}$ is of the same magnitude as $i_{c1}(0+)$. Therefore one can say

$$\frac{a_o\left(V_b - V_{bb}\right)}{R_s + 2r_b'} \gg 1 - a_o \quad i_{c1}(0+) .$$

This means the contribution of the initial condition is negligible and (19) is valid for determining both on and off times for the driven transistor.

Since the basic current-switching configuration is not symmetrical, owing to the presence of source impedance, the collector current as a function of time of the reference transistor must be different from the driven transistor.

Starting with the general circuit equations, and proceeding in the same manner as described above, one finds the characteristic equation for $i_{c2}(p)$:

$$i_{c2}(p) = \frac{a_o\omega_t^2 I_e R_s(1-a_o) - a_o\omega_t^2(V_b - V_{bb})}{(R_s + 2r_b')(p)(p + \omega_t)(p + \omega_p)}$$

$$+ \frac{i_{c2}(0+)\, p\left[p(R_s + 2r_b') + (R_s + 2r_b')(\omega_t + \omega_\beta)\right]}{(R_s + 2r_b')(p)(p + \omega_t)(p + \omega_\beta)} . \quad \text{(A-22)}$$

The partial-fraction expansion is

$$i_{c2}(p) = \frac{K_o}{p} + \frac{K_1}{p + \omega_t} + \frac{K_2}{p + \omega_\beta} , \quad \text{(A-23)}$$

where the constants have the values

$$K_o = \frac{\beta_o\left[I_e(R_s + r_b')(1 - a_o) - (V_b - V_{bb})\right]}{(R_s + 2r_b')} , \quad \text{(A-24)}$$

$$K_1 = \frac{\alpha_o\left[I_e(R_s + i_b')(1 - \alpha_o) - (V_b - V_{bb})\right] - i_{c2}(0+)(R_s + 2r_b')(1-\alpha_o)}{(R_s + 2r_b')\,\alpha_o} \tag{A-25}$$

$$K_2 = -\frac{\alpha_o\ I_e(R_s + r_b')(1 - \alpha_o) - (V_b - V_{bb}) - i_{c2}(R_s + 2r_b')(1-\alpha_o)}{(R_s + 2r_b')(1-\alpha_o)\,\alpha_o}. \tag{A-26}$$

for the "off" to "on" condition, $i_{c2}(0+) \simeq 0$, therefore the reference transistor collector current as a function of time is given by

$$i_{c2}(t) = \frac{\beta_o\left[I_e(R_s + r_b')(1-\alpha_o) - (V_{bb} - V_{bb})\right]}{R_s + 2r_b'}\left\{1 + \frac{1}{\beta_o}\exp(-\omega_t t) - \frac{1}{\alpha_o}\exp(-\omega_\beta t)\right\}. \tag{A-27}$$

Again the term associated with $\omega_t$, the gain-bandwidth product, is negligible.

Looking at the constant in Eq. (A-27) one can see that as source impedance becomes negligible, the circuit becomes symmetrical, and the current through both transistors is represented by (A-19).

# APPENDIX II

## Derivation of Equations Presented in Part II

The simplified equivalent circuit given by Fig. 6 is assumed to be a valid representation of a current-switching flip-flop during switching.

The circuit equations are:

$$i_{b1} + \beta_n i_{b1} = i_{e1} , \tag{A-28}$$

$$i_{b2} + \beta_n i_{b2} = i_{e2} , \tag{A-29}$$

$$i_{e1} + i_{e2} = I_e , \tag{A-30}$$

$$i_{c1} = \beta_n i_{b1} + i_{b2} , \tag{A-31}$$

$$i_{c2} = \beta_n i_{b2} , \tag{A-32}$$

$$V_{cc} - V_b = i_{ci} R_L + i_{b2} r_b' - i_{b1}(R_s + r_b') . \tag{A-33}$$

In addition to the circuit equations, Eqs. (A-7) and (A-9) are assumed to be valid approximations of the transistor-equivalent current generator.

Solving the circuit equations for $i_{c1}(p)$, one finds the characteristic equation for switching:

$$i_{c1}(p) = \frac{\omega_t^2 \left[(1-2a_o)(V_{cc}-V_b) + (1-a_o)^2(R_s+r_b')I_e + a_o(1-a_o)I_e r_b'\right]}{\left[\dfrac{R_L}{R_L + R_s + 2r_b'}\right] p\,(p+\omega_t)\left\{ p + \omega_t \left[1 - a_o \left(1 + \dfrac{R_L}{R_L+R_s+2r_b'}\right)\right]\right\}} \tag{A-34}$$

Again taking the partial-fraction expansion of (A-34), one has

$$i_{c1}(p) = \frac{K_o}{p} + \frac{K_1}{p+\omega_t} + \frac{K_2}{p+\omega_t\left[1 - a_o\left(1 + \dfrac{R_L}{R_L+R_s+2r_b'}\right)\right]} , \tag{A-35}$$

where

$$K_o = \frac{(1-2a_o)(V_{cc}-V_b)+(1-a_o)^2(R_s+r_b')\,I_e + a_o(1-a_o)\,I_e r_b'}{\left(\dfrac{R_L}{R_L+R_s+2r_b'}\right)\left[1-a_o\left(1+\dfrac{R_L}{R_L+R_s+2r_b'}\right)\right]}\,, \tag{A-36}$$

$$K_1 = \frac{(1-2a_o)\,(V_{cc}-V_b)+(1-a_o)^2(R_s+r_b')\,I_e+a_o(1-a_o)I_e r_b'}{\left(\dfrac{R_L}{R_L+R_s+2r_b'}\right)\left(a_o\left[1+\dfrac{R_L}{R_L+R_s+2r_b'}\right]\right)} \tag{A-37}$$

$$K_2 = \frac{(1-2a_o)\,(V_{cc}-V_b)+(1-a_o)^2(R_s+r_b')\,I_e + a_o\,(1-a_o)\,I_e r_b'}{\left(\dfrac{R_L}{R_L+R_s+2r_b'}\right)\left(1-a_o\left[1+\dfrac{R_L}{R_L+R_s+r_b'}\right]\right)\left(-a_o\left[1+\dfrac{R_L}{R_L+R_s+2r_b'}\right]\right)} \tag{A-38}$$

For transistors with small values of $r_b'$, base-spreading resistance, and assuming small values of source-impedance $R_s$, one can make the following approximations:

$$(1-2a_o)\,(V_{cc}-V_b) \gg (1-a_o)^2\,(R_s+r_b')\,I_e\,,$$

$$(1-2a_o)\,(V_{cc}-V_b) \gg a_o(1-a_o)\,I_e r_b'\,.$$

Now consider the natural frequencies given by Eq. (A-34). The gain-bandwidth product is one natural frequency while the

second natural frequency is essentially the gain-bandwidth product modified by a ratio of circuit impedances. There is one major difference, though: the modified gain-bandwidth product is a positive exponential for realistic values of circuit resistances. Except for times very near zero, the positive exponential is dominant, therefore the time-domain solution for collector current, including the approximations listed above, is

$$i_{c1}(t) = \frac{(V_{cc}-V_b)}{R_L}\left\{1 - \frac{1}{a_o\left(1+\left(\frac{R_L}{R_L+R_s+2r_b'}\right)\right)}\exp\left[a_o\left(1+\frac{R_L}{R_L+R_s+2r_b'}\right)-1\right]\omega_t t\right\}. \tag{A-39}$$

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