Printability and Inspectability of Defects on the EUV Mask for sub32nm Half Pitch HVM Application

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ABSTRACT

The availability of defect-free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing, yet little data is available for understanding native defects on real masks. In this paper, a full field EUV mask is fabricated to see the printability of various defects on the mask. Programmed pit defect shows that minimum printable size of pits could be 17 nm of SEVD from the AIT. However 23.1nm in SEVD is printable from the EUV ADT. Defect printability and identification of its source along from blank fabrication to mask fabrication were studied using various inspection tools. Capture ratio of smallest printable defects was improved to 80% using optimized stack of metrical on wafer and state-of-art wafer inspection tool. Requirement of defect mitigation technology using fiducial mark are defined.

Keywords: EUV, mask, blank defect, mask inspection, blank inspection, wafer inspection, fiducial mark

1. INTRODUCTION

Over the past year, leading-edge chip manufacturers have shifted their interest towards the insertion of extreme ultraviolet lithography (EUVL). This emphasis is increasing the pressure to resolve defect-free blanks, which remains one of the key challenges impeding EUVL insertion into high volume manufacturing (HVM). The success of the industry's mask blank defect reduction effort critically depends on the timely availability of inspection tools, which can precisely and reliably find ever smaller defects. Blank inspection tool and defect review tool should be ready before EUV HVM. However, introduction of reticle inspection and defect review tools on time is a big concern. Practical printability and specification of defects should be primarily should be studied and defined [1-3]. This paper will discuss printability using programmed pit defect to see their printability and inspectability in EUV and DUV wavelength, required blank defect quality for device development for EUV lithography, benchmarking of next generation blank inspection tool, mask defect verification method using wafer inspection, and defect mitigation technology using fiducial mark. 3 different approaches are used to investigate of defect printability study in the paper.

- Defect printability: Programmed pit defect at 35nm HP and benchmarked the gap of currently available blank inspection tool. Printability of phase defect as half pitch, scanner condition and mask type is simulated.
- Defect inspectability: Requirement of blank inspection tool for successful device integration using EUV lithography. And, Benchmarking of various blank inspection tool and requirement of blank quality for device development
- Defect verification: Defect verification procedure and improvement of sensitivity using optimized wafer stack and inspection after etched wafer [4]. Defect mitigation technology using fiducial mark and requirement for implementation technology

2. DEFECT ON EUV MASK AND INSPECTION TOOL

Two types of defects can be found on the blank level of an EUV mask: surface pit or bump, which originate from embedded scratch or particles on the substrate. Those blank defects can be covered by absorber or fully opened after absorber patterning. Figure 1 shows defect types on the substrate and blank. Pit defects are the most dominant, accounting for on average 75% of the defects observed. Embedded particles on the substrate can be cleaned by an advanced cleaning process. The remaining 25% of the defects are due to particles deposited during the deposition process. The other types are pattern defects or carbon contamination on absorber side. Those can be repaired or cleaned after mask fabrication. [5] A blank inspection tool, patterned mask inspection tool, and defect review tool are needed to qualify the mask. However, a blank inspection tool with sufficient sensitivity and an EUV AIMS^{TM} are not currently available. Furthermore, it appears that this tool will not be available even for pilot line or early HVM operations. Consequently, the final EUV mask must be qualified by wafer inspection. It is therefore important to characterize potentially printable defects on EUV masks by wafer inspection tool. Shallow blank defect, which is not detected by blank inspection tool, can be prited on the wafer. And only wafer inspection tool can detect these kinds of small and shallow blank defects in Figure 2. Pattern defect can be detected using current pattern mask inspection tool. However it is hard to predict the printability on the wafer without EUV AIMS^{TM}.

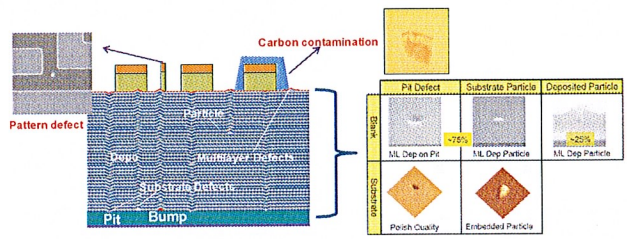


Figure 1. Types of defects on an EUV blank

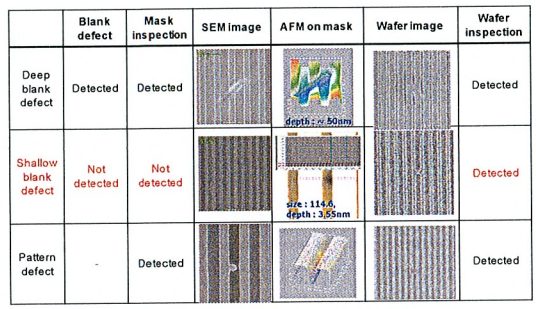


Figure 2. Detectability and printability of defect

3. EXPERIMENTAL

We mainly discuss phenomenon and issue for blank defect on EUV mask. This paper will present how to define the defects induced from the mask blank and propose how to improve the sensitivity of wafer inspection tool for better qualification of final EUV mask in Table 1. 9 Full field EUV mask including 1 programmed pit defect mask and 8 full field EUV masks are used for this study. All EUV masks are manufactured using standard EUV process. Blank inspection A, B, and C are compared for the inspection of blank inspection. 3 wafer inspection tools are compared to detect printed blank defects with sufficient sensitivity. Defect printability is simulated with S litho from Synopsys to predict the required blank defect specification for next generation device node. This work will define the requirement and introduction timing for next generation blank inspection tool. Wafer exposures are done using the EUV ADT (Alpha Demo Tool) at CNSE in Albany and IMEC in Belgium.

Table 1. Summary of defect printability study in the paper.

Requirement of blank defect specification	Requirement of blank defect quality	Defect verification & qualify
Programmed pit defect at 35nm HP	Requirement of blank inspection tool	Defect verification procedure based on wafer inspection
Gap of currently available blank inspection tool	Benchmarking of Blank inspection tool B and C	Improvement of wafer inspection
Simulation of phase defect as HP, scanner condition, and mask type	Requirement of blank quality for device development	Defect mitigation technology using fiducial mark

4. RESULTS AND DISCUSSION

4.1 Minimum printable programmed pit defect on 35nm HP.

EUV mask with programmed pit defect are manufactured using the method in Figure 4. First thin TaN layer with 16nm thickness is deposited on substrate and patterned. Designed pit sizes are varied from 60nm to 200nm to have various size of defect. Multilayer is deposited using smoothing method to make initial defects small and shallow. Measured width and depth with AFM can be converted to SEVD (spherical equivalent volume diameter) using Gaussian defect scheme (equation 1). Final size, depth, and SEVD value is visualized in Figure 3. Minimum defect has 0.55nm in depth, 23.9nm in FWHM (Full width at half maximum) on the multilayer level..

Equation 1 : SEVD conversion from depth and FWHM

$$(SEVD)_{Gaussian} = 2\left(\frac{3h_0(FWHM)^2}{16\ln(2)}\right)^{\frac{1}{3}}$$

$$pit\ \ depth = h_0$$

$$pit\ \ width = FWHM$$

Then TaN absorber is deposited on the multilayer and patterned. There are regions for 32,35,37, and 40nm HP in wafer scale. As no alignment option was used during e-beam writing, pit array position slightly moves along the y-axis. Degree of shift of defects in each unit is about 16nm in mask scale. In order to verify pit defect printability on the various positions of defects, 20 points were reviewed during defect review on 35nm HP region in Figure 5. When defect is located in the middle of ML area, AIT can see minimum printable defect of 23.1nm in SEVD, but ADT can see 28.3nm in SEVD. However, when defect is located near absorber sidewall, it will be more printable. AIT can see minimum printable defect of 17nm in SEVD, but ADT can see 23.1nm in SEVD in this case. Defect printability is very sensitive to the defect position. Blank inspection tool's specification should be based on the critical case to consider critical printable condition. Figure 6 shows sensitivity of currently available or next generation inspection tool to support [6-8]. Current blank inspection B has sensitivity of 30nm in SEVD. This value can't meet the requirement and this should be improved to be used for 35nm HP. However Blank inspection C with sensitivity in 23nm SEVD can support and quality EUV blank for 35nm HP. Currently blank inspection tool can detect the printable defect based on current resist and 35nm HP L/S pattern. But, we need confirm that what kind of inspection tool needs for sub 32nm HP generation. It is very hard to get the specification of minimum printable defect caused by difficulty of the fabrication of programmed defect and minimum resolution of current lithography performance. Simulation based approach was done in this study to predict the defect printability and blank inspection tool for 32 / 22/ 16nm HP in the next section.

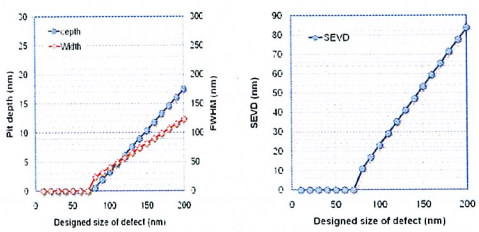


Figure 3. Size and depth of programmed pit defect

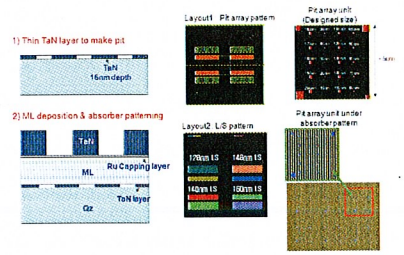


Figure 4. Reticle description with programmed pit defect

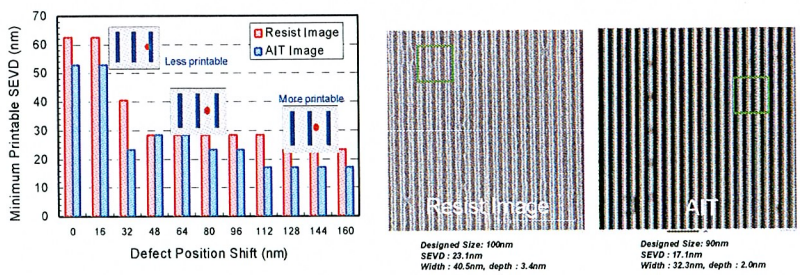


Figure 5. Minimum printable pit defect on 35nm HP

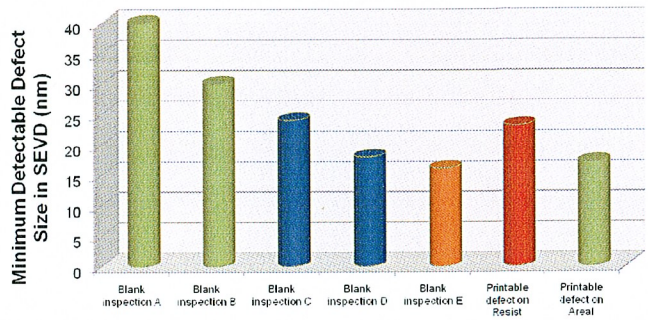


Figure 6. Sensitivity comparison & gap of blank inspection tool

4.2 Detectability based on blank inspection B and C

An EUV blank is inspected using blank inspection B and C to see which inspection tool can be used for 32nm HP device development. Experimental procedure is explained in detail in Figure 7. After wafer exposure using EUV ADT, all defects based on defect map from blank inspection B and C are reviewed in through focus with CD SEM. Figure 8 shows the various printed defects, which are captured with the information of blank inspection B. All defects have different behavior in through focus. Even defect of 1 pixel in blank inspection B is printed at -40nm defocus. 8 defects are printed on the wafer in best focus. Total printability of defect is 12%. 6 more defects are captured and printability goes up to 21% in through focus in Figure 9. When defects, detected by blank inspection C, are reviewed by CD SEM, more printed defects are found on the wafer in Figure 10. 23 more defects are found based on the defect map of blank inspection C. Figure 11 shows the printed defects detected by each blank inspection tool. More sensitive blank inspection tool or upgraded blank inspection B should be done for 32nm HP device development.

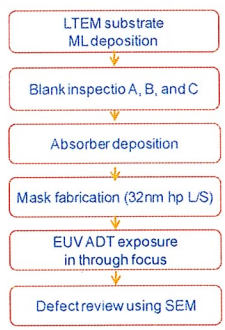


Figure 7. Experimental procedure

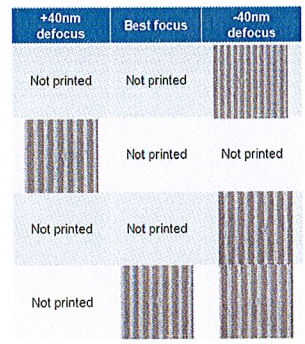
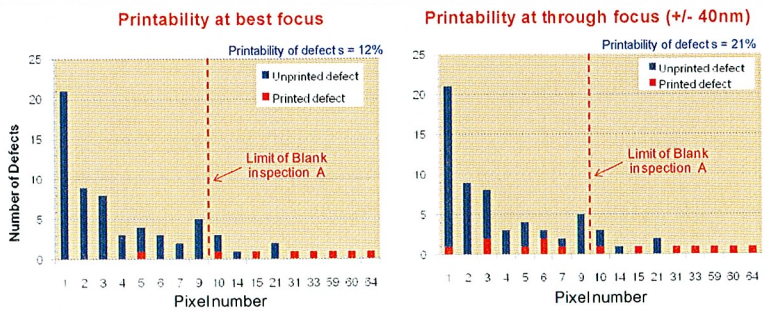


Figure 8. Focus dependency of blank defects



(a) Best focus (b) Through focus

Figure 9. Defect review captured by blank inspection B

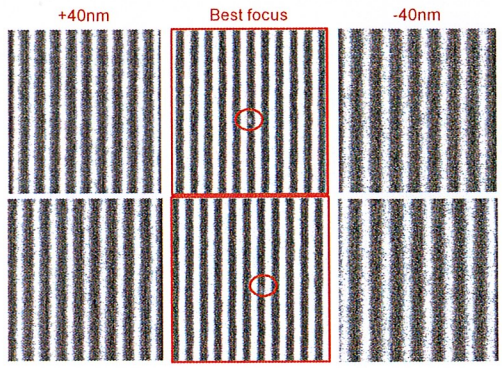


Figure 10. Defect review captured by blank inspection C

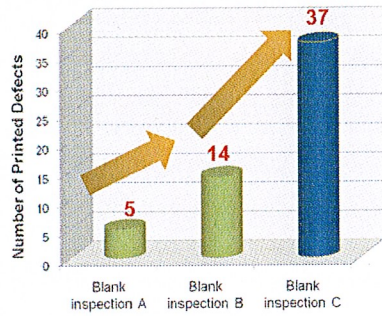


Figure 11. Number of printable defects

4.3 Simulation of phase defect printability

Phase defect printability is simulated using S litho from Synopsys as a function of FWHM and height with pattern of 1:1 L/S (line and space) for 32, 22, and 16nm HP. The simulations cover different mask types (absorber with thick and thinner thickness) and illumination conditions (conventional, annular, and dipole). Detailed condition is summarized in Table 3. The multilayer profile is assumed to be congruent with the phase defect profile. If smoothing or decorating occurs during multilayer deposition, the simulation results may be different. Constant threshold model is used, and the resist effect is not considered in the simulation. The defect printability criterion is 10% critical dimension (CD) variation in each line CD. All simulation result is visualized in Figure 12. Defect size of larger than 23~26nm in SEVD can be printed on 32nm HP. Blank inspection C can cover this range. This is identical results in section 4.1. In the case of 22nm HP, 23nm in SEVD for thick absorber and 19~22nm in SEVD for thinner absorber will be the killing defect. And more sensitive blank inspection tool (Blank inspection D) needs if thinner absorber is used for resolution enhancement technology. While, blank inspection C can be extended with thick absorber. Defect size of 16~18nm and 19~22nm in SEVD should be inspected for 16nm HP application for thick and thin absorber thickness, respectively. It is speculated that the scattered light from phase defect can be transmitted into absorber and affect the areal images.

Table 3. Simulation condition for phase defect printability

Simulation tool		S litho (Synopsys), Waveguide
Scanner	NA	0.25 / 0.32
	Illumination condition	Conventional / annular / dipole
Mask	Pattern CD	32 / 22 / 16nm HP (1X)
	Defect size / height	10 ~ 90nm / 0.5 ~ 4.25nm (4X)
	Absorber thickness	Thick, thin absorber

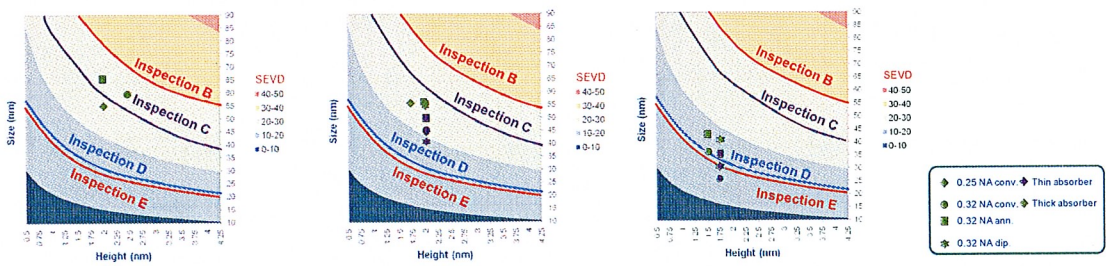
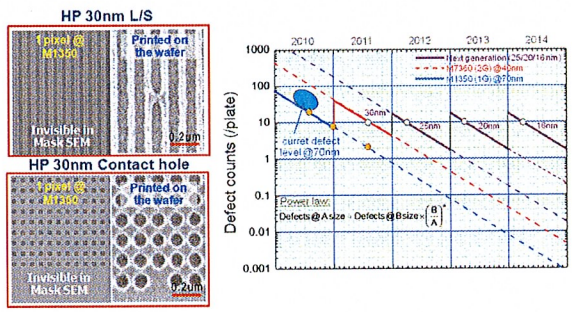


Figure 12. Phase defect printability and required blank inspection tool

4.4 Requirements of blank quality for device integration

However, current infra-structure for blank inspection is far from the requirement for successful EUV high volume manufacturing. First, all blank company qualify blank defect using M1350 in their manufacturing site. Many previous results are reported that M1350 doesn't have enough sensitivity. Defects with the size of 1 pixel at M1350 are printed on the wafer in the pattern of L/S or contact hole arrays in Figure 13(a). Second, current level of total number of defects on the blank is higher than the required roadmap for device development in Figure 13(b). Even current defect level using M1350 also can't meet the roadmap. Both minimum inspected size and total number on defect of EUV blank is critical and far away from the demand and requirement of industry. Figure 14 explains summary of previous section considering programmed defect, simulation, and benchmarking of various inspection tool based on device roadmap. Blank inspection B can cover 32nm HP. When thick absorber can be used for EUV mask, blank inspection B and C can support down to 16nm node device development. While thinner absorber needs to be used for RET, needs of blank inspection D or E should be studied now. And more aggressive study for actinic pattern mask inspection should be studied for proper introduction timing and business model.



(a) Inspection tool : Minimum size of defect (b) Blank quality : Total number of defect

Figure 13. Requirements for blank quality

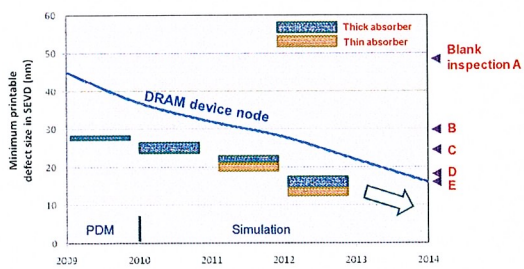


Figure 14. Required blank inspection tool for different blank structure.

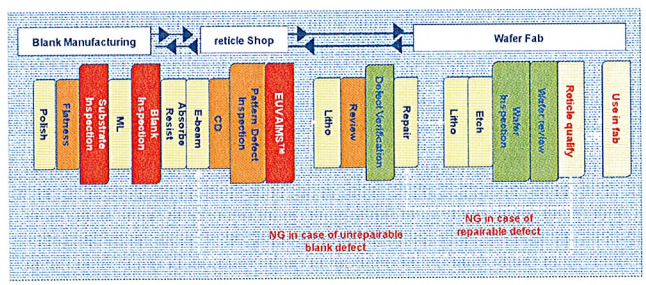


Figure 15. Defect verification process without EUV AIMS^{TM}

4.5 Defect verification method using full field EUV mask

Figure 15 shows the ideal defect verification method with sufficient EUV infra-structure of inspection and metrology. However, blank inspection tool should be more sensitive than this. Introduction timing for EUV AIMS^{TM} will be delayed to the second quarter of 2014 [9]. We need to take advantage of wafer inspection for defect verification of EUV mask. Figure 16 explains all detected defects in all fabrication process of full field EUV mask. 6 out of 17 blank defects and 1 out of 7 pattern defects are printed on the wafer. However when wafer is inspected with wafer inspection tool using developed wafer, only 2 defects are detected with repeater analysis. 1 of 2 detected defects by wafer inspection is classified as particle during mask handling or shipping, because this defect is not printed after mask cleaning. Only 1 out of 6 printed blank defects are detected by wafer inspection. This means that wafer inspection using developed resist pattern doesn't have enough sensitivity to detect all printed defects. 6 different full field EUV masks are qualified using this verification method described in Figure 14. All EUV masks are qualified with blank inspection, pattern mask inspection, and defect review on the wafer. Figure 17 shows that printability of blank defect is getting increased as

smaller device node and more multilayer open density. As the printability of defects is getting higher, detectability and capture ratio of defects with wafer inspection tool also can be increased.

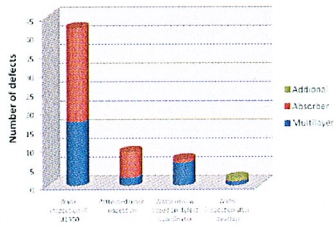


Figure 16. Number of defects during each step

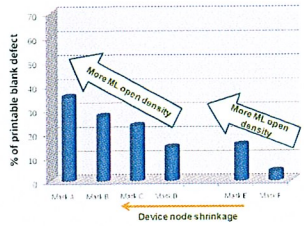
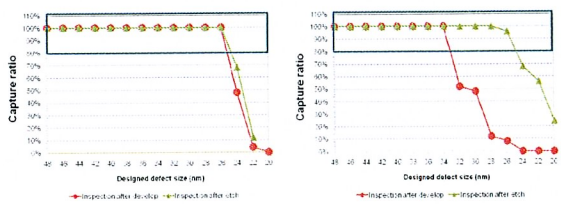


Figure 17. Printability of blank defect

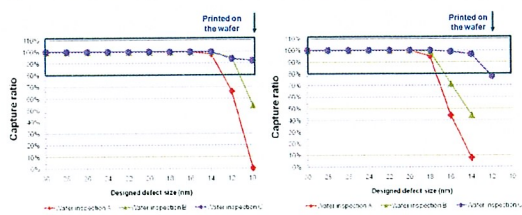
4.6 Improvement of wafer inspection for defect verification

The sensitivity of wafer inspection should be comparable of blank inspection or mask inspection. However, wafer inspection using developed wafer doesn't seem to have sufficient capture rate, and will cause missing defects. Many solutions are reported to improve the sensitivity of wafer inspection tool using through focus wafer inspection, optimized wafer stack for best condition of wafer inspection, and best wafer inspection tool [10-12]. The sensitivity of wafer inspection is evaluated using optimized wafer stack and best wafer inspection tool using programmed pattern defect mask. Through focus wafer inspection cannot be considered because little focus dependency of pattern defects on the absorber. The sensitivity of wafer inspection is improved using optimized SiN wafer stack (Figure 18) and 3 different wafer inspection tool (Figure 19). SiN etched wafer stack showed better sensitivity compared with developed resist stack in 40nm L/S pattern in the case of bridge type (a) and extrusion type (b) defect. This effect is more dominat in extrusion type defect. All 3 wafer inspection tools with SiN etched wafer show different sensitivity to see the tool effect. This is more dominant in extrusion type defect in Figure 19 (b). Wafer inspections C shows best sensitivity and succeeds to detect all printed defect on the wafer with more than 80% of sensitivity. As programmed absorber pattern defects are used in the study, there is little focus-dependent printability on the wafer. So, when printability in through focus of phase defects are used with optimized condition of wafer inspection, better sensitivity can be expected than the results described in Figure 19.



(a) Bridge type (b) Extrusion type

Figure 18. Comparison of developed and SiN etched wafer



(a) Bridge type (b) Extrusion type

Figure 19. Comparison of various wafer inspection tool

4.7 Defect mitigation technology using fiducial mark

Defect mitigation technology using with a few defects can be used when yield of defect free blank is low. After mask blank inspection, we need to get all necessary information on each phase defect so that we can define which kind of

defect is printable or which is not. Because phase defects under the absorber or open field are less likely to print on the wafer, any shift and rotation of the blank with regard to the phase defect before e-beam writing can hide the phase defect on the blank if there are fiducial marks on the blank in Figure 19. Defect mitigation is important in terms of cost of ownership on EUV mask. Standard and demonstration of defect hiding with fiducial mark has been reported to industry [13]. However there remain challenges to make more feasible technology such as pattern size to hide defect, alignment accuracy to fiducial mark, E-beam stage accuracy, and defect location accuracy. Defect position accuracy is show stopper to hide all potential killing defects on current infrastructure of blank inspection tool. Defect location under absorber is critical for the printability of defects. Because phase defect is the most printable when they are located near sidewall of absorber, partial hiding of defect can't be accepted to see the simulation result in Figure 20 (a). Current stage accuracy of blank inspection tool has around 350nm in 3sigma [14]. This value is larger than the minimum pattern size. So this technology can't be applicable with this level of defect location accuracy in Figure 21 (b). Figure 21 (c) calculate required defect location accuracy as pattern size using tolerance analysis, Defect location accuracy should be less than 30nm for sub 16nm HP application. Defect location accuracy is directly related with the stage of metrology tool. There are two options to have enough defect location accuracy with blank inspection tool or defect review tool such as EUV AIMS^{TM} with precise accuracy. Even if defect mitigation technology looks feasible, blank defect reduction should be kept down to meet the roadmap.

$$\sigma^2(A) = \sigma^2(B) + \sigma^2(C) + \sigma^2(D)$$

(A : Max space for defect to move under absorber (=CD-defect size), B : Inspection stage accuracy

C : Ebeam alignment accuracy to fiducial mark, D : Ebeam stage accuracy)

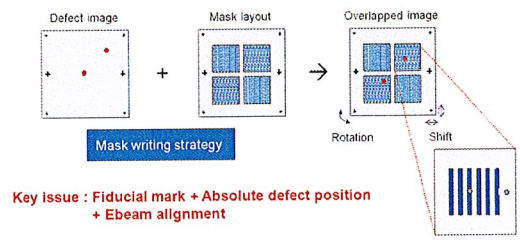
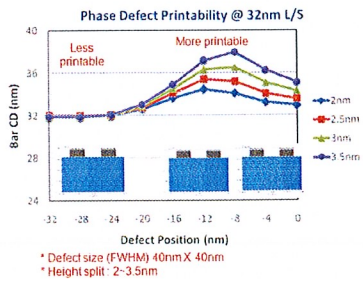


Figure 20. Fiducial mark for defect mitigation technology



(a) Printatility simulation as defect position

HP (1X)	32	22	16	11
Mask pattern size (4X)	128	88	64	44
E-beam alignment accuracy	15	15	15	15
E-beam stage accuracy	3.8	2.7	1.9	1.4
Defect position accuracy @ current blank inspection (*)	350	350	350	350

(b) Error budget analysis with current defect position accuracy

HP (1X)	32	22	16	11
Mask pattern size (4X)	128	88	64	44
E-beam alignment accuracy	15	15	15	15
E-beam stage accuracy	3.8	2.7	1.9	1.4

Required defect location accuracy (=stage accuracy of metrology tool)					
Blank defect size	10	116.9	76.4	51.8	30.4
	15	111.8	71.3	46.5	24.7
	20	106.8	66.2	41.2	18.6
	25	101.7	61.0	35.9	11.4
	30	96.8	55.8	30.3	-
	35	91.6	50.6	24.6	-
	40	86.5	45.4	18.5	-

(c) required defect position accuracy

Figure 21. Requirement of defect position accuracy for fiducial mark application (unit : nm)

5. CONCLUSION AND FUTURE WORK

The identification of defects on EUV mask blanks is a key technology for EUV lithography when used in mass production. In this paper, defect printability and inspectability are studied using simulation, PDM, and full field EUV masks with natural defects. Programmed pit defect shows that minimum printable size of pits could be 17 nm of SEVD from the AIT. However 23.1nm in SEVD is printable from the EUV ADT. Phase defect simulation shows that blank inspection B and C can't support 32nm node device development. When thick absorber can be used for EUV mask, blank inspection D or E can support down to 16nm node device development. But, needs of actinic inspection tool should be studied in the case of thin absorber. 14 printable defects are detected by blank inspection B and 25 more printed defects are detected by only blank inspection C. The sensitivity of wafer inspection is improved using optimized wafer stack and inspection tool. One tool detected more than 80% capture ratio on smallest programmed defect size. Requirement of defect mitigation technology using fiducial mark are defined. The most challenging issue is defect location accuracy. Less than 30nm of stage accuracy on the blank inspection tool or defect review tool should be guaranteed to hide the blank defect under absorber.

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