Printability Study of Pattern Defects in the EUV Mask as a Function of hp Nodes

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ABSTRACT

Amplitude defects (or absorber defects), which are located in absorber patterns or multilayer surface, can be repaired during mask process while phase defects (or multilayer defects) cannot. Hence, inspection and handling of both defects should be separately progressed. Defect printability study of pattern defects is very essential since it provides criteria for mask inspection and repair. Printed defects on the wafer kill cells and reduce the device yield in wafer processing, and thus all the printable defects have to be inspected and repaired during the mask fabrication. In this study, pattern defect printability of the EUV mask as a function of hp nodes is verified by EUV exposure experiments. For 3x nm hp nodes, defect printability is evaluated by NXE3100. For 2x nm hp node, since resolution of a current EUV scanner is not enough, SEMATECH-Berkeley actinic inspection tool (AIT) as well as micro-field exposure tool (MET) in LBNL are utilized to verify it,. Furthermore those printability results are compared with EUV simulations. As a result, we define size of defects to be controlled in each device node.

Keywords: EUV, mask, pattern defect, printability

1. INTRODUCTION

As integration of semiconductor device has been driven in recent years, introduction of next generation lithography technology has been required [3]. Among them, extreme ultraviolet lithography (EUVL) is one of the most leading lithography technologies for high volume manufacturing of sub-30-nm node devices [1, 2]. While there are many issues for the application of the EUVL to high volume manufacturing in industry, issues in EUV mask including mask defects and related infrastructures have ranked high and are of significance [4]. Fabrication of defect-free mask is very important since it affects yield of device. Mask defects in real cases come from manufacturing of blank, patterning process, wafer exposure, resist process, handling, etc. Fundamentally, we need to fabricate defect-free mask by removing all sources of defect generation, but it is practically very difficult. Therefore, combined with defect reduction, we should inspect all printable defects and repair them. At this point of view, defect printability study of the pattern defect is very essential since it provides criteria for mask inspection and repair [5-6]. Actinic review tool is required to verify whether a captured defect is printable or not,. However, since actinic review tool will not be ready within a couple of years, other evaluation tools should be utilized [7].

In this study, pattern defect printability of EUVL masks as a function of hp nodes is verified by EUV exposure experiments. For 3x nm hp nodes, defect printability is evaluated by NXE3100. For 2x nm hp node, it is evaluated by both SEMATECH-Berkeley actinic inspection tool (AIT) and also micro-field exposure tool (MET) in LBNL, since current NXE3100 is not enough to evaluate defect printability below 25nm hp nodes [8-9]. Furthermore those printability results are compared with EUV simulations. As a result, we define the size of printable defects to be controlled in each device node.

2. EXPERIMENTAL PROCESURE

For the simulations, we use Sentaurus-Lithography (S-Litho) EUV software using the waveguide algorithm, a kind of rigorous coupled wave analysis (RCWA) method. Basically, exposure conditions in ASML HVM tool (NXE3300) which include a numerical aperture (NA) of 0.33, several illumination conditions with conventional, quasar and dipole illumination, and an incident angle of 6 degree with a 4x reduction are applied in the simulations [10]. The optical constants, i.e., the refractive index n and the extinction coefficient k, are obtained from the measurement of samples from blank suppliers at the Advanced Light Source (ALS) BL 6.3.2 at Lawrence Berkeley National Laboratory (LBNL) [11]. For the simulation of resist image, SEVR140 resist parameters determined by Synopsys and IMEC are applied [12].

Patterned masks are fabricated in Samsung mask shop using commercial blanks provided by a supplier. The blanks consist of Ta-based ARC and absorber layers on Ru capped Mo/Si multilayer. A NXE3100, which is installed at Samsung electronics, is utilized for wafer exposure experiment with NA of 0.25, 4x reduction, and a conventional illumination with σ of 0.8 with a field of view of 26 x 33 mm^2 at the wafer plane. The resist images on the wafer are analyzed using a Hitachi CD SEM.

SEMATECH-Berkeley Micro-exposure tool (MET) in LBNL is utilized for the wafer exposure experiments of 2x nm hp, which has NA of 0.3 and several illumination conditions with conventional, 45-degree rotated dipole, and 18 nm dipole. JSR EUV resist is used for MET exposure experiment. Also, SEMATECH Berkeley actinic inspection tool (AIT) is used for defect printability experiment of 30-20nm hp node. Experimental conditions are wavelength of 13.4nm and NA of 0.35(4x). The images are taken by through-focus mode with 400nm step.

3. RESULTS AND DISCUSSION

3.1 Printability of programmed defect at 30nm hp

To verify defect printability at 30nm hp, programmed pattern defects were designed with splitting the defect size, and wafer exposure tests were evaluated by NXE3100. As previously mentioned, wafer review was fulfilled due to lack of actinic review tool. Figure 1 shows the mask SEM images and wafer SEM images for programmed defects. Concerning printability of programmed defect, sometimes wafer review images can give vague results due to LWR of resist itself. The printable sizes of the programmed defects are ~45nm and ~60nm for extrusion and intrusion defects, respectively, by standards of visibility.

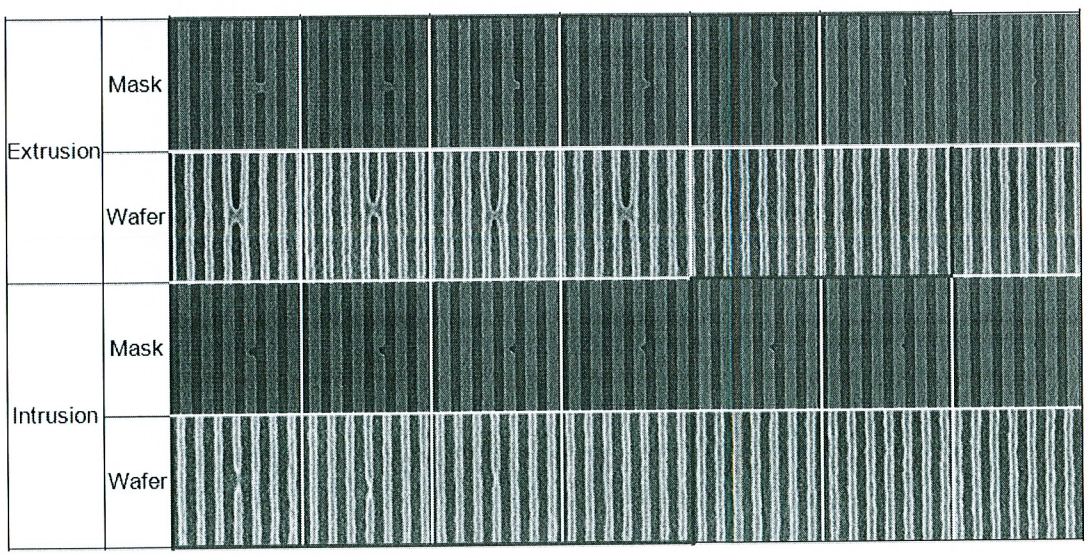


Figure 1. Mask SEM images and wafer SEM images for programmed defect at 30nm hp

3.2 Printability of native pattern defects at 30nm hp

Figure 2 shows mask SEM images of native pattern defects and wafer exposure results. In case of native pattern defects, about 63nm defect in the mask can be printed. It is less printable compared to program defect. However, in real cases, practical defect size (height, volume), shape, and location are quite various and they strongly affect defect printability on a wafer. To verify defect printability without wafer review, an actinic review tool such as AIMS^{TM} is essential. So for the printable defect size, it is tentatively recommended to apply same baseline with programmed defect since database of native defects is not enough and programmed defects are more sensitive to printability.

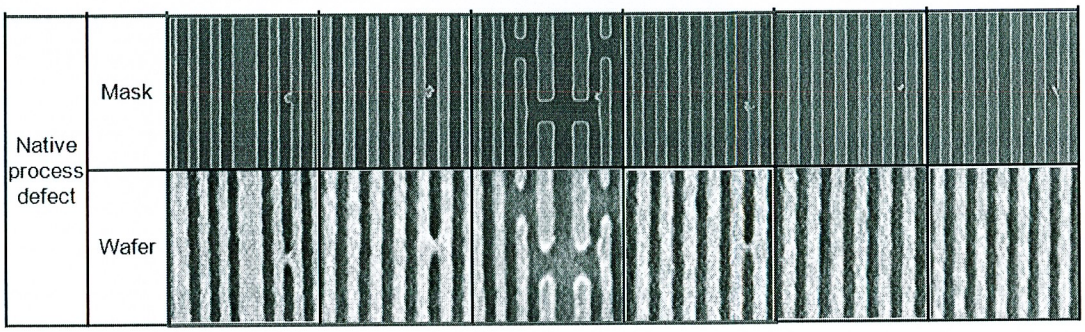


Figure 2. Mask SEM images and wafer SEM images for native pattern defect at 30nm hp

3.3 Defect printability down to 20nm hp by MET

Since current EUVL scanner and resist performances are not enough down to 20nm hp, MET with dipole condition was utilized for defect printability down to 20nm hp node. Considering image quality, results of wafer pattern can give vague boundaries of printability. Printable defects are about 45nm and about 65nm for extrusion and intrusion defects, respectively. It is thought that there might be some difference of lithography tool between MET and production tool. To give realistic criteria of printable defect, it needs to be evaluated in the EUV scanner after ensuring the resolution and the resist process. Nevertheless, results from MET are meaningful with the view of tempered criteria.

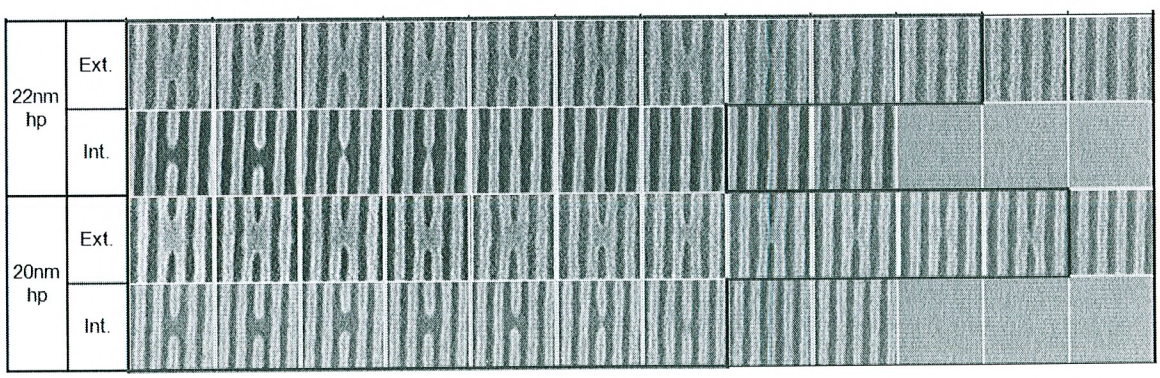
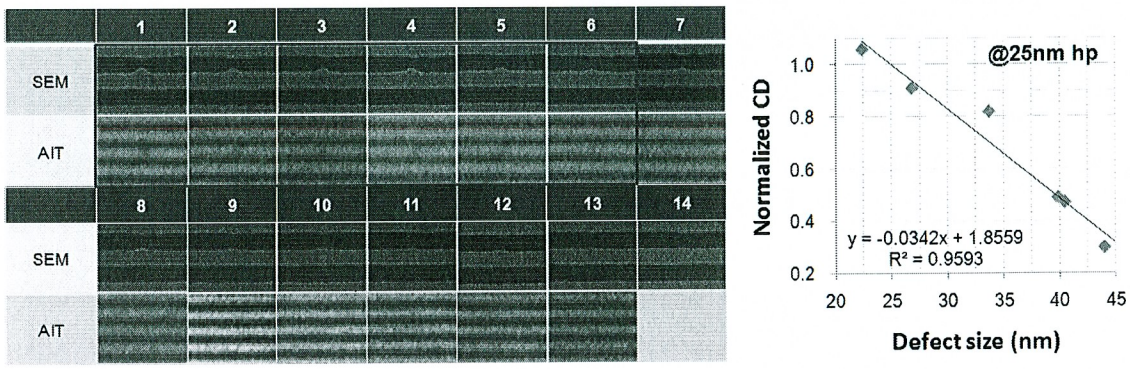


Figure 3. Wafer SEM images both 22nm hp and 20nm hp by MET

3.4 Pattern defect printability estimation by AIT

Since current AIT can cover 2x nm hp and supplement MET printability results, SEMATECH-Berkeley AIT was also used to evaluate defect printability at 2x nm hp. Figure 4(a) shows SEM images of program defects on the mask and their AIT images. Normalized CD measured from AIT images can give us printable defect sizes, as shown in Fig. 4(b). Figure 5 shows printable defect sizes obtained from AIT with two types of defect, extrusion and intrusion defects, and as a

function of hp nodes. Results both of 10% and 15% ΔCDs show higher sensitivity comparing to NXE3100. From the data of 30nm hp, we know that 20% of ΔCD meets the result of NXE3100. Minimum printable size is reduced a lot below 25nm hp. AIT results at 21nm hp are excessively lower than those of MET. It is thought that printable sizes from MET experiments are higher due to test conditions like illumination and resist process, but on the contrary AIT is more sensitive to defect printability since AIT does not reflect resist performance.



(a) (b)

Figure 4. Raw data from SEMATECH-Berkeley AIT: (a) Mask SEM images and AIT measurement images. (b) Normalized CD as a function of defect size on the mask

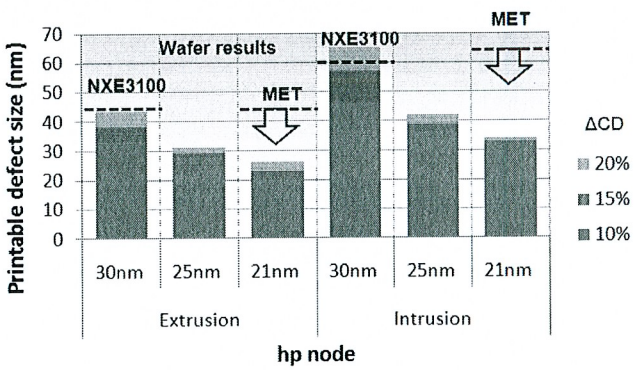


Figure 5. Printable defect size by AIT compared with both NXE3100 and MET

3.5 Pattern defect printability simulations

To evaluate printability of pattern defects from 30nm hp down to 16nm hp node, rigorous simulations using S-Litho were utilized. Two types of pattern defects, extrusion and intrusion, with various sizes were considered, as shown in Fig. 6. Corresponding ASML scanner conditions with NA of 0.33, different illumination in each node was applied in the simulations. Aerial image simulations are in good agreement with AIT results at 30nm hp comparing to Fig. 5. From the Fig. 6 printable defect size decreases by >30% from 30 to 25 nm hp node, but below 25nm hp, it does not decrease, rather it goes as far as to increase a little. As a result, we know that wafer printability of pattern defects strongly depends on illumination conditions in EUV scanner.

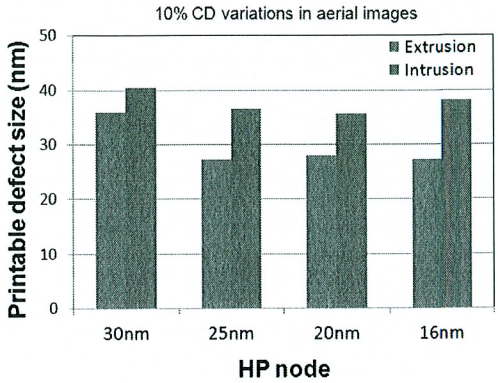
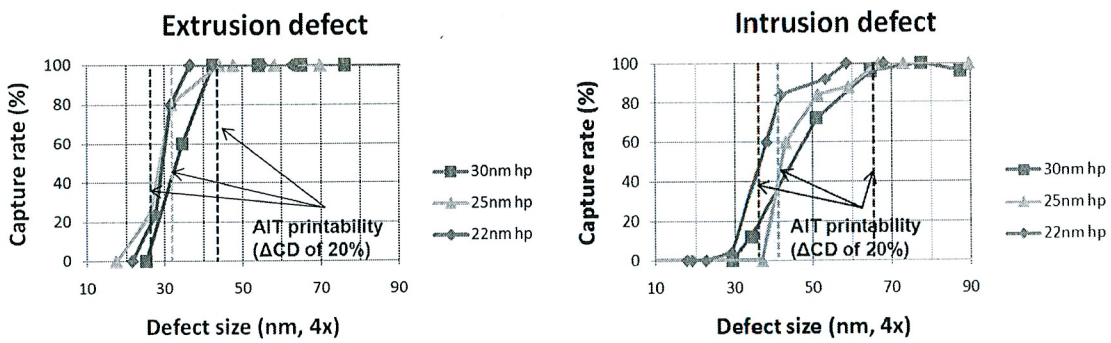


Figure 6. Printable defect size with both extrusion and intrusion defects simulated by S-Litho. Conventional for 30nm and 25nm hp, Quasar for 20nm hp, and dipole illumination for 16nm hp were applied.

3.6 Current status of defect inspection

In addition to printability studies through wafer exposure experiments, current status of inspection capability was assessed by pattern inspection. Along with exposure experiments, two types of pattern defects, extrusion and intrusion, were inspected, as shown in Fig. 7. From the inspection results, it is thought that current 193nm mask inspection tool could meet requirements of defect sensitivity in 30 and around 25nm hp node with capable improvement. But inspection sensitivity for low 20nm hp is not enough, even inspection below 20nm hp will be more difficult. Therefore actinic or e-beam inspection tool will be required for 20nm or below.



(a) (b)

Figure 7. Inspection results both (a) extrusion and (b) intrusion pattern defects of EUV mask as a function of hp node

3.7 Prospect for EUV mask infrastructure

Overall printable defect size at 30nm hp is 45nm and 60nm for extrusion and intrusion defects, respectively. Moving to about 25nm, it decreases a lot, and down to about 20nm, it decreases a little. Below 20nm, printable size does not decrease due to difference of illumination condition. With the criteria of printable defect size, current 193nm inspection tool is not enough below about 20nm hp. With introduction of upcoming 193nm tool, it is expected to improve than current performances. But, eventually, an actinic or an e-beam inspection tool is required for 1Xnm hp. Furthermore for the verification of both inspection and repair, a verification tool such as AIMS^{TM} is needed in HVM stage.

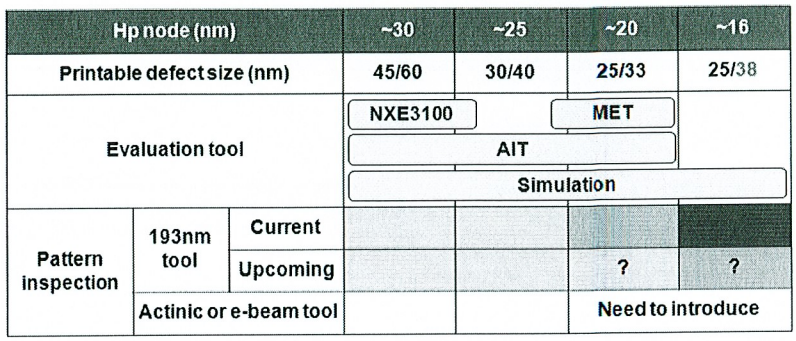


Figure 8. Roadmap of printable defect size and pattern inspection

4. CONCLUSION

In summary, printability studies of pattern defects as a function of hp nodes were evaluated, which were compared with inspection results. From the exposure test, practical value of printable defect size is to be 45nm and 60nm for extrusion and intrusion defects, respectively. Printable defect size decreases by >30% from 30 to 25 nm hp, and it does not decrease since below 25nm hp due to the different illumination condition in each hp node. AIT result at 30nm hp meet simulation, and also that of 20% ΔCD meets the result of NXE3100. Through the simulation, we know wafer printability of pattern defects depends on illumination conditions in EUV scanner. With the criteria of printable defect size obtained by NXE3100, MET, AIT, and simulation, current and upcoming 193nm pattern inspection tools could cover 30nm and 2x nm hp node printability results. For the further inspection below 1xnm hp, advanced pattern inspection tool such as actinic and e-beam inspection tool to enhance defect sensitivity might be required.

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This work was supported by the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.