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A MICROCOMPUTER BASED TEST SYSTEM FOR CHARGE COUPLED DEVICES

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Abstract

A microcomputer based system for testing analog charge coupled integrated circuits has been developed. It measures device performance for three parameters: dynamic range, baseline shift due to leakage current, and transfer efficiency. A companion board tester has also been developed. The software consists of a collection of BASIC and assembly language routines developed on the test system microcomputer.

Introduction

The Time Projection Chamber at the Stanford Positron-Electron Colliding Beam Accelerator requires about 17,000 channels of data acquisition running at a 10 MHz data rate (17,000 channels, each sampled every 100 ns). This high data rate is made possible by the use of analog charge coupled integrated circuits (CCDs), and a sophisticated trigger system. The CCDs are analog shift registers which sample input voltage every 100 ns. When the trigger system determines that an event has occurred, the CCD clock is slowed from 10 MHz to 20 KHz and the CCD output voltage is then digitized at the 50 μs slow clock rate. Although 17,000 A/Ds are still required, they need not be particularly fast or expensive. In large scale the TPC electronics resemble an analog version of a transient recorder, with the CCDs acting as an analog memory which can be read out at a convenient rate after an appropriate trigger.

System Considerations

Some form of automatic test system was required to accomplish the testing and sorting of 8500 CCDs in a reasonable time. The design goals were to duplicate as far as possible the operating conditions of the detector electronics, to minimize hardware costs, to permit the rapid reconfiguration of the test system (when work on the tester was begun two types of CCDs were under consideration), and to permit the use of semi-skilled personnel to operate the tester. A second system was designed to test the 1200 printed circuit boards used in this portion of the TPC after they had been loaded with CCDs. Commonality of hardware and software was, therefore, an additional goal.

System Configuration

The CCD test system consists of a PET* computer with 16 Kbytes of memory, a cassette recorder, a thermal printer, and an electronics bin. The bin is a standard 17 slot TPC system bin which houses five boards and is interfaced to the PET via the memory expansion bus. The board types are: PET to bin interface, programmable power DACs, clock generator and sync, A/D, and CCD driver/clock skew. Figure 1 shows the CCD driver/clock skew board.

The PET to bin interface, which resides in the 17th bin slot, decodes four of the address lines to produce a slot enable signal, and distributes four address lines to the other 16 bin slots. These four lines determine a slot subaddress. The system can therefore support 256, 8 bit registers; a maximum of 16 registers in each of 16 slots. Presently, 34 registers are used, distributed over four slots.

The programmable power DACs are used to supply bias voltages to the CCD, and to control CCD clock amplitude. There are four, 12 bit DACs on the board, each of which, with associated circuitry, can supply up to 1.5 amps at the full scale output of 20 volts. Sense resistors and differential amplifiers enable the current supplied by each of the power DACs to be monitored.

The clock generator is the heart of the system. It provides a programmable number of fast and slow clocks, a status signal to indicate either fast or slow clocks, and programmable sync pulses for pulse generation and A/D conversion. The slow clock frequency is programmable over a 15 bit range from 10 MHz to 304 Hz. The fast clock frequency is programmable over a 3 bit range from 10 MHz to 1.4 MHz. The number of fast or slow clocks is individually programmable from 2 to 4095 clock pulses. Both types of sync pulses are programmable from 2 to 4095 clocks.

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The clock generator is a synchronous programmable divider which is loaded at each terminal count with either a fast or slow count value depending on the terminal count state of either the slow or fast clock counter and the state of the mode control flip-flops. There are three possible modes: fast clocks only, slow clocks only, and alternating fast and slow clocks. The alternating mode is the one used to test devices. Due to the overall synchronous nature of this board, there are no glitches or discontinuities when switching from one clock frequency to the other.

The A/D board, on command from the PET, synchronizes with the first slow clock and then digitizes each of the 455 buckets in the CCD at each slow clock pulse. The A/D is an Analog Devices AD571*, which is a 10 bit device with a 25 μs typical conversion time. The convert command is the leading edge of the slow clock delayed by a one-shot to occur in the middle of the slow clock time. The A/D end of conversion signal is used to save the A/D output in a latch and to trigger a non-maskable interrupt sequence in the PET. The interrupt service routine reads the value stored in the latch and stores it in an array in memory. To maintain 10 bit accuracy two read operations must be performed for each datum. This double read requires that the slow clock not exceed 15 KHz to avoid dropping data. The slow clock is set to 10 KHz for the test.

The A/D board is used in one of two gain modes: unity gain or high gain (gain = 50). The unity gain is used in the dynamic range and transfer efficiency tests where the voltages are in the range of 2 to 10 volts. The high gain mode is used in the leakage current baseline shift test to expand the 100 mV range to a more usable 5V range. In both modes a 12 bit DAC is used to offset the analog input into a favorable portion of the A/D input range.

The CCD driver clock skew board accepts the clock from the clock generation board and produces two clocks for use by the CCD: sample clock and transport clock. Both of these clocks are programmable in width and separation in 5 ns steps. This programmability is accomplished with two tapped delay lines and a collection of ECL line receivers, multiplexors, and flip-flops. The resulting clocks are translated up to a ground referenced positive 14 volt swing for use by the CCD.

The pulse in the transfer efficiency test is generated by using one of the sync pulses produced by the clock generator board to chop a DAC defined level. The outputs of two DACs are summed at the inverting node of a high speed op-amp. One of the DACs establishes the CCD input bias level. The other DAC, chopped by a CMOS switch, provides a pulse whose baseline is the bias voltage set by the first DAC.

CCD Test Parameters

Three device parameters are measured. They are: dynamic range, baseline shift due to leakage current and charge injection, and transfer efficiency.

The dynamic range test measures CCD output voltage for 42 values of input voltage and determines the input knee, that is, where the device just enters its active region, as well as the corresponding value of output voltage for that input operating point, and the effective range of the device at the input. Devices are sorted according to input knee voltage for use on the CCD boards.

The leakage current baseline shift test checks each of the 455 buckets in the CCD for conformance to a straight line and for glitches. When a CCD has its clock frequency changed from fast to slow, the dwell time for each bucket of electrons is no longer the same. For example, the 454th bucket at the instant of frequency change will have been in the device for 454 x 100 ns + 100 μs before it gets read out, while the first bucket of electrons will have been in the device 454 x 100 μs + 100 ns before it gets read out. Assuming a constant rate of leakage into each bucket, the baseline will shift and will normally appear as a straight line at the output whose slope is the rate of leakage into each bucket. Defects in the device can cause local charge injection, which show up as glitches at the output. Figure 2 is a scope photo taken at the input of the A/D illustrating the use of the high gain mode to expand the scale around the region of interest. This particular device (not representative of devices in general) has two glitches, one between the third and fourth division, and one between the sixth and seventh. The baseline shift is also clearly shown, being about 20 mV (5 vertical divisions at 0.2V/DIV, divided by the scale factor of 50).

The tester also supplies a fast pulse of known amplitude for the transfer efficiency test. Transfer efficiency is the ability of each bucket to transfer a given amount of charge in each clock cycle. Poor transfer efficiency will cause the packet of charge to be spread across several buckets instead of just one, and will result in an output pulse whose edges are spread across several buckets in staircase fashion.

Most of the code is written in BASIC, with the data collection and signal averaging routines written in machine language. The machine language segments were written with the aid of an assembler, written in BASIC, running on the PET. A complete test for a device takes one minute and forty five seconds. Most of this time is spent checking each of the 455 analog buckets for both sides of the device during the leakage current test. A device consists of two

separate 455 bucket shift registers. Figure 3 is an example of device tester printout, along with a graph of the input/output characteristics of that device. Figure 4 is an example of typical good and bad device printouts.

Board Tester

The board tester is almost identical electrically and mechanically to the device tester and uses the same data collection algorithms. The power DAC board is not used and a spare bin slot is wired to accept the CCD clocks and to carry the 16 analog outputs from the 8 CCDs over to the A/D slot.

The board tester is used to perform go/no go testing, to calculate resistor values to equalize channel offsets, and to aid in the centering of these offsets at a desired value. Some simple checks are also made to weed out certain types of device defects which may have escaped the device tester.

The go/no go test applies a pulse at a board test input (all 16 inputs are pulsed) and checks transfer efficiency. Failures here are of two types: dead channels and poor transfer efficiency.

The offset equalization routine calculates the average of all 16 outputs with no input applied, and then calculates the appropriate value of offset resistor, in standard 5% steps, to bring each channel output to that average. A check is made here for CCDs with excessive offset. This check finds devices which, through human error, have been loaded onto a board set up for CCDs at a different operating point. Figure 5 is an example of printout for the offset equalization routine.

The channel offset centering routine averages all 16 board outputs as before, displays that average on the screen, and tells the test operator to turn the offset adjustment pot either clockwise or counter-clockwise until the board is adjusted to the correct value of offset. Figure 6 is an example of printout for the channel offset centering routine.

Reliability

Operating experience, accumulated over the last 18 months has been good. One system has never failed, and the other has failed twice; once due to a large clot of conductive dust shorting out some pins, and once due a RAM which suddenly developed a hard error. (The systems are installed in a shop area.) The least reliable system components have been the printers. Correlation between the testers and CCD system performance in TPC is good. The vast majority of returned boards are those which have been mechanically damaged in transit or handling.

System Enhancement

There are no present plans to upgrade either test system; however, there are at least two enhancements which should be considered for future systems of this general type. The first and most obvious improvement would be to recode the test program entirely in machine language, using the floating point routines which are stored in PET ROM to perform the calculations. A second worthwhile change would be the addition of a rapid reload capability. Presently, the PET is loaded through the cassette tape player, which takes about five minutes to load the test program. A rapid reload feature would permit instant recovery after power line induced crashes, and would also permit one computer to control more than one bin, although not necessarily simultaneously. A problem encountered with any computer of this type is that detailed documentation is difficult to obtain, and that deciphering the innermost workings of the machine and its operating system could consume inordinate amounts of time.

Conclusion

In summary, it is possible to build sophisticated test systems with relatively cheap hardware and acceptably short software development times. The most important factors are a clear understanding of the problem to be solved and an interactive approach to hardware and software development.

Disclaimer

*References to a company or product name do not imply approval or recommendation of the product by the University to California or the United States Department of Energy to the exclusion of others that may be suitable.

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2. Fairchild Semiconductor, TTL Application Handbook, August 1972, pp. 9-17 to 9-29.

3. PET User's Manual.

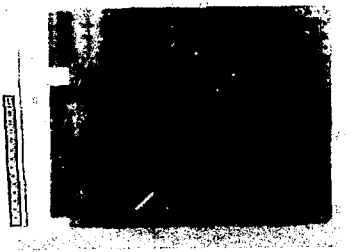

FIGURE 1 CCD DRIVER

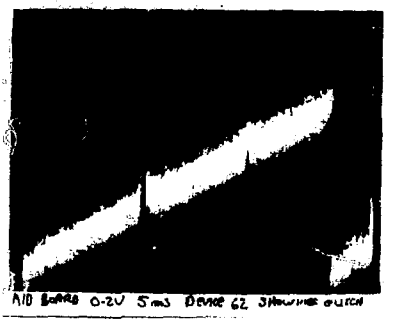

FIGURE 2

BASELINE SHIFT

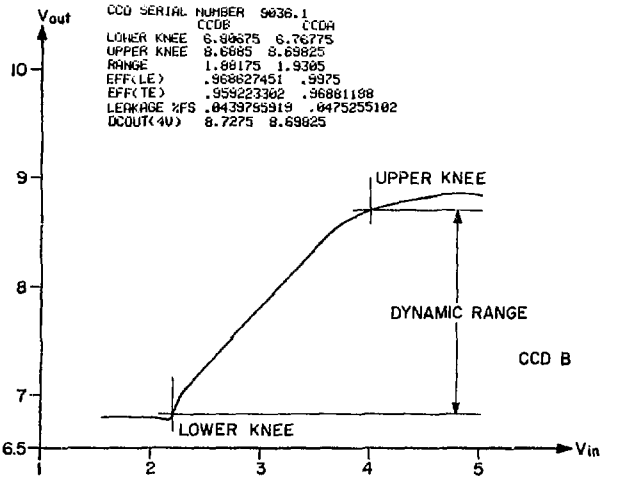

FIGURE 3

FIGURE 4

```
CCD SERIAL NUMBER  5918
GLITCH AT BUCKET  23
 .0156663633 VOLTS
              CCDB          CCDA
LOWER KNEE  6.65075  6.67025
UPPER KNEE  8.93225  8.97125
RANGE       2.2815  2.301
EFF(LE)     .95  .958482144
EFF(TE)     .941517856  .95
LEAKAGE %FS .0232653661  .0259183074
DCOUT(4V)   8.87375  8.91275
OUTPUT OFFSET B-A -.0389999971

 4.1 B 8.93225  .0389999971
```

BAD DEVICE

```
CCD SERIAL NUMBER  5851
              CCDB          CCDA
LOWER KNEE  6.61175  6.59225
UPPER KNEE  9.08825  9.02
RANGE       2.4765  2.42775
EFF(LE)     .974568967  .983043479
EFF(TE)     .958189656  .95
LEAKAGE %FS .0228826531  .0254591837
DCOUT(4V)   9.0395  8.95175
OUTPUT OFFSET B-A  .0682500005

 4.1 A 9.08825  .0682500005
```

GOOD DEVICE

```
BOARD# 605
PASSED PULSE TEST
 R4= 1960
BIAS VOLTAGE=  3
 CHANNEL  0 OUTPUT= 1.3 VOLTS
 CHANNEL  1 OUTPUT= 1.04 VOLTS
 CHANNEL  2 OUTPUT= 1.1 VOLTS
 CHANNEL  3 OUTPUT= 1.27 VOLTS
 CHANNEL  4 OUTPUT= 1.36 VOLTS
 CHANNEL  5 OUTPUT= 1.16 VOLTS
 CHANNEL  6 OUTPUT= 1.29 VOLTS
 CHANNEL  7 OUTPUT= 1.25 VOLTS
 CHANNEL  8 OUTPUT= 1.34 VOLTS
 CHANNEL  9 OUTPUT= 1.32 VOLTS
 CHANNEL 10 OUTPUT= 1.81 VOLTS
 CHANNEL 11 OUTPUT= 1.53 VOLTS
 CHANNEL 12 OUTPUT= 1.99 VOLTS
 CHANNEL 13 OUTPUT= 1.12 VOLTS
 CHANNEL 14 OUTPUT= 1.47 VOLTS
 CHANNEL 15 OUTPUT= 1.51 VOLTS
 1ST AVG= 1.37178125
 CHANNEL     R43
  1           43

  2           47

  4           68

  5           51

  7           56

  8           68

  10          100

  11          82

  12          120

  13          51

  14          75

  15          82

HAVE THE RESISTORS CHANGED
AS INDICATED ABOVE
ATTACH PRINTOUT TO BOARD
END OF TEST
```

OFFSET EQUALIZATION
FIGURE 5

```
BOARD# 530
PASSED PULSE TEST
 R4= 2370
 BIAS VOLTAGE=  3.03
 CHANNEL  0 OUTPUT= .222 VOLTS
 CHANNEL  1 OUTPUT= .232 VOLTS
 CHANNEL  2 OUTPUT= .271 VOLTS
 CHANNEL  3 OUTPUT= .251 VOLTS
 CHANNEL  4 OUTPUT= .251 VOLTS
 CHANNEL  5 OUTPUT= .261 VOLTS
 CHANNEL  6 OUTPUT= .261 VOLTS
 CHANNEL  7 OUTPUT= .251 VOLTS
 CHANNEL  8 OUTPUT= .271 VOLTS
 CHANNEL  9 OUTPUT= .261 VOLTS
 CHANNEL 10 OUTPUT= .261 VOLTS
 CHANNEL 11 OUTPUT= .222 VOLTS
 CHANNEL 12 OUTPUT= .222 VOLTS
 CHANNEL 13 OUTPUT= .28 VOLTS
 CHANNEL 14 OUTPUT= .261 VOLTS
 CHANNEL 15 OUTPUT= .271 VOLTS
 1ST AVG= .253578124

 CHANNEL  0 OUTPUT= .271 VOLTS
 CHANNEL  1 OUTPUT= .271 VOLTS
 CHANNEL  2 OUTPUT= .31 VOLTS
 CHANNEL  3 OUTPUT= .3 VOLTS
 CHANNEL  4 OUTPUT= .29 VOLTS
 CHANNEL  5 OUTPUT= .3 VOLTS
 CHANNEL  6 OUTPUT= .3 VOLTS
 CHANNEL  7 OUTPUT= .29 VOLTS
 CHANNEL  8 OUTPUT= .32 VOLTS
 CHANNEL  9 OUTPUT= .29 VOLTS
 CHANNEL 10 OUTPUT= .3 VOLTS
 CHANNEL 11 OUTPUT= .261 VOLTS
 CHANNEL 12 OUTPUT= .261 VOLTS
 CHANNEL 13 OUTPUT= .328 VOLTS
 CHANNEL 14 OUTPUT= .31 VOLTS
 CHANNEL 15 OUTPUT= .32 VOLTS
 MEAN= .295625
 PASSED PULSE TEST
```

CHANNEL OFFSET CENTERING
FIGURE 6