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Abstract

Pulsed transistor reset of high resolution charge sensitive preamplifiers used in cooled semiconductor spectrometers can sometimes have an advantage over pulsed light reset systems. Several versions of transistor reset spectrometers using both silicon and germanium detectors have been built. This paper discusses the advantages of the transistor reset system and illustrates several configurations of the packages used for the FET and reset transistor. It also describes the preamplifer circuit and shows the performance of the spectrometer at high rates.

Introduction

The development of the pulsed-light reset method applied to charge-sensitive preamplifiers[1,2,3,5] resulted in the excellent energy resolution that has been exploited particularly in semiconductor detector X-ray fluorescence spectrometers. A number of limitations were apparent to us in the early development of the method but the fact that pulsed-light feedback via the drain-gate diode of the input FET gives the absolute minimum input capacitance and results in the best possible energy resolution outweighed all other considerations. This is still the case in many applications but the growth of other applications in our programs has led us to resume an earlier investigation[4] of other pulsed reset methods.[6] In many of our programs the detector capacitance is much larger (often 20 pF or greater) than is common in X-ray spectrometers (~ 1 pF) and the small added capacitance resulting from a reset element connected directly to the gate of the FET is quite tolerable in return for the advantages gained over the pulsed-light reset method.

The potential advantages of the pulsed reset method discussed here over the pulsed light reset method include the following:

(i) Pulsed light feedback via the drain-gate junction of an n-channel FET can only be used for one polarity of detector connection—namely where the n^+ face of the detector is connected to the gate of the FET and the negative detector bias is applied to the p^+ face of the detector. Either detector direction can be accommodated by the pulsed feedback method we will discuss. This can be a useful feature in some detector applications.

(ii) In pulsed light feedback systems it is not uncommon to observe after-effects following the pulsing of the reset light. These effects can exist for quite long times (often hundreds of microseconds) and they result in severe resolution degradation at high counting rates unless a long dead time is provided following a reset. Thus, while the basic reset operation may occupy only a few microseconds the system dead time is very much longer.

Several factors can contribute to these slow after-effects. Charge storage and diffusion from extraneous parts of FET's is one possible source of the problem. Light leakage onto the detector surface, which may change the charge state of the surface, is another source of the problem. This is particularly true in germanium detectors as they are very sensitive to the long wavelength light used in pulsed light reset systems. Despite these problems, the best ultimate resolution is obtained in pulsed light reset systems and with great care excellent rate performance can be achieved.[5]

These after-effects are virtually absent in the reset systems to be discussed. Consequently, fast recovery from resets and excellent high counting rate performance can be achieved.

(iii) The light output of the LED used in pulsed light reset systems, the light coupling to the FET and the sensitivity of the FET to light are all rather poorly controlled quantities. This means that the speed of the reset is quite variable from unit to unit. The method to be discussed does not have these problems.

(iv) The high pulsed current (as much as 100 mA) used to drive the LED in pulsed light reset systems may (and in general does) cause serious crosstalk problems in multiple detector spectrometer systems. The crosstalk is primarily due to signals produced in the common ground at the front end. The pulsed reset systems discussed here involved switching only minute currents and crosstalk problems are negligible.

We have found the technique to be discussed useful in a broad range of applications where one or more of the advantages cited earlier are important. In general the detectors used in these applications have moderate or high capacity and the small added capacity due to the reset element is negligible. However, as will be seen later the added capacity can be made very small (< 0.4 pF) and the added noise due to the reset element can be virtually zero. Consequently we are also using the method in some high-resolution X-ray spectrometers containing multiple low capacity detectors where crosstalk, high rate performance and outstanding overload performance are important.

An example of the need for an alternative to the pulsed-light reset system was a 4-detector large area Ge planar array used in an X-ray astronomy balloon experiment. Practical reasons involved in the design of the array resulted in the requirement that the detectors employ positive bias with the p^+ face of the detectors being connected to the gate of the FET. As pointed out earlier, pulsed-light reset via the drain-gate of the n-channel input FET cannot cope with this situation. The need for excellent resolution (for such large area detectors) at low energies led us to eliminate consideration of resistor feedback and to consider reset methods other than the pulsed light.

The initial design chosen for this system was based on the use of an extra FET which pulsed a recharge current into the input of the main FET. However, the technique used in this system depended on rather precise setting of the reset FET conditions. It involved presetting the bias conditions for different reset FET's and, furthermore, the circuit would only work satisfactorily when the detector system reached thermal equilibrium. These problems led to the idea of using a reset transistor (rather than an FET) and to a search for suitable low-capacity low-noise transistors. The development of the circuit described in the next sections is predicated on the use of such transistors.

Feedback-Controlled Reset System

At the same time as developing a transistor reset method to replace pulsed-light feedback in some applications, we realized that a well-controlled reset could be achieved by using feedback to control the reset phase of operation of the preamplifier. Figure 1 shows a simplified block diagram of the design used to achieve this. In this particular implementation of the circuit the detector is connected in its normal direction (negative high voltage) and a p-n-p transistor is used for the reset transistor. For the reversed detector polarity an n-p-n reset transistor would be used and the circuit changed accordingly.

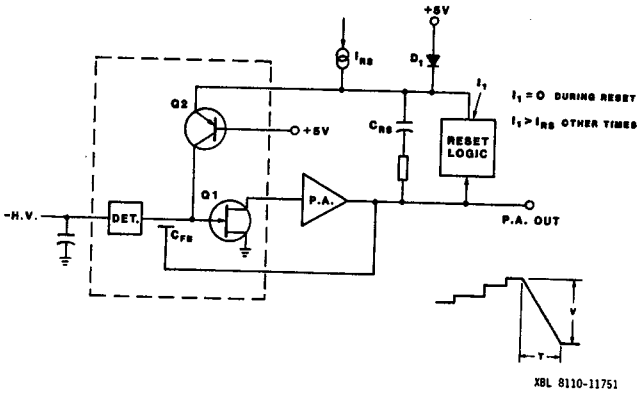

Fig. 1 Block diagram of feedback-controlled transistor reset system.

Referring to Fig. 1, the operation can be broken down into normal counting phase and a short reset phase. During the normal counting phase, detector signals and detector leakage cause the output of the preamplifier to move in a positive direction and the reset logic causes the current $I_1 (I_1 > I_{RS})$ to clamp the emitter of the reset transistor Q2 (via diode D_1) one diode drop below the +5 V line. Therefore, Q2 is non-conducting during this phase. It is important that the base and emitter of Q2 be free of noise and hum since such noise may couple via the collector (base + emitter) capacitance of Q2 to be input gate of Q1. When the preamplifier output reaches a predetermined level the reset logic turns off the current I_1 so that I_{RS} can flow into capacitor C_{RS} and raise the emitter potential of Q2. After a very short delay Q2 comes into conduction and the capacitor C_{RS} effectively becomes a feedback capacitor around the preamplifier gain stage. A small fraction of the current I_{RS} flows through Q_2 restoring the charge on C_{FB}, but nearly all of I_{RS} flows into C_{RS} and the preamplifier output moves in a negative direction at a rate given approximately by $dV/dt = I_{RS}/C_{RS}$. When the output voltage has dropped by a voltage V the reset logic switches the circuit back into its normal counting mode. The reset time is given by:

$$T_{RESET} = C_{RS} \cdot V/I_{RS}$$

It is important to note that the current gain requirements on Q2 are not severe and the drop in current gain (α) that occurs in such transistors at liquid nitrogen temperature can be tolerated. The important requirements on Q2 are its low collector-base capacitance, low collector leakage and low noise in the collector-base junction.

With the value of I_{RS} (~ 50 μA) used in our circuit the initial delay before Q2 comes into conduction after the reset mode is initiated is less than 1 μs. Another potential problem in the circuit is caused by stray capacitance coupling from the emitter of Q2 to the input circuit. At the end of the reset phase, when the current I_1 resumes, the emitter potential of Q2 falls rapidly by a small amount (this must be sufficient to stop conduction in Q2). Coupling of this voltage step into the input circuit would cause a positive step at the preamplifier output at the end of the reset phase. In the circuit actually employed this is compensated by feeding a small positive step at this time to the base of Q2 ; this step couples into the input circuit via the base-collector capacitance of Q2.

Detailed Circuit Description

Several circuits have been used in the pulsed transistor reset configuration. A complete schematic of the most complex of these preamplifiers is shown in Fig. 2. It contains three basic parts:

a) The cryostat electronics and filter box
b) The linear board
c) The logic board

which are now described below:

a) Cryostat electronics and filter box. The cryostat contains the semiconductor detector cooled to 77°K directly connected to the FET and reset transistor which are mounted in a common package. In some applications a heater, mounted onto the FET reset transistor package, is used to hold the temperature of the package at the optimum FET temperature, approximately 50°C warmer than the detector. In other applications the thermal resistance from the FET-reset transistor package to the cold finger is chosen to maintain the FET at its optimum temperature; the FET power then acts as the heater element. A temperature measuring diode (standard switching diode) is sometimes used to provide the capability to simply monitor the temperature of the detector mount. The other side of the detector connects to the high voltage filter network through a wire providing a large thermal resistance and through the high voltage feedthrough. The test pulser input is connected to the low voltage side of the final filter capacitor; it uses the detector capacitance as a test capacitor. This is useful for characterizing the detector depletion characteristics when required.

b) Linear Board. The linear board is exactly the same as we use in a pulsed light preamplifier.[5] It completes a charge-sensitive loop that includes the input FET contained in the cryostat. A bipolar output with current overload protection is provided.

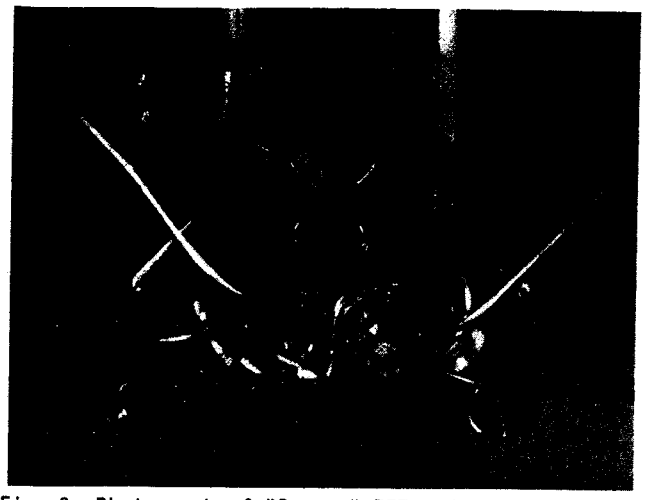

Fig. 3 Photograph of "In-can" FET and Reset Transistor Mount

Figure 3 shows a photograph of a 2N6453 FET and BF272A reset transistor in their original cans mounted in a common block of aluminum. Three of these units are used in a common cryostat. Each channel will have a large high purity N type coaxial detector. They will be used in an exotic atom experiment. The package mounts by means of a thin wall stainless steel tube heat leak which goes through the open hole in the aluminum block and connects to the coldfinger of the cryostat. A heater (current diode) mounted toward the mount end of the tube is used to heat the FET to the optimum temperature (about 50°C above liquid nitrogen temperature).

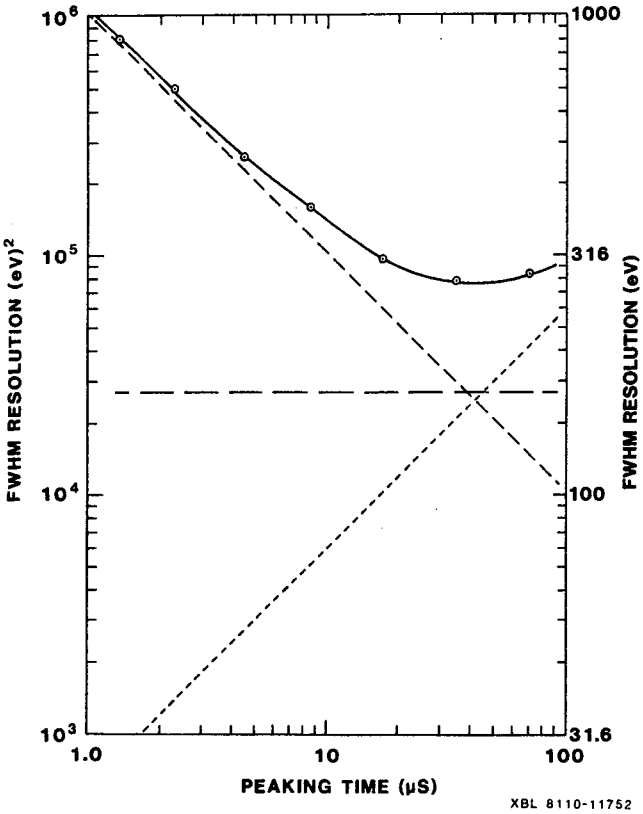

Fig. 4 Plot of (energy resolution)^2 versus peaking time of the main amplifier for a 10 pF Ge detector and 2N6453 FET.

Figure 4 shows a log-log plot of the FWHM electronic resolution squared versus the peaking time of one channel of the three detector system. The test detector is a 10 pF Ge planar. The plot contains the measured points, the best 3-component least-squares fit drawn by a computer, and three noise components: series, parallel and 1/f. As expected, tests have shown that the parallel and 1/f noise can be reduced by removing the FET and transistor from the can and mounting them in a low loss mount, but this was not necessary for this system since the system was to be used at peaking times shorter than 10 μs. Energy resolution versus input rate tests were performed on this system using a CO^{57} source with a fixed input rate of 1 KHz and varying the rate of a CS^{137} source from 0 to 100 KHz. The main amplifier, pile-up rejector, base line restorer and biased amplifier were our 11x8481 P-6 amplifier system which is generally used with pulsed light reset systems. The amplifier had a peaking time of 9 μs. The gain of the amplifier was adjusted so that the CO^{57} gamma-ray lines produced full amplitude output pulses; therefore, the CS^{137} gamma-rays pulses substantially overloaded the amplifier resulting in a more stringent rate test. Total peak shift was ± 50 eV in the 122 KeV gamma-ray line. Table 1 shows the results of this test.

TABLE 1

CO^{57} Rate (KHz)	CS^{137} Rate (KHz)	122 KeV Line Resolution (ev)
1	0	605 ± 5
1	19	602 ± 5
1	49	609 ± 5
1	99	612 ± 5

In this system the crosstalk between channels was carefully checked. No detectable crosstalk was observed.

Figure 5 is a photograph of a mount with a "decanned" FET and reset transistor. This mount is used in several systems including a spectrometer containing 6 large area silicon detectors used for plutonium X-ray counting. The mount, made of boron nitride with teflon inserts, is mounted onto a thermal heat leak by the two 0-80 flat head screws. To reduce the use of liquid nitrogen in the six detector array, the heating of the FET package was accomplished by its own internal power. The FET gate and reset transistor collector leads are connected together on the top of the mount and they are connected to the detector. The feedback capacitor uses the dielectric of the mount and is the central wire of the five wires. The other four wires are the source and drain of the FET and the base and emitter of the reset transistor.

Figure 6 is a magnified view of the other side of the mount showing the U311 FET on its nail head (gate) and the BF272A transistor on its nail head (collector). The nail heads and the flying leads on the chips are the original ones as used in the can. The other ends of the flying leads are spot welded to Kovar wires clamped in the boron nitride.

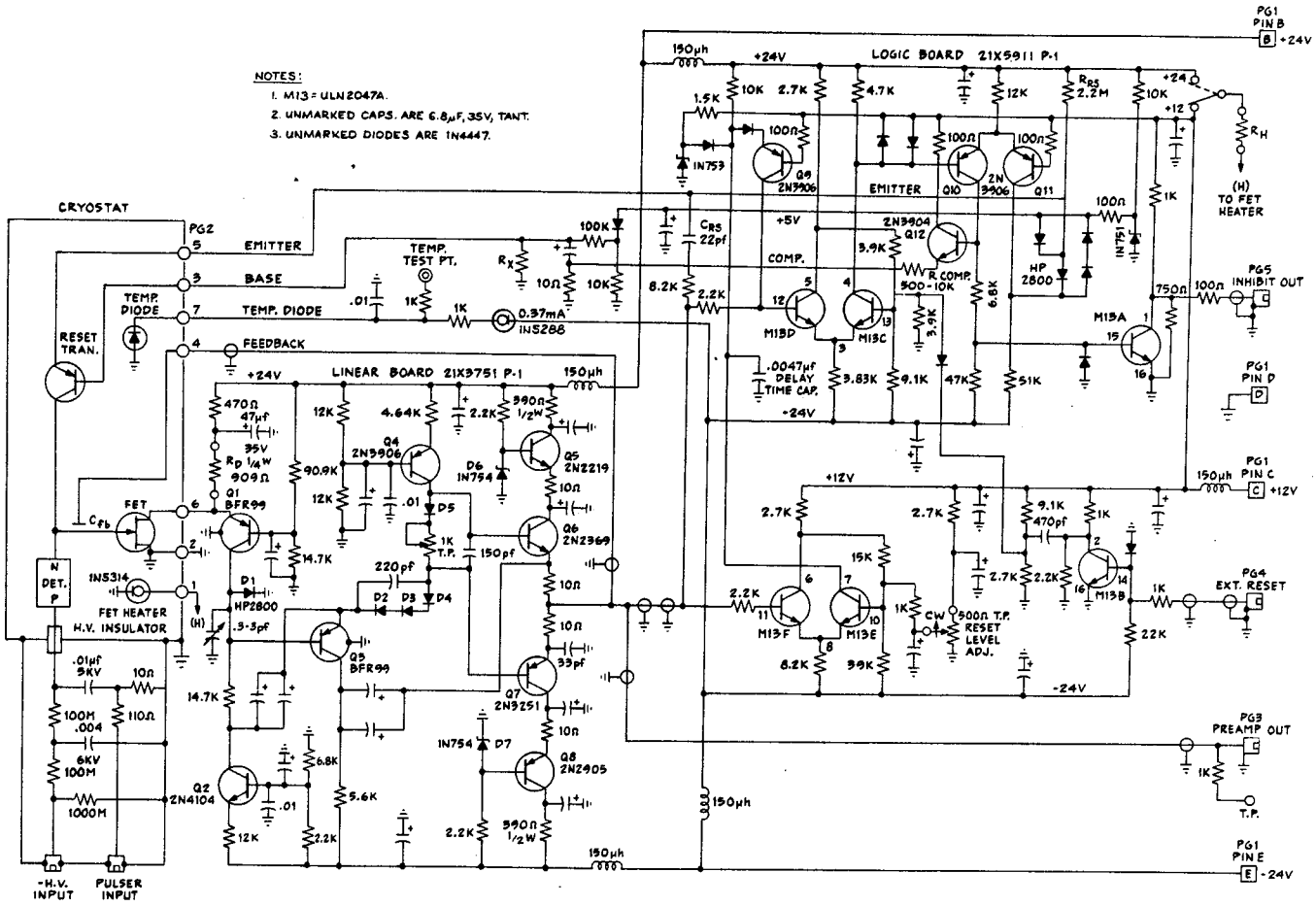

Fig. 2 Schematic Diagram of Transistor Reset Preamplifier

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This particular preamplifier is designed to have very fast rise time and to provide timing information when required. To achieve the fast rise time, low collector capacitance transistors are used for Q1 and Q3 and the collector capacitance of Q2 and Q3 are bootstrapped. These transistors are also chosen for their low noise properties. The 10% to 90% rise time is better than 5 ns when the loop contains a U311 FET, a 0.5 pF feedback capacitor, and a 15 pF detector.

c) Logic Board. The logic board contains two limit discriminators, a wait circuit, reset transistor driver and compensating circuit. It is designed to permit processing of the final event that triggers a reset and thereby to eliminate the energy dependent loses that would otherwise occur.[5]

The upper limit discriminator in Fig. 2 has a trigger threshold of +2 V and a hysteresis of 4 V. This discriminator turns on the reset transistor when the output of the linear stage exceeds +2 V and turns it off when the preamplifier output is more negative than -2 V. The lower discriminator in Fig. 2 is used to initiate a normal reset. It has an adjustable trigger level of 0 to +1.8 V. This is adjusted so that the voltage difference from this level to the upper discriminator level (+2 V) is greater than the step caused at the output of the preamplifier by the highest energy of interest. The output of the lower discriminator goes through a wait circuit (about 20 μs) before triggering the upper discriminator and causing the preamplifier to reset. The wait times (controlled by $C_{Delay\ Time}$) allows the linear amplifier to process the signal before causing a reset.

When a reset is initiated Q10 turns off causing an inhibit signal to be generated and causing the compensating emitter following Q12 to turn off producing a small negative step at the base of the reset transistor. At the same time Q11 is turned on and this unclamps the reset transistor emitter line. The current through the 2.2 M ohm resistor (R_{RS}) charges the capacitance on the emitter line and then turns on the reset transistor. The current in R_{RS} then flows into the 22 pF (C_{RS}) capacitor producing a negative ramp at the preamplifier output. When the output reaches -2 V the upper discriminator turns off the reset transistor and clamps its emitter again. The positive step produced at the base of the reset transistor at this time by the compensation emitter follower (Q12) is designed to cancel the charge coupled by stay capacitance from the emitter of the reset transistor into the FET input circuit.

FET and Reset Transistor Mounts

Several different types of FET and transistor mounts have been used for the transistor reset method. FET types 2N4416, 2N5397, U310, U311 and 2N6453, and transistors BF272A, BFR38, and 2N4957 have been used. In some cases, where the extra noise due to insulator losses could be tolerated, the transistor and FET were used in their original can; in more critical cases they were "decanned" and mounted in a low loss package.

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5. D.A. Landis, N.W. Madden, and F.S. Goulding, "Energy-Dependent Losses in Pulsed Feedback Preamplifiers", IEEE Trans. Nucl. Sci., NS-26, No. 1, 428 (1979).

6. V. Radeka, "Overload Recovery Circuit for Charge Amplifiers", IEEE Trans. Nucl. Sci., NS-17, No. 1, 269 (1970).

Fig. 5 Photograph of low loss mount for "decanned" FET and reset transistor.

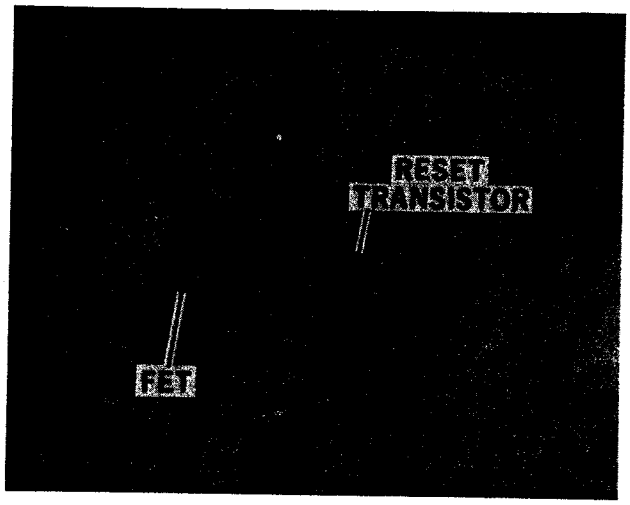

Fig. 6 Photograph of inside of low loss mount showing FET and reset transistor.

Application to High Resolution Low Capacitance Detector Spectrometers

According to its specifications, the reset transistor (BF272A) should add 0.3 pF to the gate lead of the FET. In order to assess the degradation due to the reset transistor, the resolution of a known good "decanned" 2N4416 was measured in a pulsed-light system with a silicon detector; a "decanned" transistor BF272A was then added and the system was remeasured as a pulsed transistor reset system. The results of the measurements are shown in Fig. 7. The increased series noise can be accounted for by an added input capacitance of 0.36 pF. The fact that the performance curves in this plot are almost parallel indicates that the main noise effect of the reset transistor is simply due to the added capacitance. Other minor deviations are within the errors in the computer fit. The added capacitance contributes about 6 eV to the electronic resolution at 35 μs peaking time and about 16 eV at 4.5 μs peaking time. In many practical systems (except for the very lowest X-ray energies) the degradation in energy resolution would not be significant.

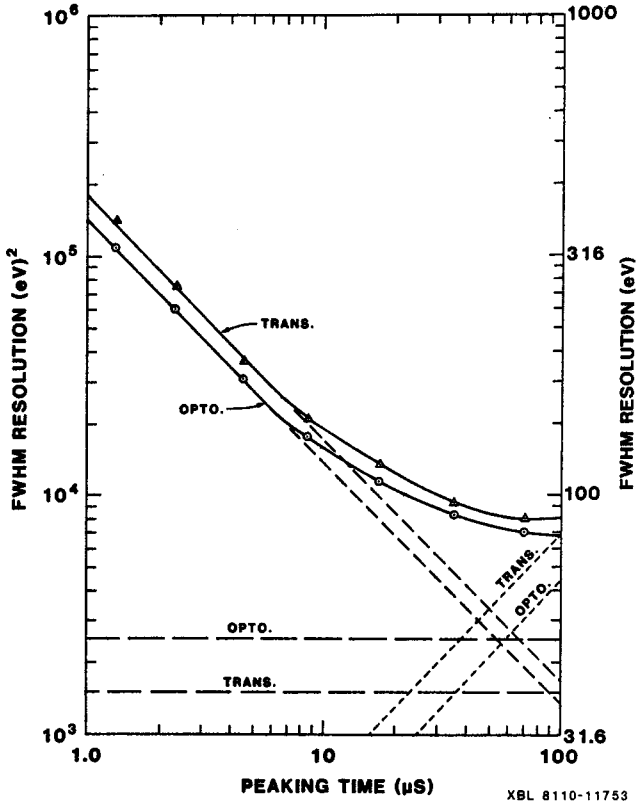

Fig. 7 Plot comparing energy resolution of pulsed opto system with transistor reset system.

Conclusion

We have demonstrated that the transistor reset system described in this paper represents a good approach in many spectrometers and particularly in high resolution multidetector arrays used at high counting rates.

Acknowledgments

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