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THE STRUCTURE AND PROPERTIES OF WSi_2 THIN FILMS FOR MOS DEVICES

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(M.S. thesis)

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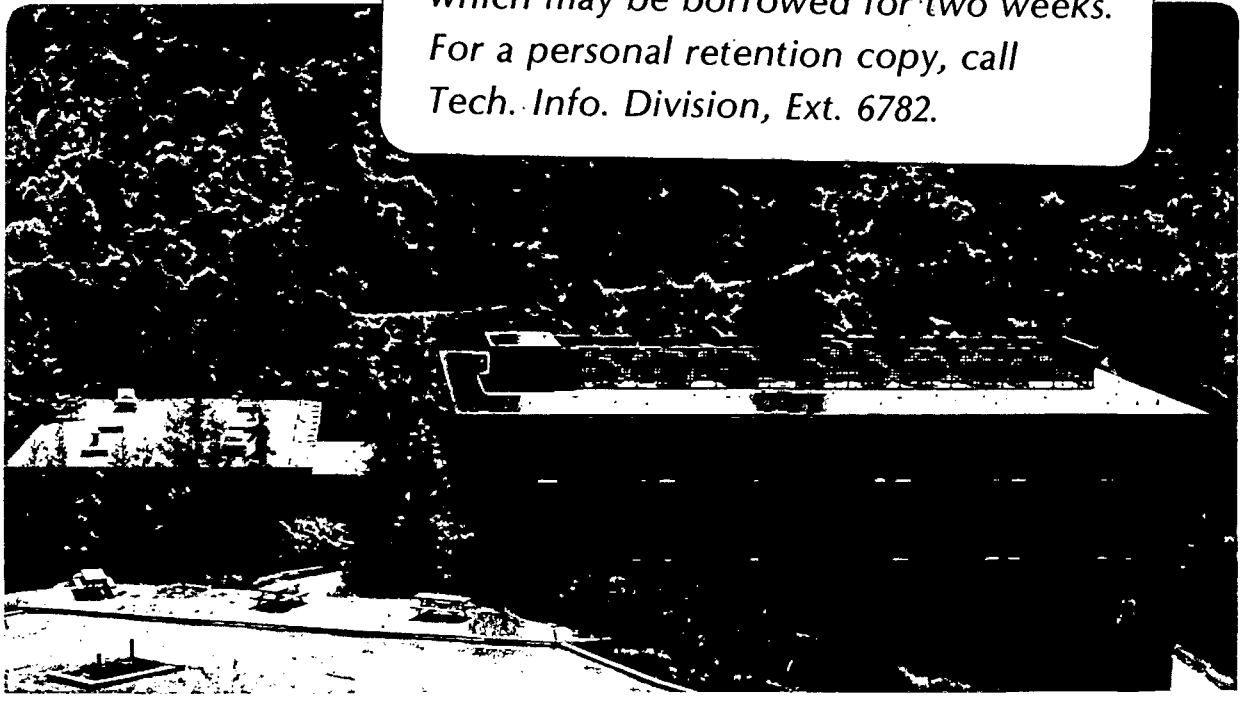

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Errata to LBL 14621

This report dealing with tungsten silicide did not properly reference previous work on this subject, specifically the articles in J. Appl. Phys. 52(8), 5350-5355 (1981); J. Electrochem. Soc. 127(2), 453 (1980); ibid. 128(10), 2211 (1981) from which much of the background and all of the data shown in Figs. 7, 10, 13 and 16 were taken directly. The author (Li-kuo Wu) is grateful to M. Pierre Beaufrère, Corbeil, France for drawing attention to these omissions which are deeply regretted.

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M.S. Thesis

June, 1982

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ABSTRACT

Polycrystalline silicon has long been used as the gate and interconnection material in metal-oxide-semiconductor field-effect transistor (MOSFET) integrated circuits, but as the device dimensions are shrinking and circuits are growing larger, the relatively poor conductivity of poly-Si is limiting its performance. As an alternative, tungsten silicide on poly-Si is being considered. No research has yet been reported on the microstructure-properties of this system. In the present research, therefore, the annealing behaviors of coevaporated WSi_2 on p-doped poly-Si has been studied by X-ray diffraction, He^+ - backscattering, transmission electron microscopy (TEM), and Auger/SIMS analysis. High temperature annealing of silicide results in crystallization of what appears to be amorphous layers of tungsten silicide as well as diffusion of phosphorous out of the poly-Si. An attempt is made to correlate the physical and chemical properties with device fabrication, and performance.

I. INTRODUCTION

Since the development of the first integrated circuit (IC), there has been a progressive movement toward achieving higher levels of integration. Moore[1] reported that the number of elements on a chip have doubled each year, and the production of such complex chips is continuing.[2] It is now possible to place thousands of logic circuits or tens of thousands of memory bits on a single chip, with an accompanying reduction in cost of circuits and an increase in the functions they perform. Therefore, it is important to realize the design problems encountered, particularly the serious limitations of interconnection lines on circuit performance for VLSI and the materials problems involved. It has been shown[3] that average delay time (T) for transmission of signal can be written as:

$$T = T_0 M \quad \ldots \qquad (1)$$

where

$T_0 \sim \rho \varepsilon_0 \varepsilon_{ox}$

$M \sim A/\lambda^2$

ρ = resistivity of electrode material

ε_0 = permittive of free space

ε_{ox} = oxide relative permittive

A = chip area

λ = maximum feature size

The value of T_0 is a purely physical measure determined by the electrode material and the property of its surrounding ambient material (SiO_2); on the other hand, M is a measure of the technology and number of components on the chip (bits of memory, logic gates). Because the

objective for improving IC fabrication technology is to pack more components on a single chip, the target is to increase the value of M; however, T_0 must be reduced to minimize T (Equation 1). This can be achieved by lowering electrode resistivity by the selection of low-resistance materials as the interconnection electrode.

A. Requirements for Electrode Materials

The basic demand is conductivity because it can substantially improve the resistances and delay times of the electrical interconnection lines used for VLSI structures. The need for a very large scale self-aligned MOS technology, however, sets the following limitations on low resistive materials.

A.1. High Temperature Process Compatibility

The electrode material must withstand the high temperatures encountered during integrated circuit processing and still retain its metallurgical integrity. This means that its melting point should be much higher than that attained in conventional processing temperatures.

A.2. Thermal Oxidation

The formation of an insulating layer on the top surface of the gate electrode and interconnection layer is necessary so as to isolate it from subsequently deposited conducting layers. Vapor-deposited SiO_2 and Si_3N_4 can be used for this application; however, thermally grown SiO_2 is generally of superior quality.

A.3. Chemical Resistance

The electrode material should not be affected by the chemicals required in the fabrication of ICs (H_2SO_4, HNO_3, HCl, HF). It must also be able to resist the common cleaning reagents for Si

(mixtures of $H_2SO_4 + H_2O_2$, $HCl + H_2O_2$, and $NH_4OH + H_2O_2$).

A.4. Stability to Final Metallization

Aluminum is widely used as the last layer to provide electrical interconnections in multilayer structures. The final step in the Al metallization process is to anneal the wafers at 400°C to 500°C which improves the ohmic contact of Al to Si, removes oxide damage caused during metal evaporation, and reduces the density of surface states at the oxide/silicon interface. The electrode material should be metallurgically compatible with Al at these sintering temperatures.

A.5. Small Grains

When a material with small grains is subjected to the high temperature process, grain growth may occur, and larger grains will cause difficulties in lithography and uniform etching of the material. It is evident, therefore, that the selected electrodes wherein grain growth is minimal and grain size is small, facilitate etching of submicron lines which is essential for higher packing density.

B. Selection of Electrode Material

Several commonly used electrode materials are compared to the metal silicon compounds (silicides) in Table I. Polysilicon is used widely for gates and interconnections; however, its inadequate properties are beginning to limit circuit performance, and its high resistivity degrades the speed of the circuits because of RC delay time. Although the grain size in as-deposited poly-Si can be very small, subsequent high temperature processing will increase it markedly[4] which causes problems in defining very fine lines.

Refractory metals (such as molybdenum and tungsten) fulfill most of the electrode requirements. They cannot withstand the high temperature oxidizing ambient in a conventional self-aligned technology, however, because their oxides are volatile. In addition, they cannot tolerate the chemical reagents applied for cleaning the wafers prior to processing.

Platinum silicide (PtSi) is less resistive, but it is limited in use to low temperatures because of its low melting point.

Titanium silicide ($TiSi_2$) is a potential candidate, but its solubility in HF solution is a disadvantage.

Tungsten silicide (WSi_2) meets all of the electrode material requirements, and its physical and chemical compatibility to IC fabrication processing is comparable to that of poly-Si. Because of their improved conductivity, these silicides appear to be the most likely selection.

C. Purpose of this Study

The objectives of this work are to carry out detailed studies on the annealing, etching, and oxidation properties of tungsten silicide deposited on poly-Si. Since annealing is one of the most important steps in the silicide processing, a proper understanding of WSi_2 annealing is necessary.

Tungsten silicide films of different compositions are studied by He^+ - backscattering X-ray diffraction. It is found that the stoichiometric WSi_2 film has the best characteristics for IC fabrication. The resistivity and grain size of WSi_2 are examined after annealing. A saturation-like behavior is observed. Finally, the P diffusion from poly-Si into WSi_2 films is measured by secondary ion mass spectroscopy

(SIMS). On the basis of these observations, the well-controlled annealing of silicide for device fabrication is shown to be possible. Chemical reagents commonly used for cleaning and etching, when used with WSi_2, showed behavior similar to poly-Si. Thermal oxidation of WSi_2 film in steam in the temperature range of 1000°C ~ 1200°C was performed and good quality SiO_2 was grown. The results of this work demonstrate the feasibility and advantages of applying WSi_2 to VLSI with extremely high density circuits.

II. EXPERIMENTAL PROCEDURES

The samples used in this study were from IC material prepared by P. Chang at Zilog, Inc., Cupertino, California. Tungsten and silicon were coevaporated onto LPCVD (low-pressure, chemical-vapor deposition) poly-Si film in a Sloan system equipped with two electron-beam evaporating units. In this study, a layer of 150 nm LPCVP poly-si was deposited on Si substrates with thin oxide to resemble the gate of MOSFETs (Figure 1). The poly-Si film was doped with $POCl_3$ deposition. Wafers were then cleaned and etched with buffered HF immediately prior to loading in the vacuum system. Tungsten silicide films of three different overall compositions (corresponding to the formulae: "$WSi_{2.3}$", "WSi_2", and "$WSi_{1.6}$") were evaporated. In order to obtain ~ 150 nm after high temperature annealing, .57 nm of W (on the crystal monitor in the evaporator) was used for all three different films. The amount of Si evaporated corresponds to thicknesses of 17.1, 14.3, and 11.4 nm, respectively (assuming theoretical density). The compositions of the films were controlled by both the evaporation rate and total thickness of W and Si. For the stoichiometric WSi_2 evaporation rates of Si .05 nm/s

and W 0.2 nm/s were controlled automatically through a feed back circuit. The Si-rich "$WSi_{2.3}$" and W-rich "$WSi_{1.6}$" film were obtained by changing the Si deposition rate accordingly. The films were deposited at a vacuum pressure of 4×10^{-6} torr on substrates that were not independently heated and were normally at room temperature.

Annealing of the silicides was performed in purified Ar or He ambient with O_2 and H_2O content less than 1 ppm.

Analytic techniques such as Rutherford backscattering (RBS), X-ray diffraction, transmission electron microscopy (TEM), and secondary ion mass spectroscopy (SIMS) were employed to study the material properties of the tungsten silicide films. RBS has traditionally been used for analyzing the chemical compositions near the surface region of thin films, whereas, SIMS has been used for studying the concentration profile of impurity elements up to microns of depth in thin films. Crystallinity of thin films can be characterized by TEM, electron and X-ray diffraction. Rutherford backscattering analysis was done with 2.3 MeV He^+ ions, the samples being tilted 7° in order to avoid channeling effects. The crystallographic structures of the films were investigated by X-ray diffraction methods. X-ray diffraction patterns were obtained with a Philips diffractometer equipped with a Cu tube and a post sample monochromator. Transmission electron micrographs of annealed WSi_2 films were taken with a Philip 301 transmission electron microscopy. The phosphorous distribution in the silicide was measured by secondary ion mass spectroscopy. The SIMS measurements were performed in a surface analysis system with 12 KeV O_2^+ as primary ions. A detailed description of this system is

provided elsewhere.[5] The concentration of P was obtained from $^{31}P/^{30}Si$ ratios. Samples of WSi_2 and poly-si implanted with known doses of P were also measured to establish standards for calibrating the P concentration in silicides. The resistivity of the film was measured by the use of a four-point probe. Oxidation thickness was determined by creating a step in the film by etching and then measuring the step height using a Taly-step height reader.

III. RESULTS AND DISCUSSION

Since the as-deposited films are prepared by simultaneous deposition of W and Si, the post-deposition annealing is essential prior to other device processing steps in order to obtain silicide, for example, cleaning, etching, oxidation, etc. Annealing of as-deposited films drastically affects the characteristics of these films. The major changes are crystallization, grain growth, grain sizes, composition, adherence, surface morphology, conductivity, and phosphorous distribution in silicides.

A. Structure, Crystallinity, Grain Size

The X-ray diffraction spectra analyses presented in Figure 2 and 3 are supplemented by the transmission electron microscope photographs presented in Figure 4. Both Figure 2 and 4 were obtained with samples close to the exact composition of WSi_2, however, Figure 3 was obtained with samples that were W-rich "$WSi_{1.6}$". The sequence of diffraction patterns obtained with a Si-rich "$WSi_{2.3}$" is the same as that obtained with the stoichiometic sample (Figure 2). In the X-ray diffraction patterns, results corresponding to the silicide films alone are complicated by effects due to the presence of the underlying poly-Si films as well

as the occasional presence of a diffraction line due to the (100) Si substrate. The substrate diffraction line at about 16.5°, whose appearance or absence depends on subtle changes in substrate orientation, is thought to correspond to the Bragg angle for (400) Si, and where it is present has been crossed on the two figures. The relatively sharp diffraction lines for polysilicon are indicated by arrows and the correct Miller indices on the top part of the two X-ray diffraction figures.

As-deposited films are essentially amorphous as evidenced by the electron diffraction pattern of Figure 4(a). The X-ray diffraction patterns for as-deposited samples are, as expected, almost totally featureless (e.g., Figure 2). After one hour annealing at 300°C, the X-ray diffraction patterns for the W disilicide films produced by co-evaporation do not show any significant change from the patterns for the as-deposited films. Figure 2 shows that after 30 minutes annealing at 450°C, the WSi_2 film has undergone considerable crystallization; Figure 3 shows that the "$WSi_{1.6}$" samples reach a similar degree of transformation after an anneal at 550°C. In both cases, the poorly defined diffraction peaks are indicative of a rather disorganized crystalline state, a small grain size, and high internal microstrains. The films can be said to crystallize between 300°c and approximately 500°c. As will be discussed briefly later on, the transformation in the W-rich films appears to be somewhat sluggish and thus requires slightly higher temperatures than the transformations in the stoichiometric or Si-rich films. The X-ray diffraction patterns after the anneals at 650°C (Figure 2) or 725°C (Figure 3) correspond to the well defined structure of WSi_2: tetragonal with a = 3.211 Å and c = 7.869 Å. By comparison,

one may notice that the patterns obtained with the samples annealed at low temperatures contain extra lines, such as the lines at approximately 13.3°, 20.8°, and 23°. It has been shown[7], in the case of WSi_2 films obtained by means of ion implantation through W films on Si substrates, that the diffraction patterns containing these lines are characteristic of an hitherto unreported hexagonal form of WSi_2 with a = 4.164 Å and c = 6.414 Å which, like the similar form of $MOSi_2$, is stable only at low temperatures. A similar behavior for WSi_2 films deposited via dc sputtering has also been briefly reported.[8] The estimated temperature for the transition from the hexagonal to the tetragonal structure of 550°-650°[7] is seen to be in quite good agreement with evidence presented in Figure 2 (625°C in this case). For the W-rich films (Figure 3) the transition temperature appears to be approximately 675°C, somewhat higher than for the stoichiometric films. This difference is thought to be related to adhesion problems discussed below. The X-ray diffraction patterns obtained after the high temperature anneals (Figure 2 and 3) are quite sharp, corresponding to relatively well ordered, low strain crystalline materials. More precise information can be derived from the TEM results, e.g., as in Figure 4. In Figure 4(b), for a sample annealed at 800°C for 0.5 hour, one sees a large number of grains with a diameter of about 45 nm, and a distribution of smaller grains. An anneal at 900°C (Figure 4(c)) does not cause any significant increase in the size of the large grains which have now an average size of about 50 nm, but most of the small grains have disappeared. The 1000°C (Figure (d)) causes the formation of fairly equiaxed grains with an average

diameter of about 100 nm. This is typical of grain coarsening where small grains disappear at the expense of larger grains, thus minimizing the interfacial energy. It can be readily seen that the evolution of the electron diffraction patterns reflects quite clearly the effects observed in the TEM micrographs.

In order to verify that the rings observed in Figure 4(b,c,d) are indeed due to WSi_2, one final experiment was done. A 100 Å layer of polycrystalline gold was evaporated on the WSi_2 sample used in Figure 4. The diffraction patterns from this specimen and from a polycrystalline, purely gold specimen are shown in Figure 5. Since the lattice parameter of gold is known, the spacings of the gold rings can be used to calibrate the other rings. The results of these measurements are shown in Table II. The measured d-spacings of WSi_2 in Table II agree well with those reported in the ASTM files.[6]

B. Homogenization

The transformation of the tungsten silicides to their final tetragonal form occurs between 625° and 675°C. However, the composition throughout the film may still not be homogeneous. As shown by the backscattering analysis in Figures 6 and 7, the as-deposited W-rich and Si-rich films do not have a homogeneous composition (solid curves). From Figure 6, the W-rich film is seen to become homogeneous after annealing at 800°C for 15 minutes. This is evident from the lowering of the W signal and the simultaneous raising of the Si signal to a flat plateau. Interestingly, it is more difficult to homogenize the Si-rich films as can be inferred from Figure 7. Unlike W-rich films, Si-rich films do not homogenize after annealing at 800°C for 4 hours (Figure 7(a)). Figure 7(b), showing only the W signals, indicated that the Si-rich film is still

not completely homogenized after 900°C annealing. Annealing at 1000°C for 15 minutes is necessary to homogenize the film completely (Figure 7(c)). The resistance of the Si-rich film to reach homogeneity is very interesting. The W signals shown in Figure 7(c), rise to a plateau and shrink in width. This suggests that the excess Si atoms move to the interface of WSi_2 and poly-si after homogenization annealing. The Si migration here is analogous to the epitaxial growth of Si on poly-Si films, which normally requires high temperatures. On the other hand, the W-rich film homogenizes by drawing Si atoms into the silicide films (Figure 6). In this case, the Si atoms are provided from the underlying polysilicon. The driving force for this homogenization process is the heat of formation of WSi_2. However, the homogenization of the Si-rich films occurs through the deposition of Si on the substrates. The driving force for this process is only the surface energy of small Si precipitates within the silicide film. This latter quantity is much smaller than the heat of formation of WSi_2(Kcal/g.atom). Hence, the corresponding process requires higher temperatures. The stoichiometric WSi_2 film should be homogeneous after evaporation if the evaporation is well controlled. Any small fluctuations in composition can be easily homogenized between 800° ~ 1000°C.

C. Adherence and Surface Morphology

It is not only the crystallization and homogenization temperatures that are determined by the composition of the tungsten silicides. In addition, the adherence and surface morphology of the films also differ according to the composition. Figure 8 shows a SEM micrograph of a "$WSi_{1.6}$" film after 1000°C annealing for 15 minutes. The micrograph shows a rough surface morphology. However, the WSi_2 and "$WSi_{2.3}$" films

(Figure 9) show a much more regular, smoother surface.

Apparently, the W-rich film is inferior with respect to adherence and surface smoothness. Although W-rich films homogenize at lower temperature, they do not seem suitable for device application.

Similar surface roughness behavior of W-rich films has also been observed in the case of W-silicide films deposited either by cosputtering of W and Si[9] or by simple dc sputtering of compound cathodes.[10] It is thought that this behavior results from high internal stresses, developed by the delayed crystallization behavior of the W-rich films. As discussed in Section III. A, "$WSi_{1.6}$" crystallizes to the final tetragonal structures at 675°C, while WSi_2 or "$WSi_{2.3}$" crystallizes at 625°C. The higher crystallization temperature results in higher internal stress (for the correlation between crystallization temperature and stress (e.g., see Reference 11). The characteristics of coevaporated films with different compositions are outlined in Table III, From this Table, the W to Si ratio, viz., 1:2 is found to be the best choice for device applications.

D. Conductivity and Grain Growth

The annealing studies of stoichiometric WSi_2 are further detailed by resistivity measurements and TEM of films annealed at 800° ~ 1000°C. Figure 10 shows the sheet resistivity of WSi_2 annealed for various times. It is apparent that the resistivity decreases drastically within the first 0.5 minute at all three temperatures, after which the improvement is very slow or even close to saturation. This indicates that the resistivity is a strong function of annealing temperature and time. In order to achieve low resistivity, high temperature (1000°C) annealing

is required. The same phenomena were observed in the grain growth of WSi_2 films. The grains are not uniform after annealing at 800°C or 900°C as shown in Figure 4. Only after the 1000°C annealing were uniform grains of ~ 100 nm observed. This correlates with the resistivity measurements shown in Figure 10; low resistivity is achieved after 1000°C annealing. The sample shown in Figure 4(c) went through an additional 30 minute annealing at 900°C. The corresponding microstructure shows identical grain sizes (Figure 11). This agrees with the saturation-like behaviors in the resistivity measurement shown in Figure 10. Furthermore, samples annealed at 800° and 900°C were re-annealed at 1000°C for 37 minutes as shown by the arrows in Figure 10. The sheet resistivity of these samples reduced to 2.9 Ω/□ which is the value for the 1000°C annealed sample. Electron microscopy shows that the grain size of these samples (two step annealed) are exactly identical to the 1000°C annealed sample (one step) in Figure 4(d). These observations suggest that the properties of the annealed film are determined by the highest temperature in the heat treatments and a close correlation exists between the grain size and resistivity of WSi_2 films. This is important for device fabrication because the thermal treatments in a device fabrication process involve various temperatures for different times. The resistivity of W silicide is almost entirely determined by the highest temperature in the process.

E. Phosphorous Redistribution in Silicide

All the WSi_2 films utilized in device applications are deposited on phosphorous-doped poly-Si. It is important to realize that the dopant P atoms in poly-Si redistribute during silicide annealing. this P redistribution is observed by Auger/SIMS measurements shown in Figure

12. In this figure, P concentrations are plotted versus the depth from the surface of WSi_2/poly-si stack. All the P atoms are confined to the poly-Si layer before annealing. After 900°C annealing for 20 minutes, a large amount of P atoms diffuses into WSi_2. This sample was annealed with a layer of 40 nm SiO_2 for passivation. The diffused P curve suggests that the migration of P atoms in WSi_2 is relatively fast and anomalous. As shown in Figure 12, the P profile after 900°C annealing is not a normal diffusion profile due to the concentration gradient; rather a pile-up of P atoms in WSi_2 is observed. Furthermore, this diffusion profile is not changed after an additional 35 minute annealing at 900°C. Apparently, the P migration in WSi_2 occurs by a very complex mechanism. Figure 13 shows the data from a sample annealed at 1000°C for 20 minutes. The P distribution after 1000°C annealing appears to reach equilibrium. some accumulation at the surface of WSi_2 is also observed. This sample was passivated with SiO_2 during the annealing. An additional 35 minute annealing at 1000°C did not appreciably change the P distribution. However, the dashed curve in Figure 13 indicates an out-diffusion of P into the atmosphere during annealing if the SiO_2 passivation is absent. Compared to the case with SiO_2, the loss of P in the sample without SiO_2 passivation is substantial. This out-diffusion of P has two important effects. First, the concentration of P in WSi_2 has a large effect on the plasma etch rate of WSi_2[12]; the out-diffusion of P atoms results in an uncontrollable concentration of P in the silicide, which is an important cause of uncertainty in the rate of etching. Secondly, the P concentration in poly-si affects the flat band voltage of the MOSFETs. If the

remaining activated P concentration in poly-si is too low, the threshold voltage of the device could shift from the designed value. For these two reasons an understanding of P migration in silicide is important. From this work, rapid migration of P atoms in silicide is observed and the presence of a layer of SiO_2 on silicide during annealing is also found to be essential to prevent the out-diffusion of P.

F. Etching

Tungsten-silicide films are not affected by the chemicals generally used in the fabrication of ICs (H_2SO_4, HNO_3, HCl, HF) or by mixtures of $H_2SO_4 + H_2O_2$, $HCl + H_2O_2$, and $NH_4OH + H_2O_2$ commonly used as cleaning reagents for Si. In the following experiments, therefore, all WSi_2 samples were cleaned by the standard procedures employed for silicon.

F.1. Dry Etching

It has been demonstrated[13] that Si_2 can be patterned by reactive ion etching, employing aluminum as a reactive ion-etching mask. The rate of etching in CF_4 at 13.56 MHz and 0.2 W/cm^2 is 400 Å/min. for WSi_2 as compared to 600 Å/min. for silicon.

F.2. Wet Etching

Because the etching process and chemical properties of WSi_2 film are similar to those of polysilicon[14], dilute solutions of HF-HNO_3 and NH_4F-HNO_3 can be used to etch and define its patterns. The etching rates based on various volume fractions of HNO_3 : NH_4F are plotted in Figure 14.

G. Thermal Oxidation

The formation of an insulating layer on top of the gate electrode and interconnecting layer is necessary so as to isolate it from subsequently deposited conducting layers. Vapor-deposited SiO_2 and Si_3N_4

can be used for this application. However, thermally grown SiO_2 is generally of superior quality. Therefore, thermal growth of SiO_2 on WSi_2 is of extreme importance. The oxidation mechanism of WSi_2 has been studied. It is generally agreed that the underlying silicon diffuses through the WSi_2 film to form SiO_2 on the surface.[15] In order to oxidize WSi_2, an innert gas preannealing step is essential. This preannealing procedure allows the wafers to be heated to a temperature at which Si diffusion through WSi_2 is adequate before oxidation of WSi_2 begins. Exposure of WSi_2 to O_2 at temperatures below 900°C usually results in film corrugation caused by the formation of volatile WO_3 or by the stress in the silicide film due to local formation of W-rich phases. With this preannealing procedure, WSi_2 can be oxidized successfully. Figure 15 shows the cross sections of oxidized WSi_2 on the thin gate oxide and on thick oxide regions. CVD SiO_2 is then deposited conformally on the WSi_2 structures.

After etching a step in the grown SiO_2, the thickness was measured with a Talystep machine. Figure 16 shows the thickness of SiO_2 as a function of time for the three temperatures of growth. It is seen that the growth of SiO_2 is a stronger function of temperature for WSi_2 films deposited on poly-Si. In order for SiO_2 to be used as an insulating layer in between conducting layers, it must have high electrical breakdown strength. For the oxide's growth on WSi_2, the mean value of breakdown strength was about 4×10^6 V/cm, which is comparable to that found for oxides grown on poly-Si. The composite CVD SiO_2 and thermal oxide on WSi_2 form a reliable isolation layer between the Al and the devices.

CONCLUSIONS

An understanding of the properties of WSi_2 film is essential for applying metal silicides in device fabrication. The W to Si ratio during deposition is proved to have important effects on subsequent annealing behavior. It is found that the stoichiometric ration W/Si = ½ is a better choice than other compositions (either Si-rich or W-rich). The as-deposited amorphous films crystallize between 300°C and 500°C into a hexagonal form of WSi_2. The transformation to the final equilibrium tetragonal structures occurs between 625° and 675°C, but complete homogenization (and stress relieving) of the film requires a temperature between 800° and 1000°C. A low sheet resistivity of 2.9 Ω/□ can be achieved in a 150 nm WSi_2 film after 1000°C annealing. The saturation-like behavior is observed both in the resistivity and grain size of the silicide film. This enables WSi_2 to be annealed with minimal annealing times at various temperatures. This result is important for device fabrication. An understanding of the P redistribution in silicide during annealing is also important for silicide application. Both the threshold voltage of a silicide device and the processing parameters of device fabrication are a strong function of P concentration in silicides. Hence, P migration during annealing is one of the important properties of silicide films. The feasibility of thermal oxidation of WSi_2 was demonstrated. Growth of SiO_2 on WSi_2 is a strong function of temperature for WSi_2 films deposited on poly-Si. Other physical and chemical properties of WSi_2 are quite comparable to those of poly-Si from the point of view of compatibility with the fabrication technology. Therefore, in conclusion, the use of WSi_2 as the gate and interconnecting material is feasible and should markedly improve the performance of integrated circuits.

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TABLE I.

Properties of Materials Used As Electrodes

MATERIAL	R_S (Ω/) 0.5 μm FILM	MELTING POINT(°C)	CHEMICAL COMPATIBILITY	THERMAL OXIDATION
Poly-Si	10.0	1410	YES	YES
Al	0.05	660	NO	NO
W	0.11	3410	NO	NO
Mo	0.1	2610	NO	NO
WSi_2	1.5	2165	YES	YES
$MoSi_2$	2.0	2050	YES	YES
PTSi	0.6	1229	YES	YES
$TiSi_2$	0.3	1540	NO	YES

TABLE II.

Lattice Plane Spacings From Figure 5

RING NO.	RAD. (γ)	d Å	hKL	
1	2.85	2.355	111	An fcc
2	3.29	2.039	200	
3	4.65	1.442	220	
4	5.46	1.230	311	
a	2.96	2.271	110	WSi_2 bct
b	3.33	2.020	103	
c	4.19	1.604	200	
d	4.52	1.485	202	

TABLE III.

Tungsten Silicide Annealing

	"$WSi_{2.3}$"	WSi_2	"$WSi_{1.6}$"
CRYSTALLIZATION	625°C	625°C	675°C
HOMOGENIZATION	1000°C	800 ~ 1000°C	800°C
ADHESION	GOOD	GOOD	PEELING
SURFACE MORPHOLOGY	SMOOTH	SMOOTH	ROUGH

FIGURE CAPTIONS

Figure 1. SEM micrograph and drawing showing a cross section of a WSi_2 MOSFET.

Figure 2. X-ray diffraction patterns for "WSi_2" or "$WSi_{2.3}$" after being annealed at various temperatures for 30 minutes.

Figure 3. X-ray diffraction patterns for "$WSi_{1.6}$" after being annealed at various temperatures for 30 minutes.

Figure 4. Transmission electron micrographs of WSi_2 deposited on poly-Si (a) unannealed (b) [a] bright field [b] dark field images after annealing at 800°C for 0.5 hour (c) [a] bright field and [b] dark field images after annealing at 900°C for 0.5 hour (d) [a] bright field and [b] dark field images after annealing at 1000°C for 0.5 hour. The corresponding electron diffraction patterns are also shown in the insets.

Figure 5. (a) Electron diffraction pattern from polycrystalline Au (b) Diffraction pattern from WSi_2 with evaporated Au layer. Numbers and letters refer to Table III.

Figure 6. He^+ - backscattering results of "$WSi_{1.6}$" on poly-Si. Before annealing, the high W signal indicated W-rich. After the sample is annealed at 800°C for 15 minutes, the sample is completely homogenized.

Figure 7. He^+ - backscattering results of "$WSi_{2.3}$" on poly-Si (a) after 800°C annealing, the sample is Si-rich, (b) after 900°C annealing, the sample is still Si-rich, and (c) after 1000°C annealing for 15 minutes, the sample is finally homogenized. Only the W signals are shown in (b) and (c).

Figure 8. SEM micrograph of a $WSi_{1.6}$" film after annealed at 1000°C for 15 minutes.

Figure 9. SEM micrographs of (a) WSi_2 and (b) $WSi_{2.3}$ films after annealed at 1000°C for 15 minutes.

Figure 10. Sheet resistance of WSi_2 on poly-Si after annealing at various temperatures and times.

Figure 11. Bright field electron micrograph of WSi_2 thin films sample in Figure 4 (c) went through an additional 30 minutes annealing at 900°C.

Figure 12. Phosphorous concentrations in silicide. Before annealing, all the phosphorous atoms are confined to the poly-Si layer. After 900°c annealing, a large amount of P migrates into WSi_2. The The sample has a SiO_2 cap layer during annealing.

Figure 13. Phosphorous concentrations in silicide. After 1000°C annealing, the phosphorous distribution in WSi_2 of the sample is not passivated with SiO_2 during annealing, a large amount of P out-diffuses into the annealing ambient.

Figure 14. Etching rate of WSi_2 films vs. ratios of etchant volumes. HNO_3: NH_4F.

Figure 15. SEM micrograph and drawing of a cross section of WSi_2 MOSFET's structure on the gate oxide and field oxide.

Figure 16. Oxide thickness as a function of time for steam oxidation of WSi_2 deposited on poly-Si.

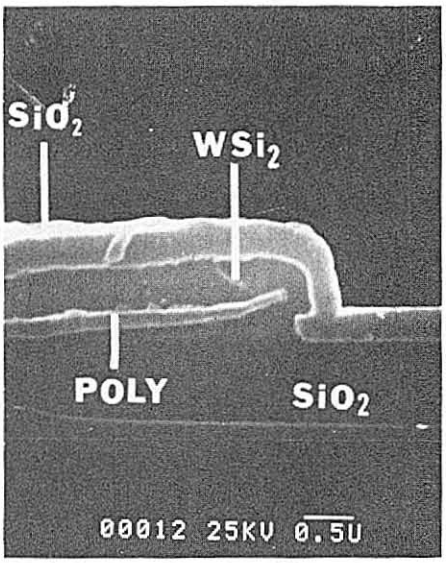
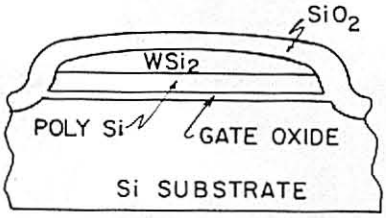


Fig. 1



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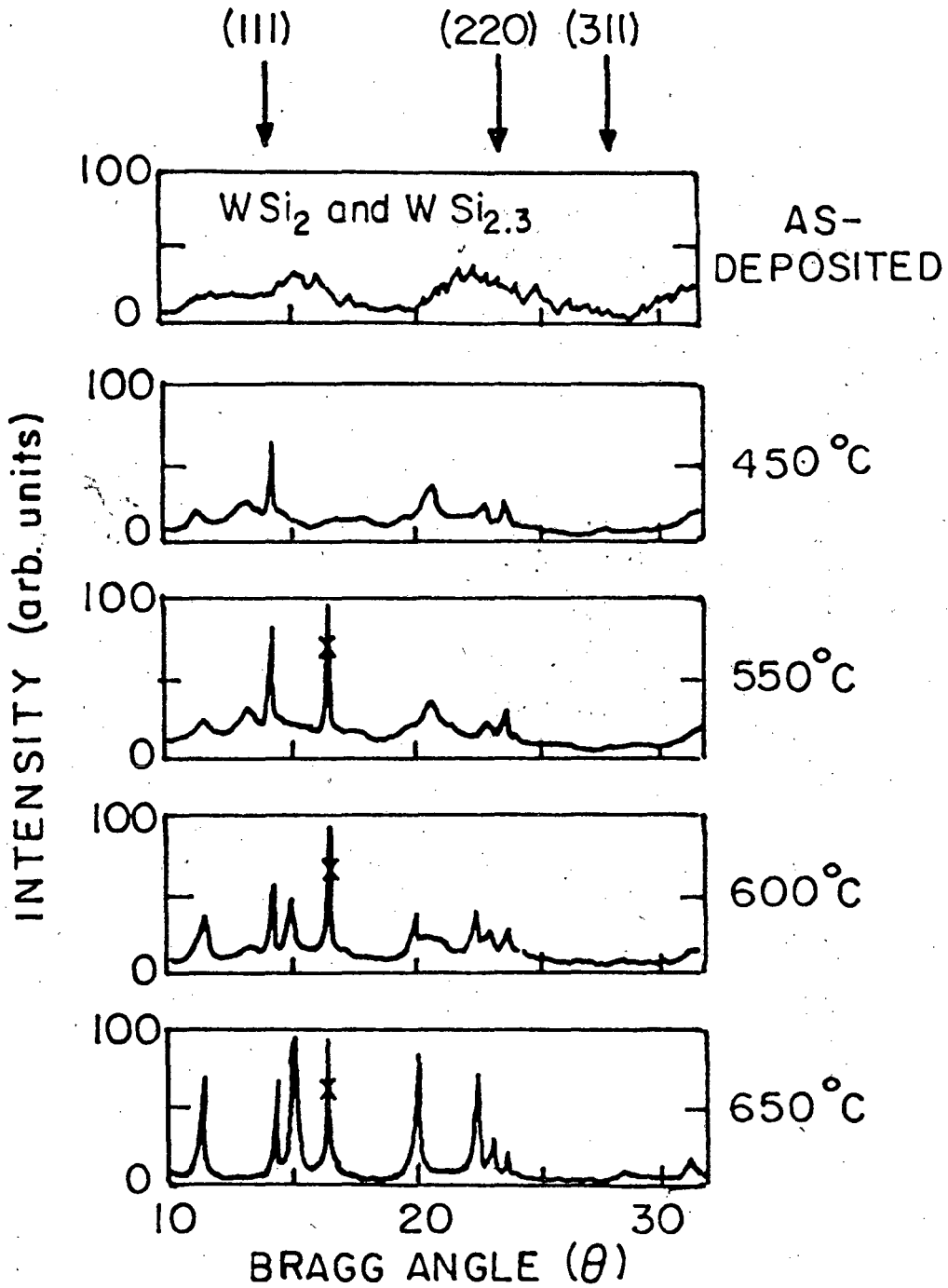

Fig. 2

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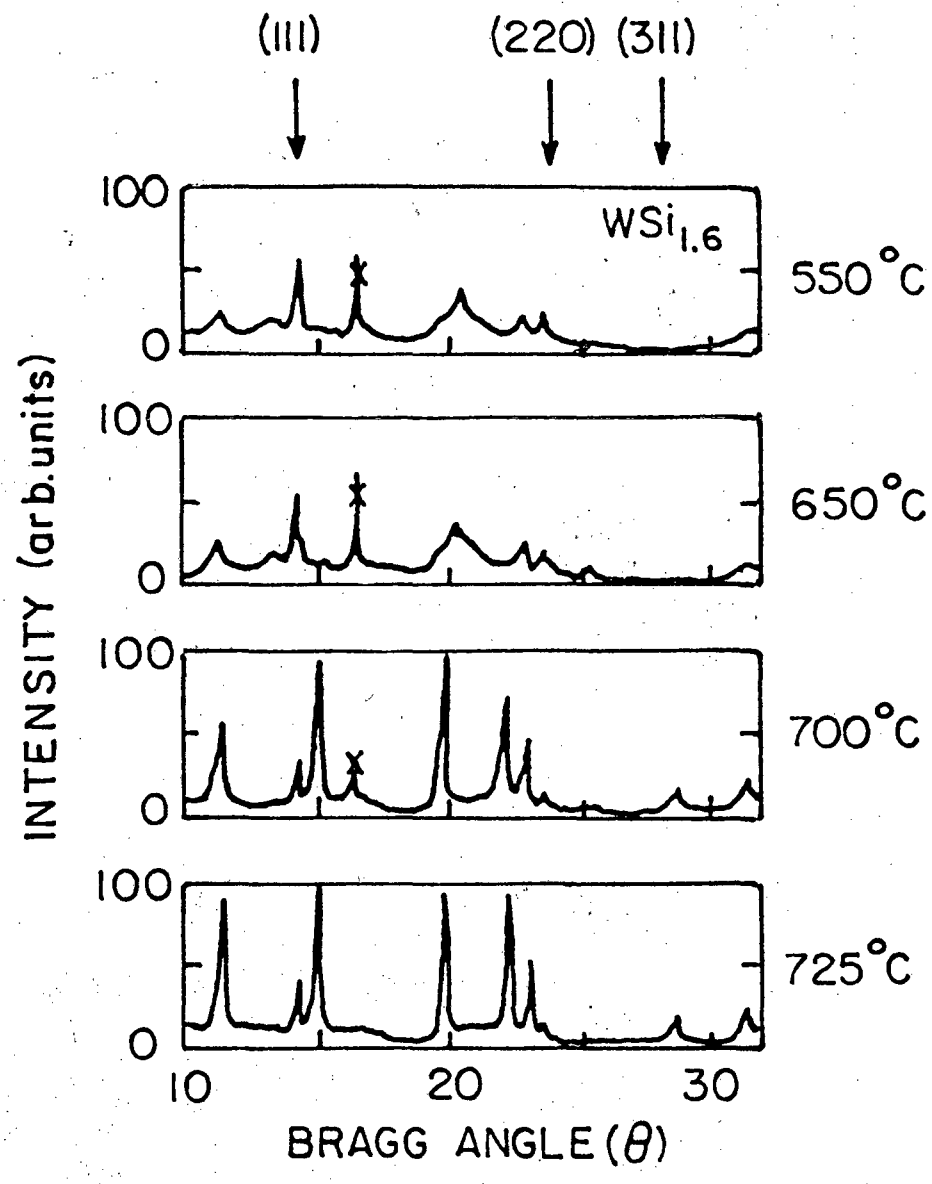

Fig. 3

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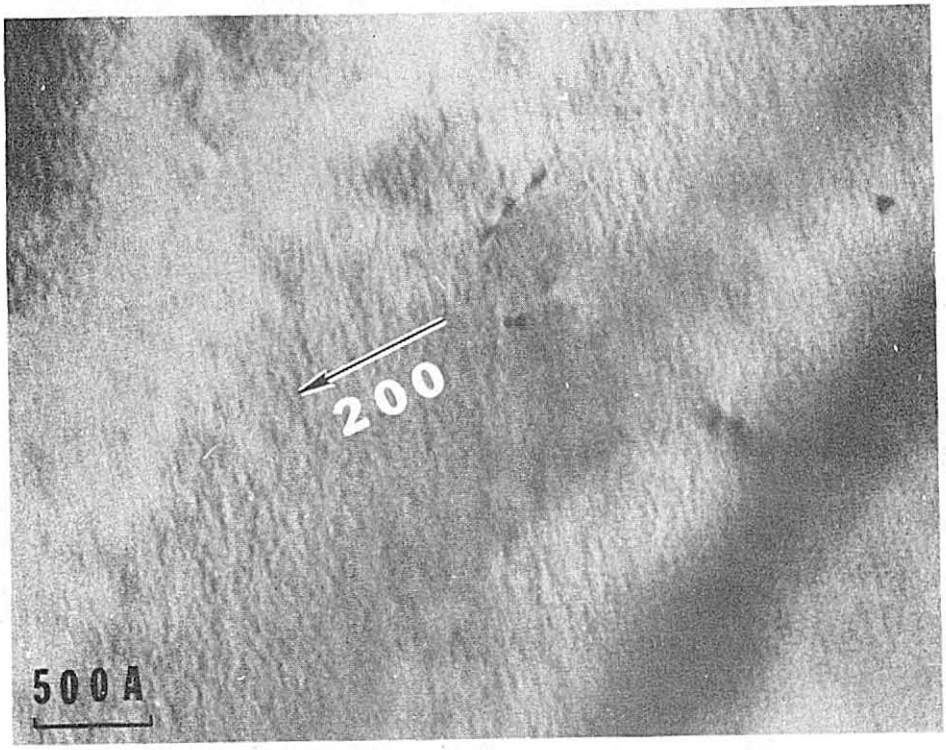


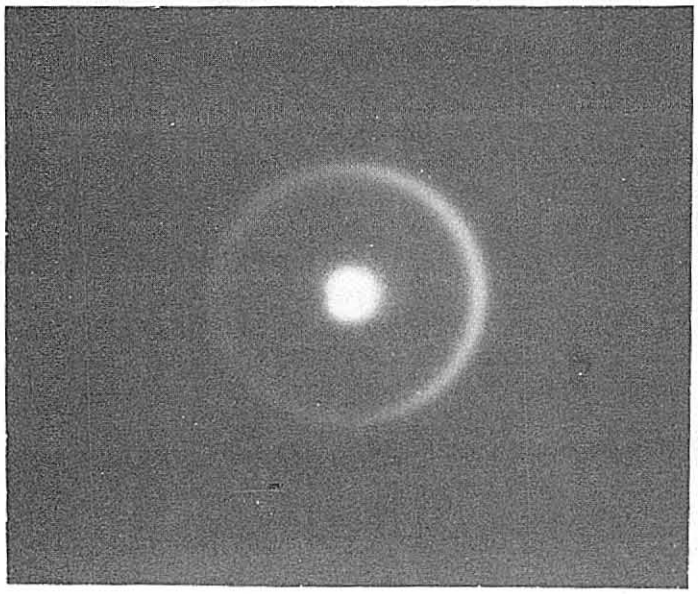


Fig. 4(a)

XBB 825-4752

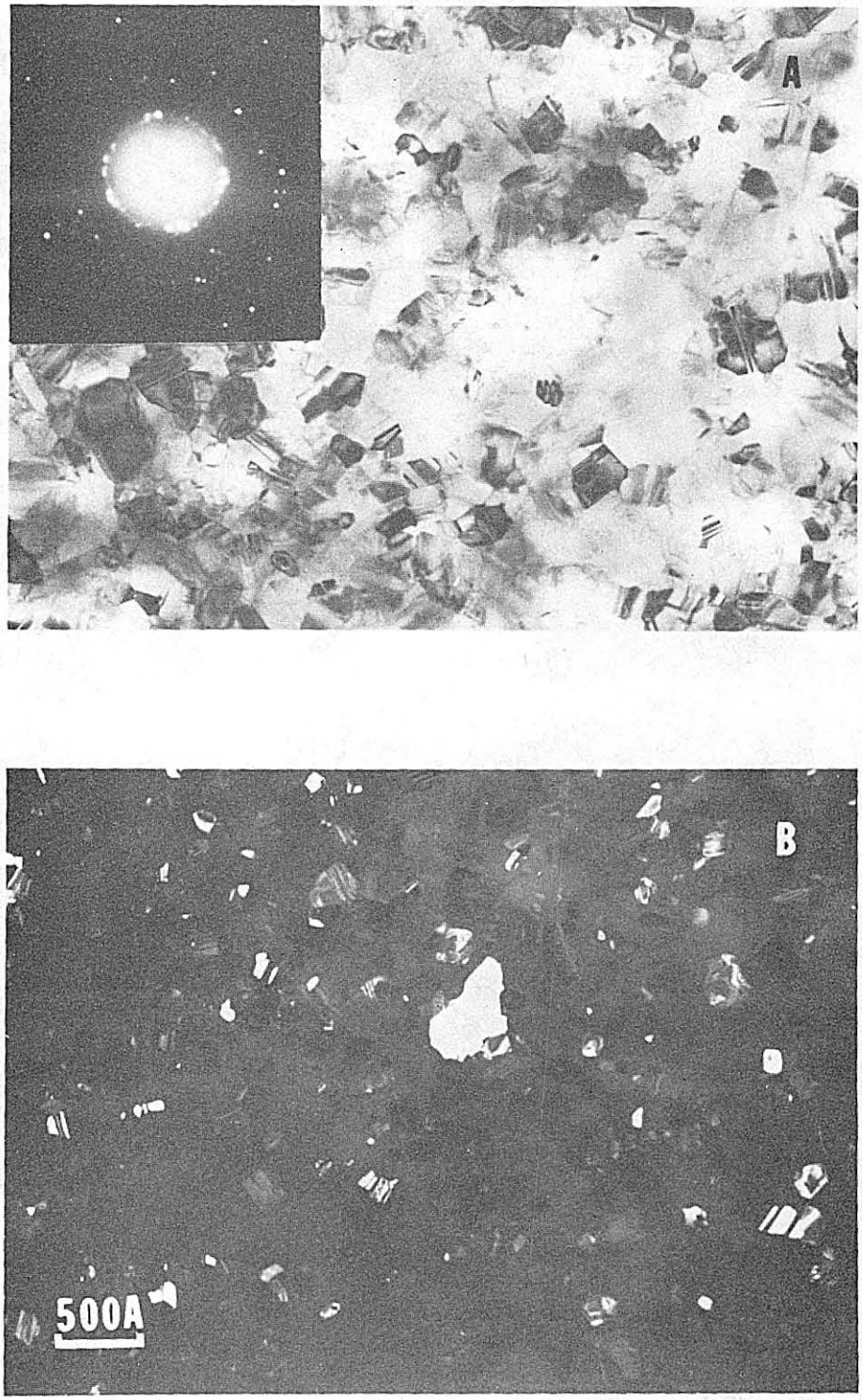
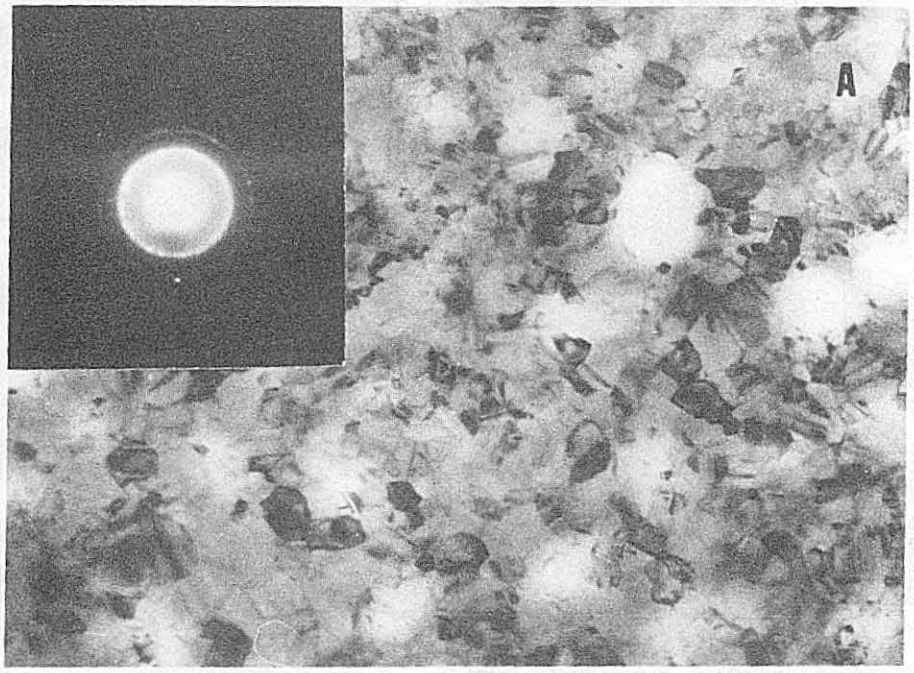


Fig. 4(b)

XBB 825-4756



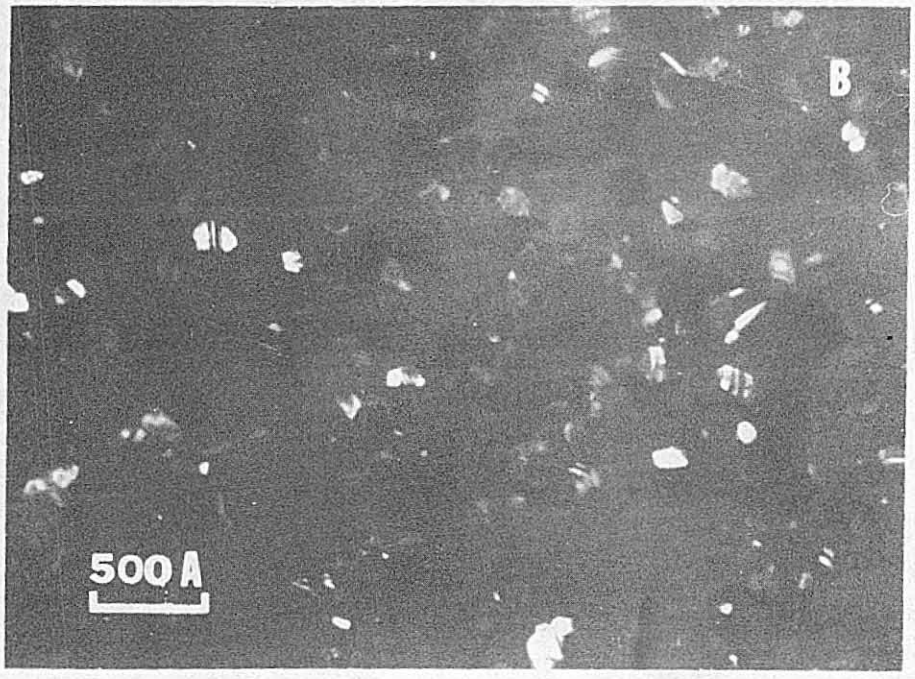


Fig. 4(c) XBB 825-4755

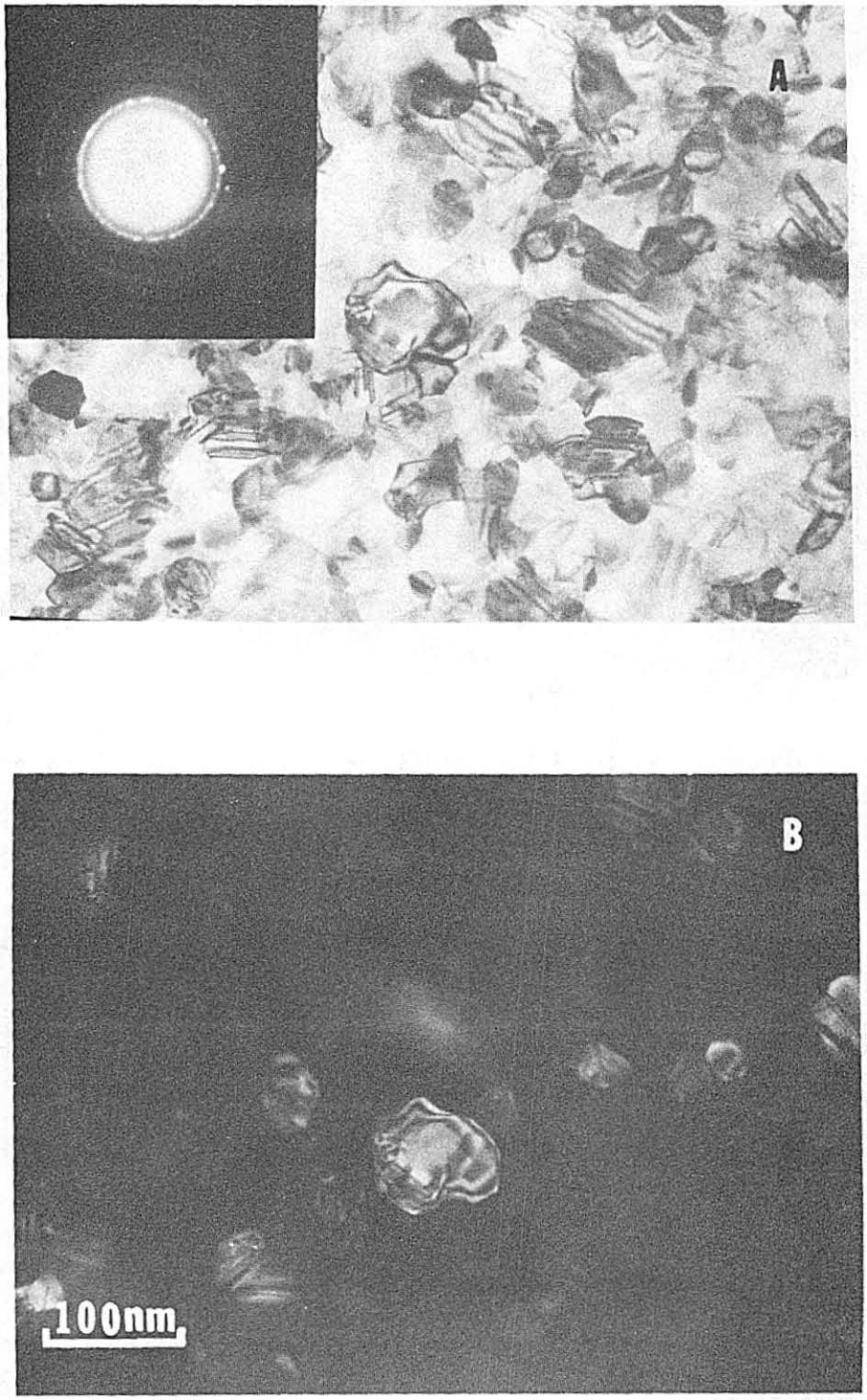


Fig. 4(d)

XBB 825-4754

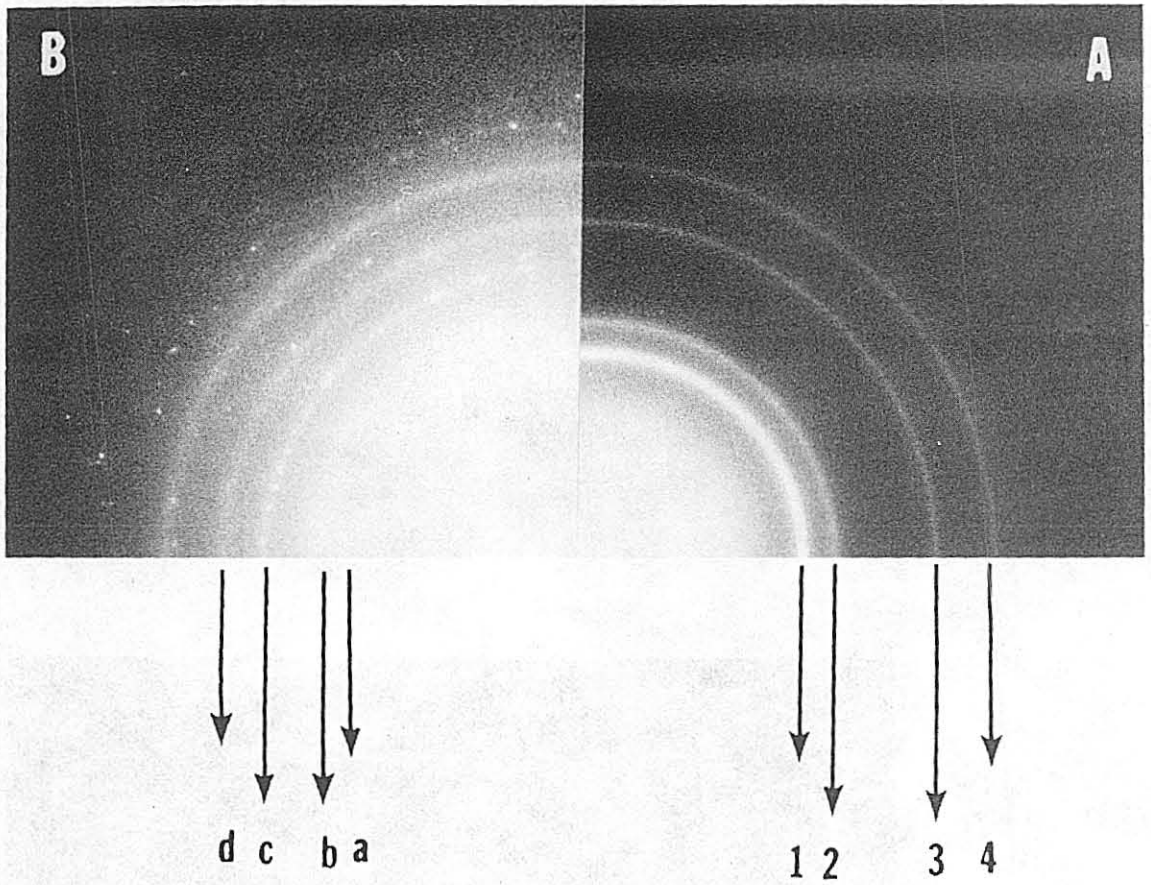


Fig. 5

XBB 825-4854

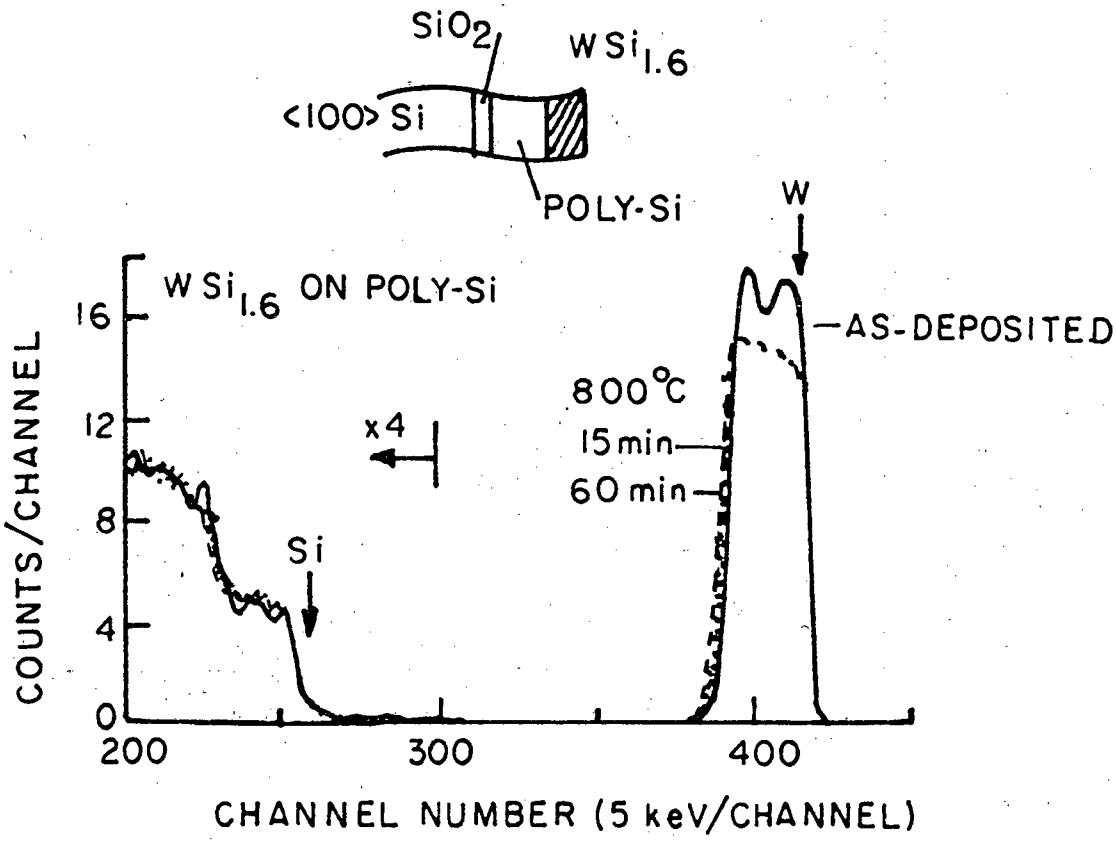


Fig. 6

XBL825-5852

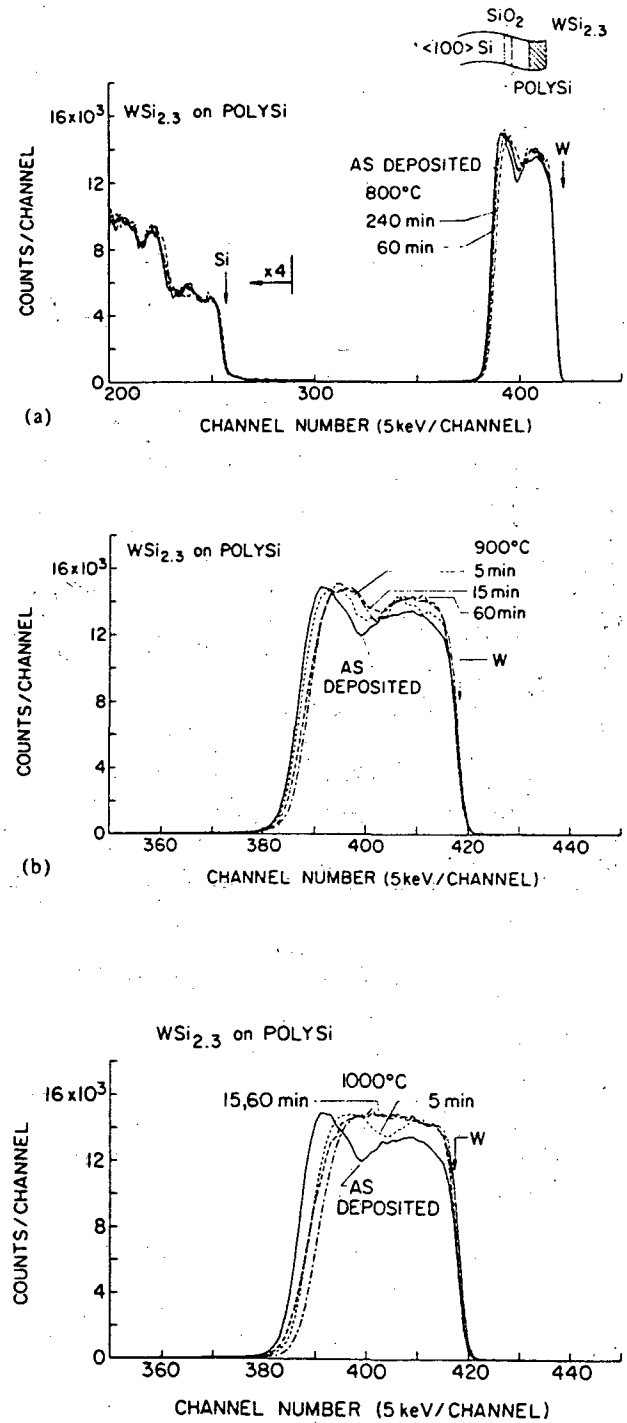


Fig. 7

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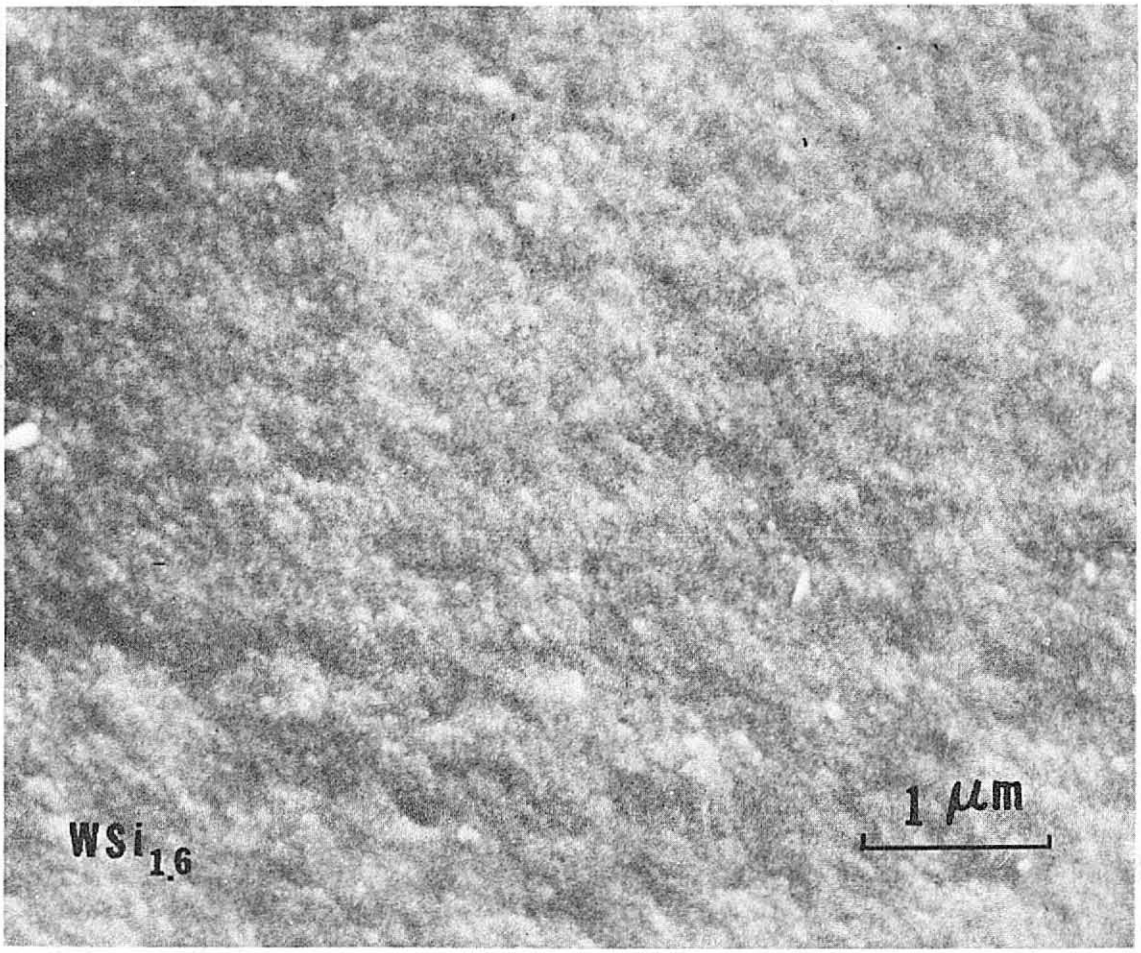

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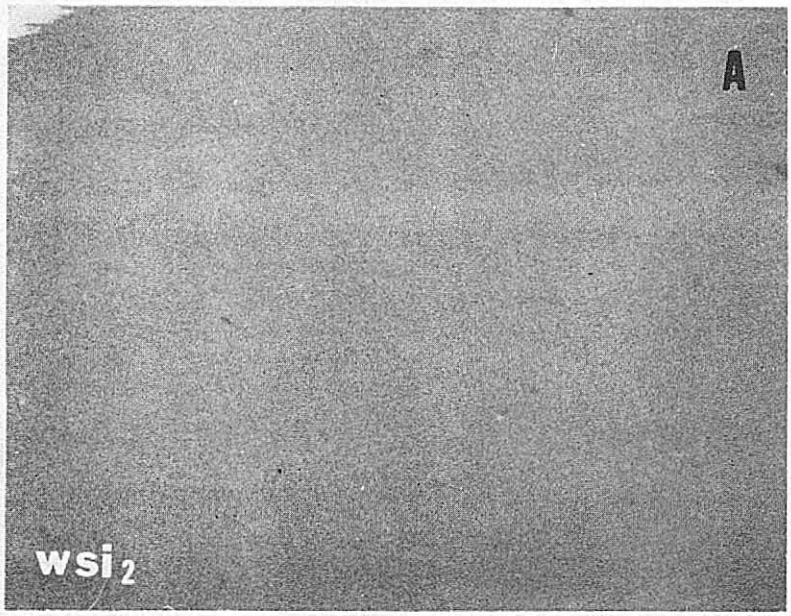

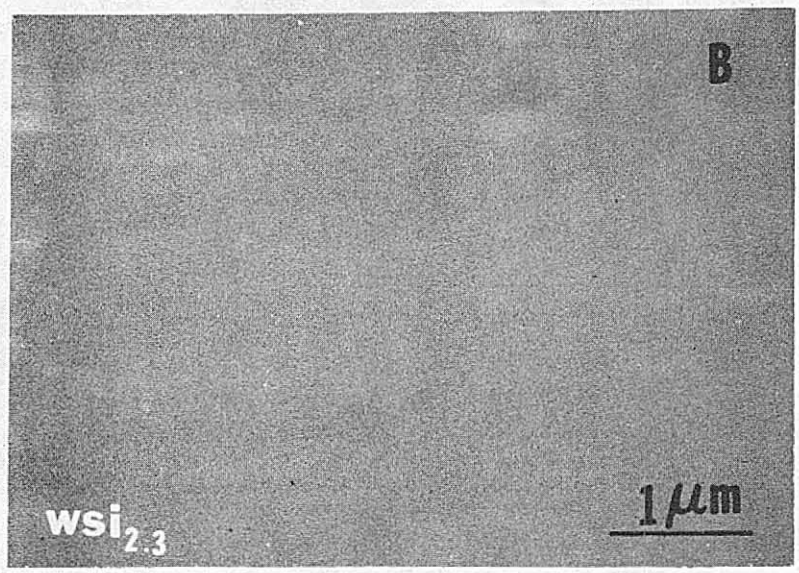

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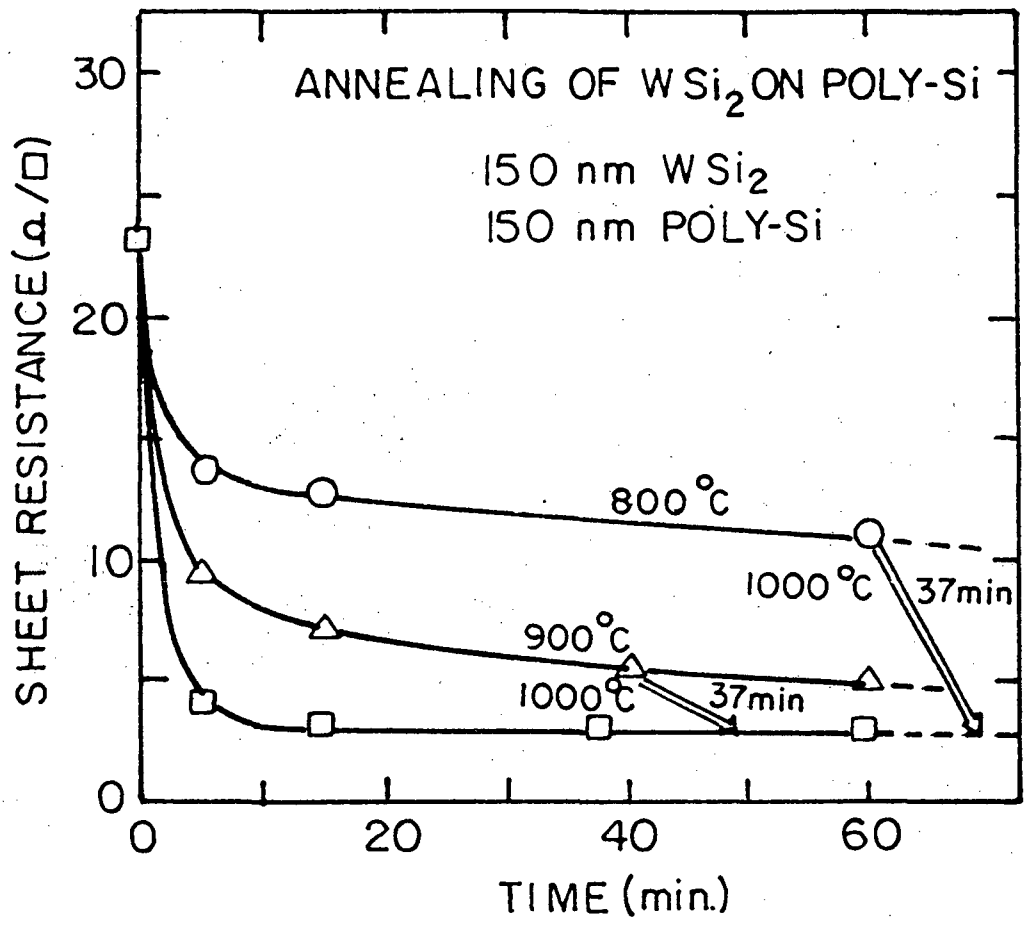

Fig. 10

XBL 825-5849

Fig. 11

XBB 825-4753

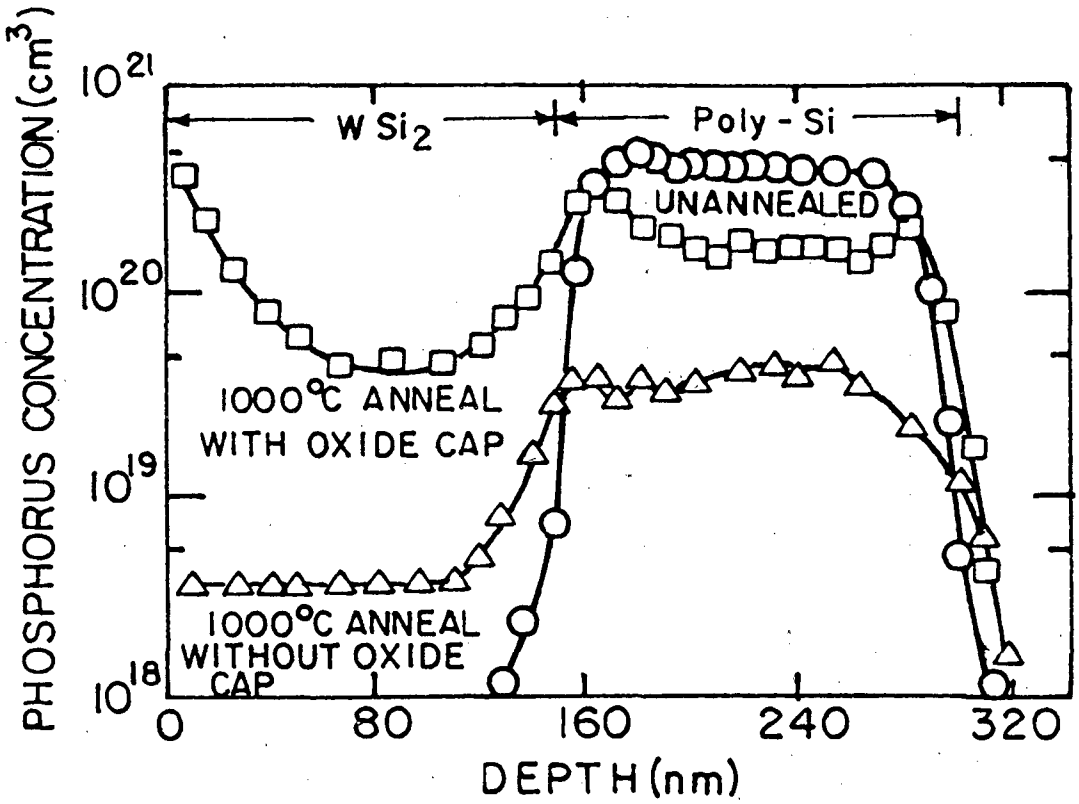

Fig. 13

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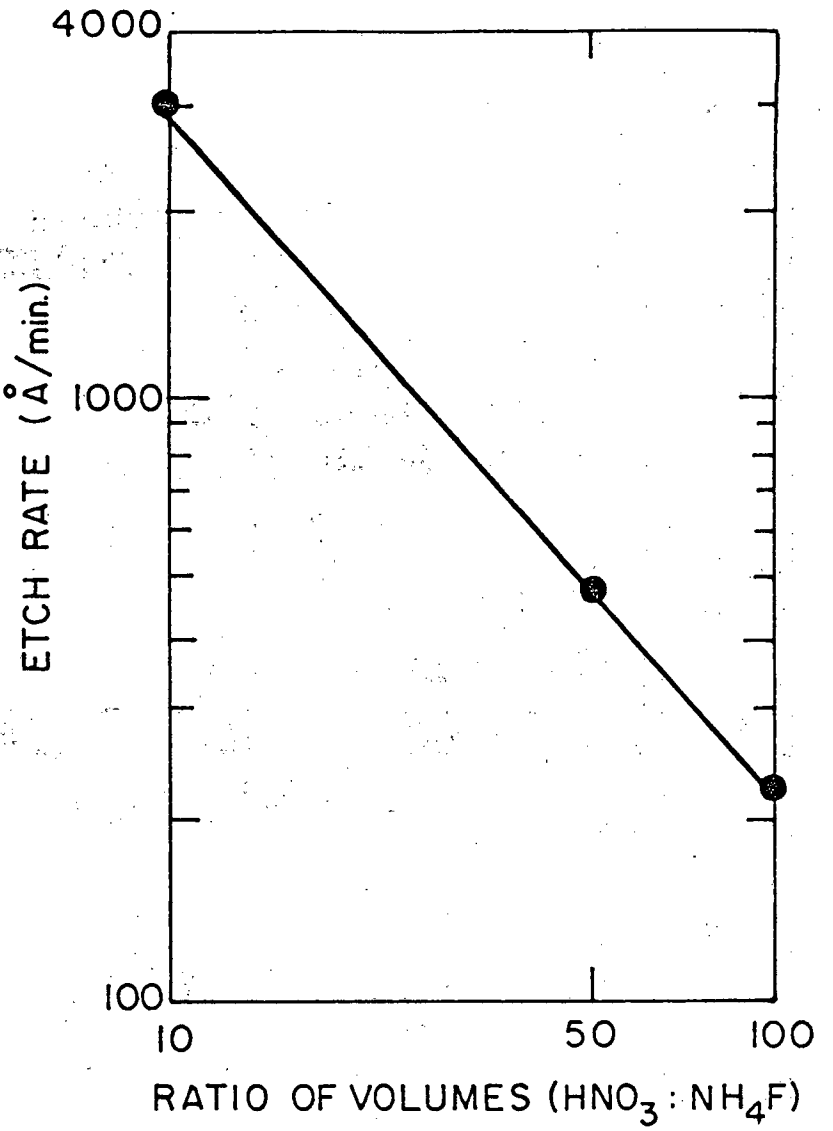

Fig. 14

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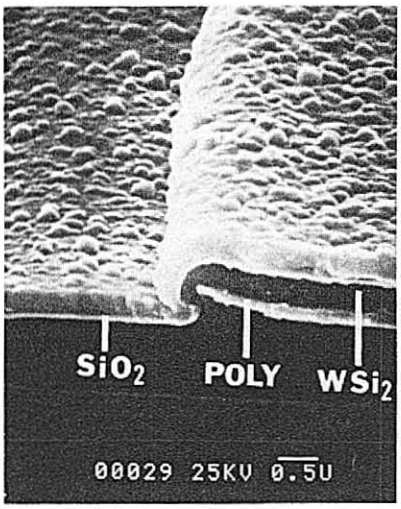

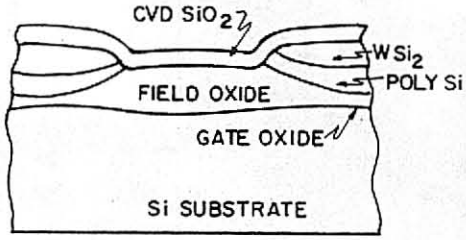

Fig. 15

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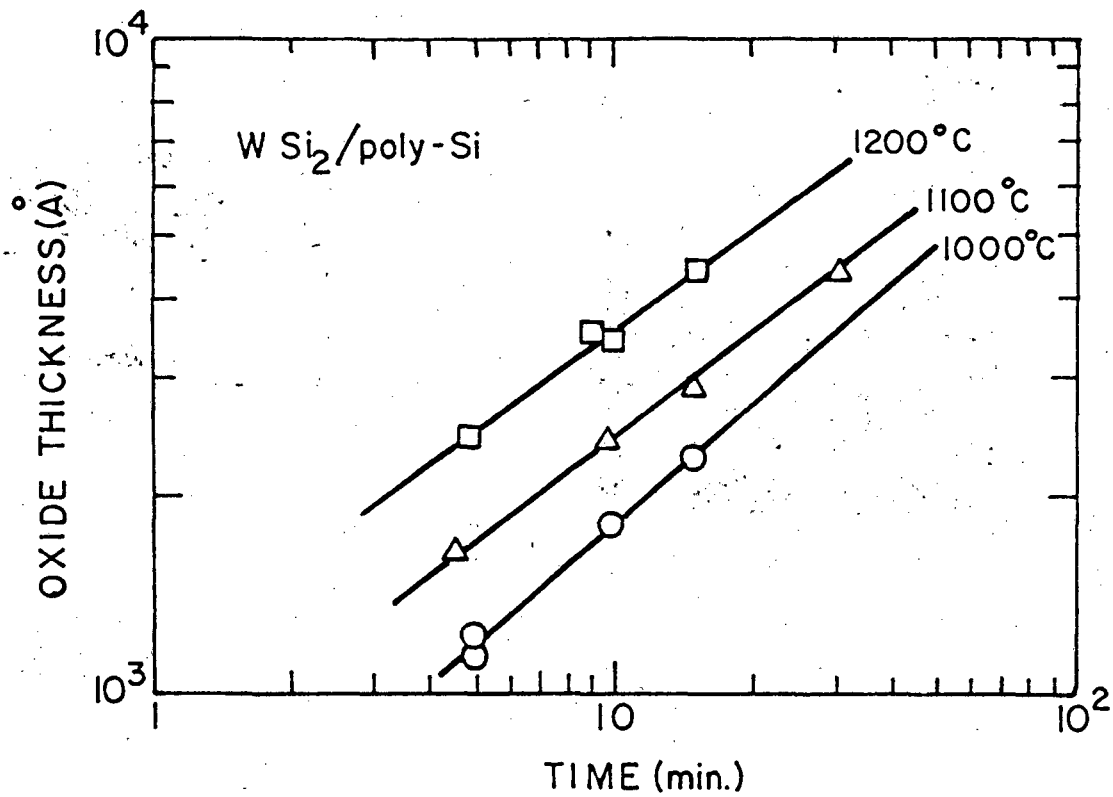

Fig. 16

XBL825-5845

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