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INTEGRATED CIRCUIT CONTROL FOR TWO-LAMP ELECTRONIC BALLAST: FINAL REPORT

Thomas P. Kohler

November 1982

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INTEGRATED CIRCUIT CONTROL

FOR TWO-LAMP ELECTRONIC BALLAST:

FINAL REPORT

Thomas P. Kohler*

Lighting Systems Research
Lawrence Berkeley Laboratory
University of California
Berkeley CA 94720

November 1982

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*EETech, Division of Beatrice Foods Co.
2735 Brundage Road
Baldwinsville, New York 13027

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ABSTRACT

This report describes circuitry for a solid-state, high-frequency fluorescent ballast designed to operate two F40 T-12 rapid-start lamps. The circuits are designed to be produced by hybrid integrated circuit (IC) technology. The signal components are produced on a single IC chip; the power transistors are attached to an alumina substrate. The initial IC version reduces the component count by about 50%. The cost of each IC in 500K lots is $0.70, replacing discrete parts costing $2.25. Additional savings of more than $1.00 per unit are realized by the decreased assembly time and improved reliability of the ICs.

The system performance (two-lamp F40) was compared to the discrete version of the ballast and to an efficient core-coil ballast and found to be 6% less and 20% more efficient, respectively. The decrease in efficiency relative to the discrete version of the ballast is due to retaining some power to the filaments during operation in order to maintain normal lamp life.

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1.1 Introduction

The first production of dual 40 ballasts used a discrete design that was configured for later conversion to integrated control. The discrete version was developed first because it was believed that would result in the shortest possible development time. Conversion to IC control was planned as an improvement in cost and producibility that would be necessary as the market matured. About 40,000 were built in the discrete version and the experience gained from these led to some modification of the original circuit plan.

Cherry Semiconductor developed the IC to specifications which were supplied by EETech and consultant John Wu. Two hundred and thirty samples of the integrated circuit were delivered to EETech and thirty of them were tested in ballasts before the program was terminated.

Fifteen ballasts using the integrated control were delivered to Lawrence Beckeley Laboratories in June 1982 as part of their program to promote the development of energy efficient lighting.

This report discusses details of the ballast development and the performance that was measured at EETech before delivery of the samples to LBL.

1.2 Control Theory

There are three modes of operation of the ballast using the integrated circuit control; preheat, ignition, and running. Reference is made to the functional block diagram of figure 1 to better understand the relationships in the control method.

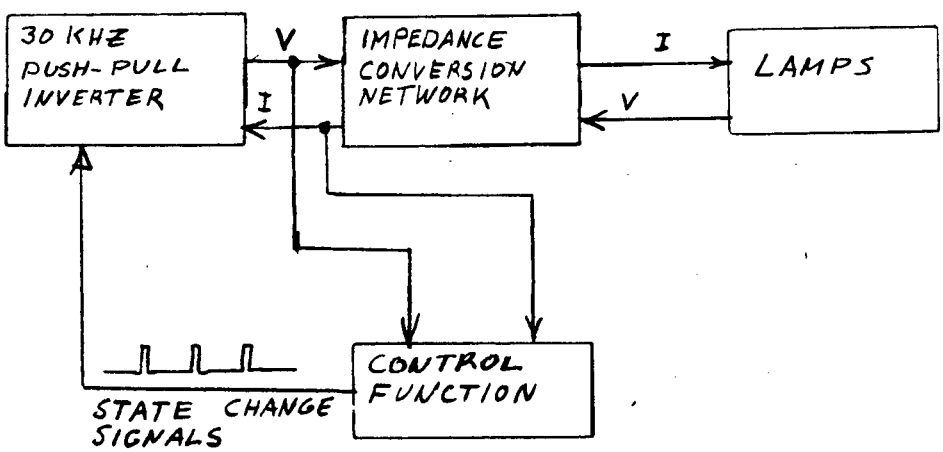

Figure 1. Functional Block Diagram

The impedance conversion network is the "ballast" in a conventional sense. i.e. it converts the constant voltage load of the gaseous discharge lamp into a constant current load for the inverter. All three operating modes make use of the state change signal into the inverter to control inverter current. Increasingly rapid state changes decrease the current of the inverter because the input impedance the inversion network always appears somewhat inductive to the inverter.

During preheat, the state change signal is controlled in response to the voltage level on the filaments. Increasing voltage results in a higher inverter frequency which in turn tends to keep the voltage from increasing. The result is a stable operating point which is independent of transistor parameters. The operating level is chosen so that the voltage out of the inversion network is not enough to ionize the lamps during preheat mode. The turns ratio on the filament transformer are chosen to give the proper filament current during this mode.

Periodically, at 1 sec intervals the feedback path from the filament voltage is interrupted. This is the ignition mode. State change signals are derived by sensing the times at which instantaneous inverter current exceeds some chosen maximum limit. The limit must satisfy a number of design constraints. First it much be low enough to ensure survival of the inverter switches no matter what output load conditions are present. Second it must be high enough so that ignition of the lamps is ensured. If ignition is not obtained in 20 milli seconds, the ballast reverts to preheat mode and waits another second.

If ignition is obtained during the ignition mode, the state change signals come from a phase detector which compares the phase of the inverter voltage with the phase of the inverter output current. In effect, this causes the inverter to operate at some frequency where the load on the inverter is some chosen power factor. Tight control of the inverter power factor by means of the phase control is important for several reasons:

1) The emitter switched inverter, (a form that has minimum switching losses) can only operate properly driving a lagging power factor load.

2) Excessively lagging power factor has an efficacy penalty in both the inverter and the impedance inversion network.

3) As the resonance of the impedance inversion network moves around, in response to the varying lamps impedance, the frequency of the inverter keeps a proper relation to the impedance inversion network.

1.2.1 Circuit Considerations

Figure 2 is a schematic of the ballast before the integrated circuit replaced the control elements. A comparison with Figure 3 which includes the IC illustrates the part's count advantage of producing the ballast with the IC.

A schematic of the integrated circuit is shown in Figure 4. Transistor N22 performs the function of Q5 in the discrete version. N23 and N24 and the associated diode clamps comprise the phase detector circuit. The components to the right of the dashed line make up the replacement for the NE555 timer, which was an integrated circuit in the original design.

A comparison of the schematics shows that the integrated circuit is almost an element by element copy of the discrete version. It was felt that this was a low risk path to an integrated circuit because the original version is in effect a thoroughly checked out breadboard for the integrated circuit. Not quite.

In some of the samples, the timer would not function in the presence of high signal levels into the inputs of the phase detector. Only one of the inputs exhibited this sensitivity and the samples were screened by Cherry Semiconductor to obtain enough working samples, to fulfill the contract. The coupling appeared to result from a substrate overload. If the integrated circuit version is to become a commercial ballast, a new layout of the IC is probably necessary.

1.2.2 Relative Cost Information

The quoted prices for this IC in semi-custom version was $1.19 for quantities of 200 thousand. For higher quantities, Cherry Semiconductor recommended a full custom IC with a $20K tooling charge and a $.70 piece price in 500K lots. The parts replaced by the IC have a total cost of about $2.25. More important cost benefits would result from lower assembly time and greater reliability due to an un-cluttered layout.

1.2.3 Performance Comparisons

Table 1 shows the relative light output of the 15 samples which were prepared for LBL. The measurements were made in a surface mounted closed ceiling fixture, suspended 4 feet above the floor, with the photo-cell on the floor. for reference purposes, the same measurements were performed on commercial energy saving magnetic ballasts, on a Thomas electronic ballast, and on a First generation EETech ballast (discrete components and filament heat removed after ignition). The readings were taken over several days, and the magnetic ballast measurements were repeated every day to track any drift in lamp characteristics. The lamps used were GE 34W WATTMIZER II lamps.

Note that if the first reading on the magnetic ballast is taken as the reference, the average increase in efficacy for the EETech IC samples is $\sim$20%. If the reference is adjusted for later readings the increased efficacy is 22%.

Sample #12 doesn't seem to be in the "group" but no reason for its low performance was found.

1.3 SUMMARY

The integrated circuit version of the EETech ballast is not simply a repackaging of all the transistors and resistors that are in the SSB1 model. The major functional difference is that a maintenance level of filament power is kept on the filaments during the running of the lamp, while in the SSB1 model all filament power was removed after lamp ignition.

There are two advantages to this approach:

1) It eliminates the need for the power transistor which switched the filament power in or out.

2) It holds the promise of longer lamp life by keeping the lamp cathodes at a higher temperature.

The disadvantage is that it decreases the efficacy of the system because filament watts don't contribute to any light output.

The integrated circuit replaces 6 resistors, 7 transistors, 14 diodes, and an NE555 timer. The board area that is saved by the integration can be used to spread out the remaining parts, making manufacture somewhat easier.

1.3.1 The LBL Samples

The 15 samples that are delivered to LBL have the following physical and functional characteristics.

The samples were built by removing parts from an SSB1 board and attaching the integrated circuit. Connections were made to the circuit board by soldering in the necessary jumper leads. Therefore, these samples don't exhibit the layout advantages that will result from integration.

With energy saving lamps the maintenance voltage on the filaments is from 2.3 to 2.5 volts. Using about 2.5 to 3 watts in the filament. With standard 40W lamps the filament voltage will increase to 3.5 volts, using about 5 to 6 watts in the filaments. This is a significant handicap in the efficacy "race". Although sales literature will steer the user toward energy-saving lamps, data should also be taken on F40 lamps.

Preheat voltage on the filaments is around 4.5 volts. This occurs with energy-saving lamps and standard F40 lamps.

The open lamp ignition voltage was inadvertently decreased about 15%, in the LBL samples. Because of this, some difficulty may be experienced in starting lamps below room temperature. However, it should not interfere with the LBL data gathering.

Refinements for Production Ballasts

The decrease in open lamp ignition voltage experienced in the LBL samples is not intrinsic to the integrated version and it would be restored to the levels present in the SSB1 model.

The selection of a proper filament maintenance voltage cannot be made based on presently available data. The factors involved are as follows:

1) The purpose of leaving filament power on is to avoid lamp life penalties.

2) It has been determined that lamp life without any filament power after ignition is approximately 10,000 to 12,000 hours.

3) Some ballasts are on life test with filament maintenance at same level as the LBL samples. Only 4,000 hours have been logged in this test, so no conclusions can be drawn about the adequacy of this filament maintenance level.

If it is determined that 2.5 watts of filament power isn't enough to make a significant difference in the lamp life, someone will have to decide whether the most appealing product would result from decreasing the filament power to the lowest possible level (consistent with the integrated configuration) and accept the life penalty or raise the filament power to some higher level and accept an efficacy penalty.

Table 1. Relative Light Output

Ballast	Line Watts	L.U.	Efficacy	Relat. Efficacy	Relat. Adj. Efficacy	Temp.
Advance	72.3	407	5.629	1		78 Deg F
EETech Sample #1	57.0	395	6.930	1.23		78 Deg F
EETech SSB-1	57.5	422	7.189	1.27		73 Deg
EETech Sample #2	56.2	385	6.851	1.22		74 Deg
EETech Sample #3	58.4	399	6.832	1.21		74 Deg
GE Maximiser	78.3	450	5.747	1.02		75 Deg
Advance	71.8	398	5.543	.985	1	75 Deg
EETech Sample #4	56.3	380	6.750	1.20	1.22	
EETech Sample #5	56.4	387	6.862	1.22	1.24	75 Deg
EETech Sample #6	58.5	399	6.820	1.21	1.23	75 Deg
EETech Sample #7	56.3	383	6.803	1.21	1.23	75 Deg
EETech Sample #8	56.3	381	6.767	1.20	1.22	74 Deg
EETech Sample #9	56.7	378	6.666	1.18	1.20	74 Deg
EETech Sample #10	54.7	363	6.636	1.18	1.20	71 Deg
Advance	72.3	397	5.491	.98	1	71 Deg
Thomas	61.5	390	6.341	1.13	1.15	73 Deg
EETech Sample #11	58.9	399	6.95	1.23	1.27	

Ballast	Line Watts	L.U.	Relat. Efficacy	Efficacy	Relat. Adj. Efficacy	Temp.
EETech Sample #12	57.4	385	6.438	1.14	1.17	73 Deg
EETech Sample #13	59.8	401	6.705	1.19	1.22	73 Deg
EE Tech Sample #14	57.1	390	6.83	1.21	1.24	73 Deg
EETech	58.6	399	6.808	1.21	1.24	73 Deg

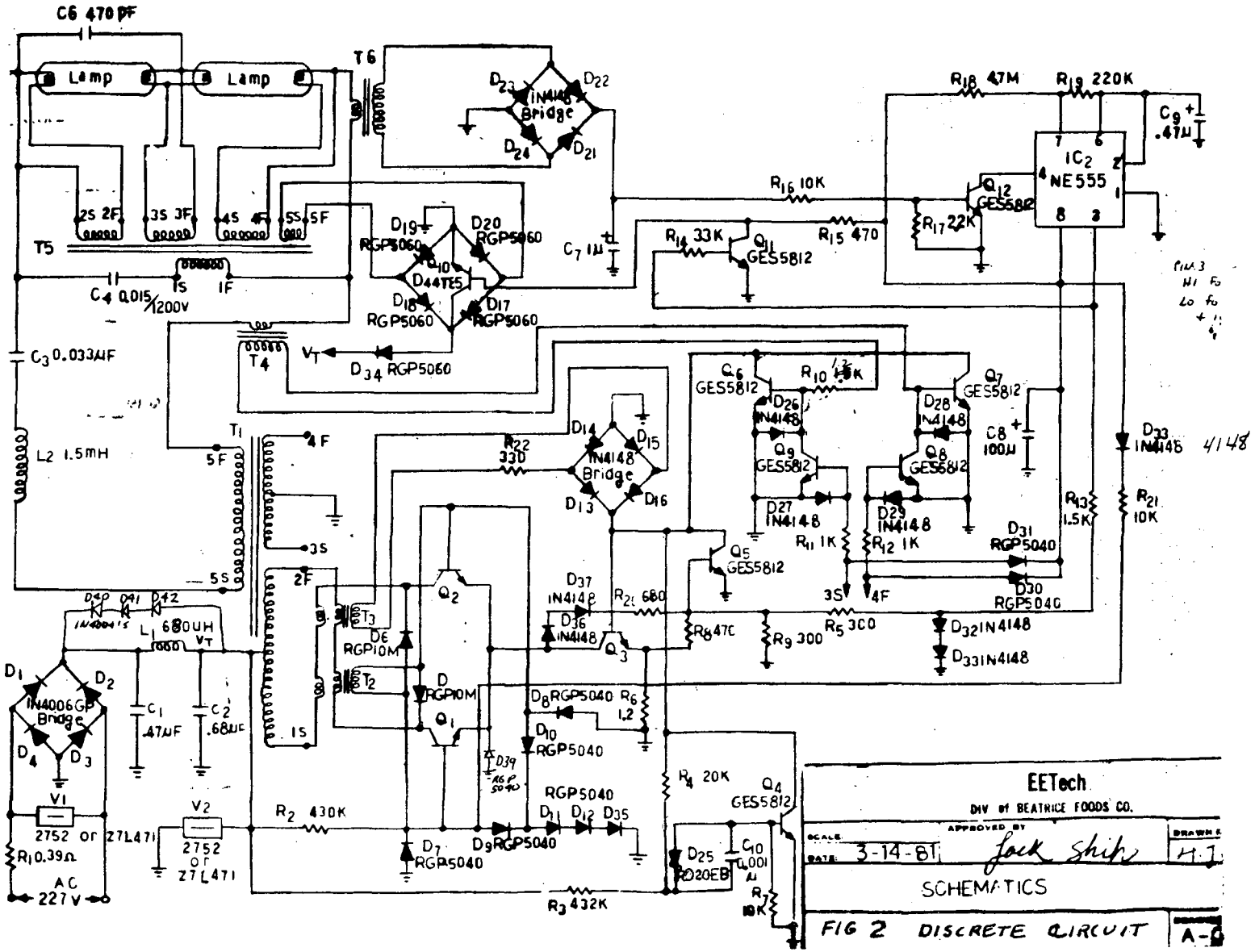
C6 470 pF
Lamp
Lamp
T6
D23
D22
1N4148 Bridge
D24
D21
R18 47M
R19 220K
C9 .47µ
IC2 NE555
R16 10K
Q12 GES5812
R17 22K
R14 33K
Q11 GES5812
R15 470
C7 1µ
T5
2S 2F
3S 3F
4S 4F
5S 5F
D19
D20 RGP5060
RGP5060
D44TE5
D18 RGP5060
D17 RGP5060
C4 0.015/1200V
1S
1F
C3 0.033µF
T4
VT
D34 RGP5060
L2 1.5mH
T1
5F
4F
3S
5S
2F
1S
R22 330
D14
D15
1N4148 Bridge
D13
D16
Q6 GES5812
R10 1.5K
Q7 GES5812
D26 1N4148
D28 1N4148
C8 100µ
Q9 GES5812
Q8 GES5812
D27 1N4148
D29 1N4148
R11 1K
R12 1K
D33 1N4148
R13 1.5K
R21 10K
D31 RGP5040
D30 RGP5040
Q5 GES5812
D37 1N4148
R20 680
D36 1N4148
Q3
R8 470
R9 300
R5 300
D32 1N4148
D33 1N4148
D40 D41 D42
1N4004's
L1 680UH
VT
D1
D2
1N4006GP Bridge
D4
D3
C1 .47µF
C2 .68µF
T3
D6 RGP10M
T2
D RGP10M
Q2
Q1
D8 RGP5040
R6 1.2
D10 RGP5040
D39
RGP5040
V1
2752 or Z7L471
R1 0.39Ω
AC 227V
V2
2752 or Z7L471
R2 430K
D7 RGP5040
D9 RGP5040
RGP5040
D11
D12
D35
R4 20K
Q4 GES5812
D25 RD20EB
C10 0.001µ
R7 10K
R3 432K
EETech
DIV of BEATRICE FOODS CO.
APPROVED BY
SCALE
DATE 3-14-81
Jack Shih
SCHEMATICS
FIG 2 DISCRETE CIRCUIT
A-6

Figure 2.

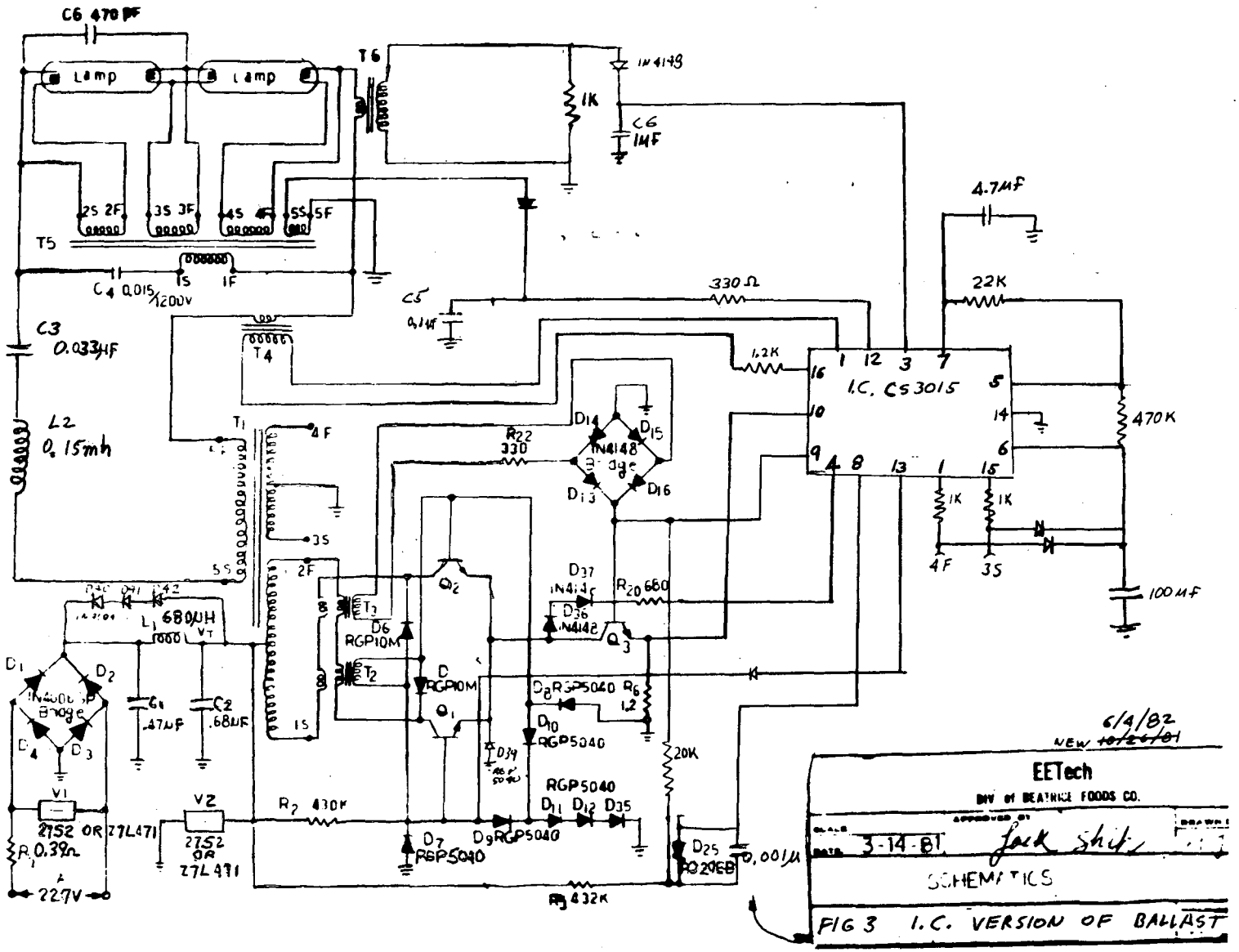
C6 470 pF
Lamp
Lamp
T6
1N4148
1K
C6 1μF
4.7μF
T5
C4 0.015/1200V
C5 0.1μF
330Ω
22K
C3 0.033μF
T4
1.2K
I.C. CS3015
470K
L2 0.15mh
T1
R22 330
D14
D15
1N4148 Bridge
D13
D16
1K
1K
4F
3S
100μF
D37 1N4148
R20 680
D36 1N4148
Q3
680μH
L1
D6 RGP10M
Q2
D1
D2
1N4001 Bridge
D4
D3
C1 .47μF
C2 .68μF
D RGP10M
Q1
D8 RGP5040
R6 1.2
D10 RGP5040
D34
20K
V1
2752 OR Z7L471
V2
2752 OR Z7L471
R2 430K
D7 RGP5040
D9 RGP5040
RGP5040
D11
D12
D35
D25 RGP20EB
0.001μ
R1 0.39Ω
227V
R3 432K
6/4/82
NEW
EETech
DIV of BEATRICE FOODS CO.
3-14-81
SCHEMATICS
FIG 3 I.C. VERSION OF BALLAST

Figure 3.

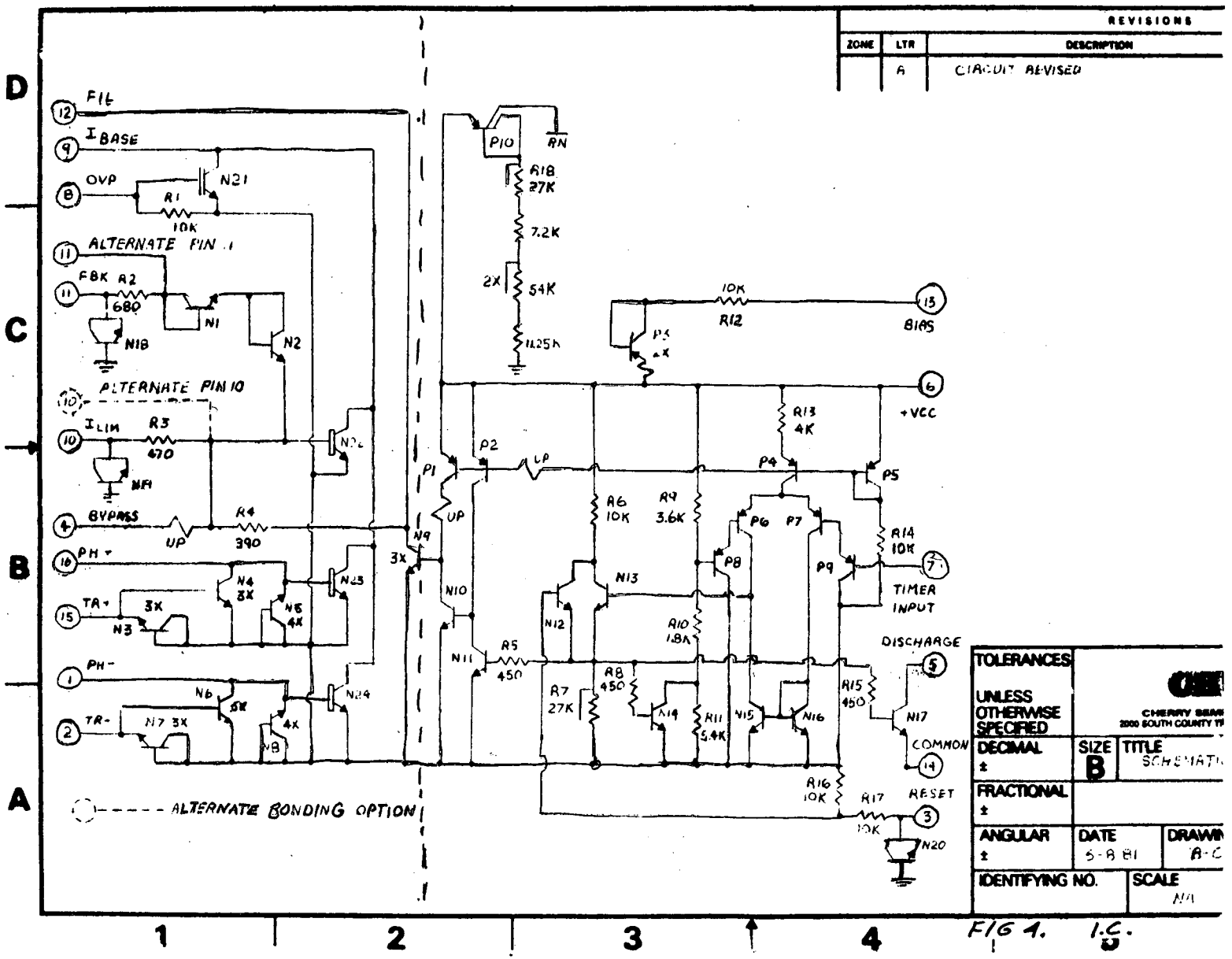
REVISIONS
ZONE
LTR
DESCRIPTION
A
CIRCUIT REVISED
FIL
IBASE
OVP
R1
10K
N21
ALTERNATE PIN 11
FBK
R2
680
N1
N2
N18
ALTERNATE PIN 10
ILIM
R3
470
BYPASS
UP
R4
390
PH+
TR+
N3
N4
N5
4K
PH-
TR-
N7
N6
N8
N24
N9
3X
P10
RN
R18
27K
7.2K
2X
54K
1.25K
P3
10K
R12
BIAS
+VCC
R13
4K
P1
P2
UP
N10
N11
R5
450
R6
10K
R9
3.6K
N12
N13
R10
1.8K
R7
27K
R8
450
N14
R11
5.4K
N15
N16
P4
P5
P6
P7
P8
P9
R14
10K
TIMER INPUT
DISCHARGE
R15
450
N17
COMMON
R16
10K
R17
10K
RESET
N20
ALTERNATE BONDING OPTION
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL ±
FRACTIONAL ±
ANGULAR ±
IDENTIFYING NO.
SIZE B
TITLE SCHEMATIC
DATE 5-8-81
SCALE N/A
CHERRY SEMI
2000 SOUTH COUNTY TR
FIG 4. I.C.

Figure 4.

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