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TIME-OF-FLIGHT MASS SPECTROSCOPY MULTIPLE STOP DIGITIZER: Instruction Manual

B.T. Turko

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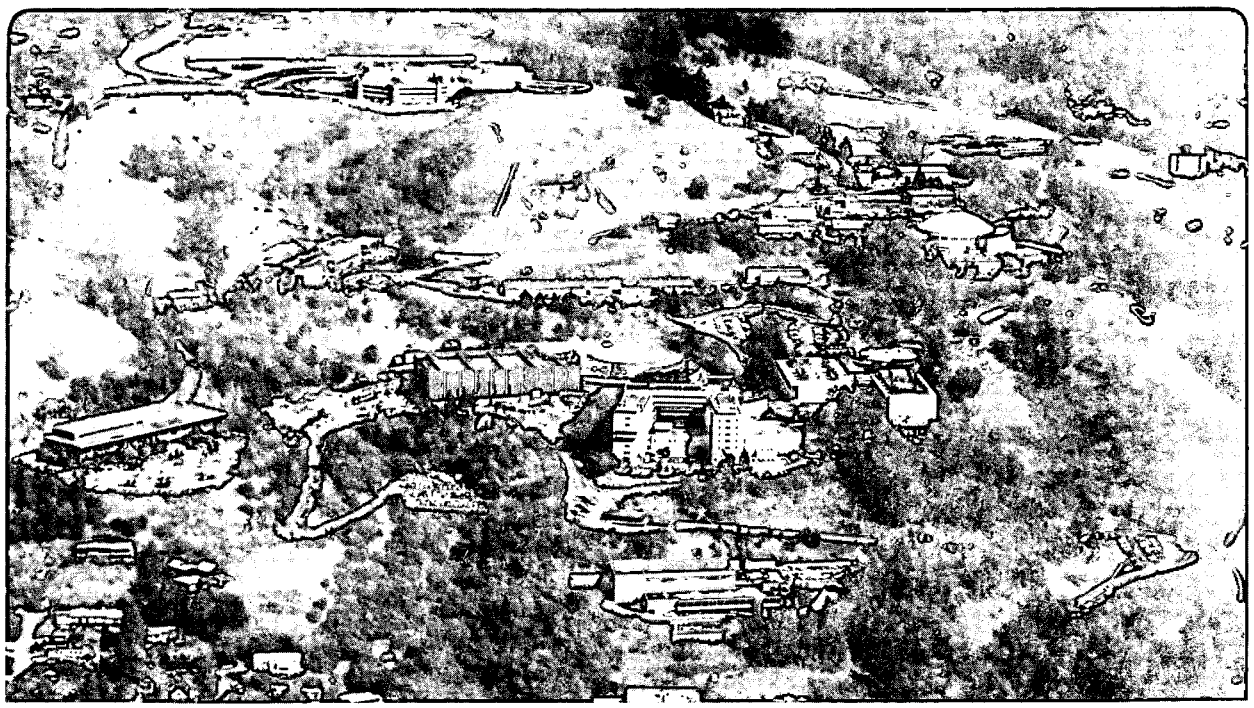

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TIME-OF-FLIGHT MASS SPECTROSCOPY MULTIPLE STOP DIGITIZER

Instruction Manual

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1. Introduction

A multiple stop time digitizer is described which was designed specifically for applications in plasma desorption time-of-flight mass spectrometry, (1-2). The digitizer is a high resolution time intervalometer capable of resolving bursts of stop events following a common start. The resolution of 78.155 ps is achieved over a time range 320 ms (max.). Stop event processing time takes less than one microsecond, enabling high resolution measurements of closely spaced bursts of events.

Multiple stop digitizers have been utilized previously in other fields of high resolution measurements of time intervals such as laser ranging (3-16) and high energy nuclear physics (17-22).

2. Multiple Stop Digitizer General Description

Basic operation of the digitizer is essentially analogous to a mechanical stop watch. The counting of a time interval is initiated by a start pulse. The time measured is expressed in increments equal to the period of an interval frequency reference. These increments are counted until a stop pulse is received. One problem is how to read-out the time interval without stopping the counting and thus lose the time reference to the start. Any number of stop pulses can arrive during the clock's time range. The readout and storage of an already accepted stop pulse takes some time. During this short processing time no stop of the counting can be tolerated and the counting of time must continue accurately. However, the stop deadtime defines the maximum stop rate. This assumes that an external data storage is able to absorb them all.

In order to keep not only the cost low, but also the size and power dissipation of such a clock small, a trade-off between the time range, incremental resolution and the stop deadtime must be made. The clock described here is modular, which makes for easier maintenance. Trouble-shooting is carried out simply by exchanging the suspected module by a spare. The modules conform to the widely used CAMAC standard system. Inexpensive CAMAC crates provide both the power and room for expansion. Although this digitizer is intended for use with an external data processing system, it can be easily interfaced with a number of modern data processors. Commercial hardware is available at a reasonable cost, both for additional, fast de-randomizing, temporary data storage and transfer to the processor.

The digitizer consists of three basic units. Each unit is complete in itself and contained in a separate module, requiring minimum interconnections. The units are a frequency standard module with a calibrating pulse generator, an analog interpolator module for the start and stop channels and a digital module containing counters, logic and interface circuits. A 50 MHz frequency standard has been selected. Although a higher frequency would be desirable since it would make possible higher resolution and a lower stop deadtime, 50 MHz is a practical limit of convenient low-power Schottky counting and logic circuits. An externally supplied frequency standard can be used an an alternative, for instance, when several digitizers are operating simultaneously. The digitizers thus operated become automatically calibrated and no correction for the difference in individual frequencies is necessary. It should also be pointed out that

digitizers in a group can serve as the master frequency source, supplying the reference to the other units.

Range of the digitizer is defined by counting coarse 50 MHz clock pulses. A maximum time interval of 335.36 ms is covered by a 32-bit binary number. Shorter ranges in any multiple of 5.12 μs can be preselected. The minimum time range is 5.12 μs. Once initiated by a start pulse, the digitizer cannot be stopped until the end of the selected range is reached. A master clear sequence is then generated and the digitizer restored into the armed state, awaiting a new start pulse. A manual master clear overrules all other functions and resets the digitizer immediately.

Many interpolation techniques have been used to increase the incremental resolution of the time measurements (16). Linear stretching of time intervals smaller than a full reference frequency period has been employed previously with very good results. The interval stretching gives the same result as though the whole measured time interval were digitized by a much higher reference frequency. For instance, a stretching factor of 256 is equivalent to increasing the 50 MHz reference frequency to 256 x 50 = 12,800 MHz.

When using this stretching, the digitizer is paralyzed for the duration of the conversion time. It would take 5.12 μs in order to stretch by a factor of 256 times an interval close to the reference frequency period. Such long conversion times are prohibitive in typical time-of-flight measurements where closely spaced bursts of stop pulses are often expected. Deadtime of a system may greatly increase the length of an experiment which must accumulate statistically sufficient data.

Substantial deadtime reduction has been accomplished by multiple successive interpolations of time intervals fractions smaller than the clock pulse period (15). Even two successive interpolations are sufficient to reduce drastically the conversion deadtime. Additional conversion time reduction is also possible by starting the conversion of a new event while the second stage of the preceding event is still in progress. Two successive 16-time stretchers result in 72.125 ps incremental resolution of the time measurements using a reference frequency of 50 MHz. The conversion deadtime is only 320 ns. A single step stretcher would require 5.12 μs deadtime for the same resolution at the same reference frequency.

The short deadtime of the dual interpolation technique yields another important advantage. The same circuit can be used for the interpolation at both the start and the end of the measured time interval. A stop input will

be enabled only after the acceptance of the start pulse. Therefore, the interpolator which first serves the start circuit at the beginning of the time measurement can be switched to the stop circuit as soon as the start conversion is completed. The interpolator remains serving the stop pulses until the end of the time range. The master clear at the end of the time range switches the interpolator back to the start input.

The difference between the stop and the start interpolation is computed and the coarse counting of the reference clock intervals is taken into account for a readout of the measured start-stop time interval. Thermal drift of the interpolator is automatically fully compensated. In other multiple stop digitizers employing separate start and stop interpolators imperfect thermal tracking may be a major source of time error. Also, a change of average stop rates can cause additional drift because the start pulse rate usually remained the same while the stop event rate may vary. The time accuracy of the digitizer with a common dual interpolator is virtually equal to the specifications of the reference frequency source.

The photograph of the Time-of-Flight Mass Spectrometry Multiple Stop Digitizer is shown in Fig. 2.1 and its general block diagram in Fig. 2.2. The digitizer comprises three double-wide modules housed in a CAMAC minicrate. The crate provides only the power to the modules. The few module interconnections are made with 50-ohm miniature cables in the rear. One half of the space in the minicrate is available (up to six CAMAC slots) to the user. Alternatively, this free space can be used for one more digitizer.

The three modules of the digitizer are Clock and Calibrator, Tandem Stretcher (i.e. a dual interpolator) and Logic Module.

The first two modules are shown on the left end of Fig. 2.2. The <u>clock module</u> contains, as has been pointed out, an accurate interval frequency reference of 50 MHz. A front panel input and operation mode switch are provided in case an external frequency source is used for running the digitizer. Also, a clock output is available for frequency monitoring purposes or for driving another digitizer. An independent precision calibrator is located in the same module. Basically, the calibrator is a divide-by-n counter, programmable by a 10-position front panel switch. The calibrator can handle any frequency up to 100 MHz, supplied externally. The output of the calibrator is a train of fast NIM pulses, appearing after every n^{th} period of the input frequency. Therefore, the output pulse separation is as accurate and as stable as the external frequency source.

The calibrator output can be used for driving the start and stop inputs of the digitizer. Any number of stops following a start can be digitized and the measured time compared with the reference frequency, making possible a quick and reliable procedure for the check-up and calibration of the digitizer. The digitizer's own clock output can be used for driving the calibrator. The operation of the digitizer is then in full synchronism with the clock, simplifying greatly the trouble-shooting and repair. The tandem stretcher expands the small time fractions, which are smaller than a clock period, remaining at the start and the stop end of a measured time interval. The time expansion takes place in two steps, greatly reducing the conversion time. The operation of this stretcher is explained in the next section. The start-stop separation is computed after each counting is completed. The stretcher is then cleared (CR) for another event.

The same stretcher serves both start and stop events. The start input is enabled first by the central logic (EN), preventing at the same time the acceptance of any stop pulse. The start conversion event takes place after the acceptance of the start pulse. The event is digitized by the "coarse" and "fine" start counters in the logic module (Fig. 2.2). Also, the counting of time in reference clock periods is started first in the auxiliary counter (AC). During the counting of 32 preset pulses (640 ns), the "coarse" start interpolation (and the "coarse" start counting) is completed. The "fine" start conversion and "fine" start counting takes place immediately afterwards. The main counting of clock periods is switched from the auxiliary to master counter (MC_1). The 640 ns of the auxiliary counting time is also added to the master counter. In the meantime, the control logic enables the stop input of the stretcher and the start input is disabled for the rest of the digitized time range. Soon after the end of auxiliary counting, a clear (CR) signal enables the stretcher. A stop event can now be accepted. Detailed timing sequence is given in the following section.

The master time counting is switched to the auxiliary counter again as soon as a stop event is accepted. The control logic routes the stretcher's "coarse" conversion gate to the "coarse" stop counter. The "coarse" data is transferred to the "coarse" stop register when the counting is completed. The master counter data is also transferred to the master register (MR). The anticipated missing 32 counts of the auxiliary counter are now added to the master counter, before the counter resumes the operation. The master counter starts again immediately after the 32nd auxiliary counter

pulse. No time is lost and the timing remains referred to the original start pulse, no matter how many stop events have been digitized before the end of the time range. The stretcher is again cleared and the stop input enabled after the master counter continues. Although the "fine" conversion is still taking place (and the "fine" stop continuing), the stop input of the stretcher is already enabled and a new stop event can be accepted. Two stop events can be digitized in tandem, reducing greatly the conversion deadtime.

"Fine" data is the last in the digitizing of an event. Arithmetic operations take place in the adder (AD) as soon as the "fine" register is strobed in. Eventually, the result appears on the binary front panel LED display and the are available for transfer to an external storage. It is essential that the data be transferred in less than one microsecond and the register cleared since only two stop events can be retained simultaneously by the digitizer. A "FIFO" type external memory is advised in case bursts of closely spaced stop events are expected. The stretcher stop input remains disabled as long as both previous stop events remain in the digitizer. Variable stop deadtime may result, complicating statistical analyses of the measured time spectra.

Basic time sequence of events in a typical time-of-flight operation of the digitizer is shown in Fig. 2.3. Both start and stop inputs can be gated, i.e. their acceptance may be conditioned by a coincident start gate pulse or stop gate pulse, respectively. Any gating pulse should appear at least a few nanoseconds before the leading edge of the start or stop pulse and last about five or more nanoseconds afterwards. All pulses are standard fast NIM signals, i.e. current pulses producing 0.5 volts across a 50 ohm load. All inputs of the digitizer are internally terminated by 50 ohms. The start or the stop input is independent of the gate signals if the corresponding front panel gate enable switch is in its "off" position.

The start pulse, when coincident with a gating pulse, can appear at any time (with respect to the free-running reference clock), provided the digitizer was previously initialized. An Event Busy signal appears at the tandem stretcher module front panel (Fig. 2.3, line 4) every time either a start or stop event conversion is in progress. The duration is fixed to about 800 ns. This output can be conveniently used for deadtime corrections, counting of the accepted events, gating of external fast logic and/or for monitoring purposes.

Two reference clock pulses (Fig. 2.3, line 1) after the start, a busy output (line 6) appears at the front panel connector of the logic module. This signal lasts until the end of the time range. An internal event ready pulse (line 7) is generated at the end of each interpolation, followed by the event clear (line 8) which prepares the digitizer for the acceptance of the next event. Master clear is generated automatically at the end of the time range. The digitizer is then ready for the acceptance of a new start pulse.

Random stop pulses (line 10) are shown, arriving at the times marked from a to n. The stop pulses not coincident with the stop gate (line 11) are immediately rejected (c,f,h). The stops at a and b are internally rejected because the stretcher is still busy with the interpolation of the start pulse. The stop at d is the first one to be accepted, meeting all the conditions. (The logic module enabled the stop input and disabled the start input by sending the stop enable signal [line 0] to the stretcher.) The accepted stop produces another event busy. The data is strobed into the buffer register at the end of conversion (line 12), and the register ready (line 13) sent to the external data storage. The buffer retains the data until cleared externally after the data transfer is completed (line 14). The next accepted stop at g (line 10) is also strobed into the buffer memory, but remained there since no external clear came in the time range. The third stop at k was still processed, but remained stored in the master register. Next eligible stop arriving at m was rejected because all registers still retain two preceding stops. Event busy signal (line 4) remains low. Such overload conditions can be monitored by an oscilloscope.

3. Low Deadtime Tandem Interpolation Technique

Time resolution of only 20 ns can be achieved if the 50 MHz reference clock frequency pulses are counted during the measured time interval. Various interpolation techniques were used to obtain resolutions of only a fraction of the period of the reference frequency (16 - 18). In order to get a resolution of 80 ps for instance, the residual time fractions of the measured interval smaller than 20 ns, the clock period must be stretched 256 times. The stretched intervals are then digitized by counting the clock pulses as is done in well-known Wilkinson-type analog-to-digital converter. The conversion time, however, is prohibitively long for the application in a short deadtime multiple stop time digitizer. A variant of the tandem interpolation technique (15, 21, 22) is used in this digitizer, resulting in about tenfold deadtime reduction.

The principle of tandem interpolation technique is shown in the timing diagram of Fig. 3.1. A pair of Event Start and Stop pulses (line B) defines the measured interval duration, T_{ak}. The points a and k at which the two events occur are uncorrelated to the free-running reference clock pulses (line A). Upon the acceptance of the start pulse, the Event Busy signal is generated (line C) as a Tandem Interpolator output for timing and monitoring purposes. No other event can be accepted until the end of this signal.

The measured interval, T_{ak}, can be divided into three segments, T_{ab}, T_{bl} and T_{kl}, respectively:

$$T_{ak} = T_{ab} + T_{bl} - T_{kl} \qquad (1)$$

T_{ab} is the section from the beginning of the start till the second following clock pulse (lines A and B) and T_{kl}, the section from the beginning of the stop pulse and the second following clock pulse. The section T_{bl} is thus synchronized with the clock. The number expressing the time T_{bl} is thus an integer, obtained by counting the clock pulses between the points b and k. T_{ab} and T_{kl} vary, since the start and stop pulses are random with the respect to the clock. Each may vary from one to two clock pulses.

In order to save on conversion time, T_{ab} is first shortened by a fixed time delay $T_o/2$ = 10 ns and then expanded by a factor K_c = 16. The stretcher

is a capacitor charged by a constant current during $T_{ab} - T_o/2$ and then discharged to the initial level by a constant current K_c times smaller (line D). Therefore,

$$T_{ab} - T_o/2 = (T_{be} - T_{cd})/K_c \qquad (2)$$

A level-sensing discriminator generates a gating pulse defining the duration of the first, "coarse", step in the interpolation (line E). T_{cd} is the residual time interval between the end of "coarse" conversion and the second, following clock pulse at e. T_{be} can also be expressed as an integer, since its both ends are synchronized with the clock.

T_{cd} is first shortened by a constant delay $T_o/2$ - 10 ns and then interpolated once again in a "fine" stretcher (line G). The procedure and the circuits are the same as in the "coarse" conversion. Then

$$T_{cd} - T_o/2 = T_{ef} / K_f \qquad (3)$$

K_f = 16 is the "fine" stretching constant, selected identical to K_c. By substituting (3) into (2), we obtain

$$T_{ab} = (1 + 1/K_c)T_o/2 + T_{bl}/K_c - T_{ef}/K_cK_f \qquad (4)$$

A similar procedure is followed in the stretching of T_{kl} in the interpolation of the stop pulse:

$$T_{kl} = (1 + 1/K_c)T_o/ \ + T_{lo}/K_c - T_{op}/K_cK_f \qquad (5)$$

By substituting (4) and (5) into (1), the measured time interval T_{ak} can be expressed by

$$T_{ak} = T_{bl} + (T_{be} - T_{lo})/K_c - (T_{ef} - T_{op})/K_cK_f \qquad (6)$$

It can easily be shown (15) that the conversion time is minimum when

$$K_c = K_f = \sqrt{K} \tag{7}$$

where K is the ratio of the clock period T_o to the desired incremental resolution of the digitizer, T_{oi}. The reference frequency of 50 MHz (T_o = 20 ns) was selected so that low power digitial circuitry could be utilized. In order to get a resolution below 100 ps, $K_c = K_f = 16$ was selected. Incremental resolution of T_{oi} = 78.125 ps is thus obtained.

The interpolation of each event is thus defined by three pulses, T_1, T_2 and T_3, (lines F, K and H), that are precisely correlated to the reference clock frequency. These pulses are brought to a Control Logic circuitry (See also Fig. 2.2) where the difference between T_1 and T_2 produces a "Coarse" Start Counter gating pulse (line L in Fig. 3.1). The difference between T_2 and T_3 produces a "Fine" Start Counter gating pulse (line M). The counters operate for the duration of these pulses, counting N_{be} and N_{ef} clock pulses, resp. lines T and U. The start conversion is then completed and remains stored in the start counters for the rest of the selected time range.

Both start and stop events are served by the same interpolator. The switching of interpolator from the start to the stop input occurs during the start event conversion. A stop can be accepted as soon as this conversion is completed, i.e. after the end of the Event Busy/Valid Stop output signal (line C).

The start interpolation digitized the T_{ab} portion of the measured interval T_{ak} (line A). The interval T_{bl} is digitized by first feeding 16 clock pulses (from b to g) to an Auxiliary Counter. The clock pulses are switched to a Master Counter after the point g. The Master Counter is thus resting for 640 ns during each conversion of an event. The lost time is compensated for by adding a single count to the 6th binary stage of the Master Counter before the point g.

A stop event is received at the point k and the interpolation of T_{kl} started. The counting is switched to the Auxiliary Counter at l. The Master Counter idles, retaining $N_{bl} = N_{gl} + 16$ clock pulses (line S), representing the time interval T_{bl} (line A). This time is shifted into a Master Register before the Master Counter starts counting again at q. After

q the time is again referenced to b as though the Master Counter had never been interrupted.

The interpolator generates a pair of "coarse" and "fine" intervals, T_{lo} and T_{op}, i.e. a new set of control pulses T , T , T , which, in turn, define the number N_{lo} and N_{op} clock pulses counted by a "Coarse" Stop Counter and "Fine" Stop Counter, respectively (Fig. 2.2).

Dividing (6) by T_o and substituting $K_c = K_f = K_o$, we obtain

$$T_{ak}/T_o = N_{bl} + (N_{be} - N_{lo})/K_o - (N_{ef} - N_{op})/K_o^2 \qquad (8)$$

To facilitate the computing of binary numbers, the Eq. (8) can be rewritten into

$$T_{ak}/T_o = N_{bl} + (N_{be} + N_{lo})K_o^{-1} + (N_{ef} + N_{op})K_o^{-2} - C \qquad (9)$$

where $C = 2 \neq K_o^{-1} - K_o^{-2}$. Only adding operations are needed for the computing of T_{ak}/T_o. The constant C subtraction is simple, as explained later in the description of the Logic Module of the Digitizer.

4. Description of the System's Modules

The Multiple Stop Digitizer consists of three, two-wide CAMAC modules. The modules are housed in a standard CAMAC minicrate. Only power is provided by the crate. All interconnections between the modules are at the rear panels. The system's modules are designed to require a few 50-ohm cables distributing only fast signals. Analog and digital circuits are thus contained in separate modules, minimizing crosstalk. A rear panel connector is provided for the connection of the digitizer's output to an external data storage or digital processor. All other signal inputs and outputs, as well as other controls, are located on the front panels (Fig. 2.1).

There is enough room in the crate to accommodate an additional digitzer or other CAMAC-compatible modules if required in an experiment. The three modules of the Digitizer are the Clock and Calibrator, the Tandem Stretcher (i.e. an analog interpolator) and the Logic Module.

4.1 Clock and Calibrator Module

4.1.1 Clock

Only the Clock is an integral part of the digitizer. The Calibrator has no internal connections and operates independently of the Digitizer. The module is shown in Fig. 4.1 and its general block diagram in Fig. 4.1.2. The clock operates either on its internal 50 MHz reference frequency oscillator or on an external frequency source. Another digitizer may also be used to ensure identical time calibration of two or more digitizers operating simultaneously. The external reference frequency does not need to be 50 MHz. The digitizer typically operates in the reference frequency range from 25 to 60 MHz. A change in the reference frequency, fo, affects only the calibration (Eq. 9). The incremental resolution (the time calibration of the least significant bit) is always To/256 - 1/256fo.

The characteristics and temperature stability measurement of a typical internal reference clock are shown in Fig. 4.1.3. The clock frequency is converted into fast pulse trains by shaping circuits (Fig. 4.1.2 and 4.1.4). Outputs CK1 and CK2 feed the Tandem Stretcher Module and CK3 the Logic Module. A4 is an amplifier providing a fast NIM clock output signal at a front panel connector. The internal oscillator is turned off by a front panel switch when an external reference is used. A typical peak-to-peak amplitude of 1V is sufficient. It is advisable to disconnect the external source when the internal oscillator is used.

4.1.2 Calibrator

A block diagram of the Calibrator is shown in Fig. 4.1.2 and its schematic in Fig. 4.1.5. The Calibrator is a divide-by-n counter that provides accurate time mark pulses suitable for driving the start and stop inputs of the Digitizer. Any external stable frequency source can be used for driving the Calibrator input. The first counting stage divides the frequency by 4, followed by ten divide-by-eight stages. Ten ranges can be selected with a front panel switch. Every n^{th} clock pulse will appear at the Calibrator's output. The width of the pulses is half of the input frequency period. An output current amplifier delivers shaped marker pulses into two parallel 50-ohm lo-ds. The pulses conform to the NIM standards (16 mA, or 0.8V into a 50-ohm load). The outputs can feed the start and stop inputs of the digitizer.

If the internal Digitizer clock reference f_o = 50 MHz is used for driving the input of the Calibrator, the following time ranges can be generated (in multiples of the clock period $T_o = 1/f_o$ = 20 ns):

Pos.	Range	n	2^n	$T=2^nT_o$
1.	A	2	4	80 ns
2.	B	5	32	640 ns
3.	C	8	256	5.120 µs
4.	D	11	2048	40.96 µs
5.	E	14	16384	327.68 µs
6.	F	17	131072	2.62144 ms
7.	G	20	1048576	20.97152 ms
8.	H	23	8388608	167.77126 ms
9.	I	26	67108864	1.34217728 s
10.	J	29	536870912	10.73741824 s
11.	K	32	4294967296	85.89934592 s

Range K is optional. It can be obtained by sacrificing one of the ten remaining ranges, since there are only ten selector positions available.

The two connecting cables have to be of the same length in order to prevent a time offset. On the other hand, very small propagation delays and time differences can be readily measured.

The Calibrator provides a very useful tool for trouble-shooting the Digitizer. By using the Clock's reference frequency output to drive the Calibrator, the start and stop signals to the Digitizer will be synchronized with the reference

clock frequency. Consequently, all points can be easily tested with an oscillosocpe. A complement Calibrator is provided for the external triggering of the oscilloscope.

A photograph of the Clock and Calibrator P.C. board is shown in Fig. 4.1.6 and the component lay-out in Fig. 4.1.7. Component lists are provided on the pages following the drawings.

4.2 Tandem Interpolator Module

This is the analog module of the Digitizer. Tandem interpolation technique is based on stretching small, less than one clock pulse long time intervals by a factor of 256. The equivalent frequency of the time digitizing is greatly increased by means of this method. The Digitizer's clock period, in effect, decreased from 20 nsecs to about 7.8 psecs. Tunnel diodes are used in the most critical circuits(Figs. 4.2.3 to 4.2.5), such as the conversion discriminators, the Busy Latch and the synchros, improving significantly linearity and jitter-free time interval measurement.

The Busy Latch is set each time an event is accepted (Fig. 4.2.2). The latch is cleared by the Logic Module each time after an event is processed and data transferred from the Event Register to the Buffer Register of the logic module. As long as the Event Register is busy, no new event can be accepted (Fig. 2.2).

The Busy Latch can be set by either a start or stop events passing the OR-gate G8. The status of the gates G7 and G10 defines which signals will be accepted at any given time. G7 controls the acceptance of start events. The gate G7 must also be enabled internally by the logic circuits. A coincident Start gate front panel pulse is also needed to start the digitizer, unless this condition is eliminated by setting a front panel switch which will permanently enable the OR-gate G6.

Similar logic applies for the Event Stop and Stop Gate inputs. G10 remains enabled and G7 disabled by the logic module for the duration of the time range.

Busy Latch opens the gate G11 after a delay of $T_o/2$ = 10 ns. A constant current source is turned on in the Coarse Stretcher, charging a capacitor with a constant current. The charging stops when G11 is closed by the "Coarse" Synchro circuit, latched on the leading edge of the second clock pulse following the event that had set the Busy Latch.

"Coarse" Synchro is a dual tunnel diode latch. The first clock pulse that passes G14, after the Busy Latch is set, locks the latch after a delay (D1),

making sure that the leading edge of the second clock pulse sets the latch G15 - G16. The closing of G11 starts the discharge of the memory capacitor by a constant current, which is exactly 16 times smaller than the charging current. The "coarse" time conversion is over when the capacitor charge returns to the initial level. A tunnel diode discriminator fires at this point, opening the gate G18 in the "Fine" Synchro. After a delay of 10 ns the next charging process starts in the Fine Stretcher. Two clock pulses later, the "Fine" Synchro latches and G12 is closed, stopping the charging of the memory capacitor and the "Fine" Stretcher discharge starts. The "Fine" Stretcher tunnel diode discriminator fires when the memory capacitor is discharged to the initial level. The "coarse" time conversion is thus defined by the signals T1 and T2 and the "fine" conversion by T2 and T3, as shown in the timing diagram, Fig. 3.1.

These three signals are fed to the Logic Module by coaxial cables where the "coarse" and "fine" stretched intervals are digitized. The small number of interconnections minimizes the interference from the digital module.

The interpolator module has a set of individual power regulators which enhance the stability and noise immunity of the stretcher.

The Tandem Interpolator circuit diagrams are shown in Figs. 4.2.3 to 4.2.6, a photograph of the module showing the components in Fig. 4.2.7 and a component lay-out drawing in Fig. 4.2.8. The figures are followed by the 8 pages of component lists.

4.3 Logic Module

The Logic Module contains all the digital and control circuits of the Digitizer. The panel of the module (Fig. 4.3.1) contains a row of 16 switches for presetting time ranges up to 320 ms in any binary combination of 5.12 μs. Data representing time between a pair of start-stop events are stored in two registers. A light-emitting diode array displays the data of the output (buffer) register. Either 16-bit group of a 32-bit binary word can be selected for the display by a switch. Two additional LED's display status of the registers. Two output signals (Busy and Valid Stop) can be used for the monitoring with an oscilloscope or for driving counters to determine real start and stop event rates for statistical corrections. Rear panel has 6 miniature coaxial connectors for the 50-ohm cables to the clock and interpolator modules. A 36-pin edge connector provides the connection for data transfer to external processors.

The main components of the logic module are shown in the general diagram (Fig. 2.2). The Control logic interprets signals from the Tandem Interpolator and Clock modules and generates a sequence of commands and clock pulse trains for each digitized start and stop event. Several counters digitize the pulse trains. Data is transferred into registers in order to release the counters for another event as soon as possible. Arithmetic operations take place along the data transfer to save time. The result is eventually stored in the final, buffer register, where it can wait indefinitely for the transfer to an external processor. In the meantime, the next event can be processed, but the result remained stored in transit registers. Unless the buffer register is cleared at the end of the conversion of the second event, the digitizer's input remains closed.

The Digitizer generates a master clear (MCR) at the end of the preselected time range. All counters and registers (except Buffer Register) are cleared regardless of their status, and the inputs set for the acceptance of a new start event. A more detailed block diagram of the Control logic is shown in Fig. 4.3.2. The counters, registers and arithmetic units are shown in Fig. 4.3.3. The timing diagrams showing the processing of two successive events are given in Figs. 4.3.4 and 4.3.5. The waveforms are referred to the appropriate points in the schematics (Figs. 4.3.6 - 4.3.10).

Each event is defined by a sequence of pulses, T_1, T_2, T_3, generated by the tandem interpolator. The leading edge of T_1 marks the event start and the beginning of "coarse" counting. The trailing edge of T_2 marks the end of "coarse" counting and the beginning of the "fine" counting, and the trailing edge of T_3 marks the end of the "fine" counting (Fig. 3.1). The control logic consists of latches, gates and delay circuits that provide a sequence of clock trains and pulses controlling the operation of the counters and registers.

The first event after a master clear is interpreted as a start. All the latches are reset and the counters preset to the time range as selected by the front panel switch combination. The pulse T_1 of the start event, passing gate G1, sets three latches (Master, "coarse" and Range). Gate G4 opens, passing clock pulses to Master and Auxiliary Counters until the end of the time range. A pulse is generated by G5 and delay D1 when the "Coarse" latch is set, which starts the counting in the Auxiliary counter first. The counting is switched automatically to the Master Counter after exactly 32 clock pulses. Gate G6 is also open, passing clock pulses to "Coarse" Counter.

The setting of the Range Latch controls the Tandem Interpolator, enabling the stop input and disabling the start input for the duration of the time range. At the same time, a NIM busy signal is available at the front panel connector, supplied by the translator, T_1.

Gate G7 opens at the end of T_2, setting the "Fine" Latch. At the same time it closes G6, ending the "coarse" pulse train. Gate G10 starts passing the clock pulses to the "Fine" Counter. A clock shaper, G11, is placed in series for reshaping of the last pulse of "fine" train. That last pulse can be generally of any width, since the closing of G10 by the end of T_3 (after the passing of G12) is not in synchronism with the clock frequency. The end of T_3 completes the start event conversion. The delay D3 makes sure that the counters have settled before the contents of "Fine" Counters is strobed into the "Fine" Register. The latch L5 is also set, disabling the "Fine" Start Counter and enabling the "Fine" Stop Counter for the next event, i.e. the first stop event following the start.

Status of the Auxiliary Counter is monitored by L6 and G14, setting the Master Register Latch. This status indicates that the contents of the Master Counter have been transferred into the Master Register and that the Master Counter has resumed counting. G13 takes into account that both the auxiliary and "fine" counting is over and that data are ready for transfer into the Buffer Register. Buffer Ready signal is sent to the external interfacing register and a "ready" indicator is lit.

A clear pulse is generated by a monostable multivibrator (SS2) when L7 is set, resetting the "coarse" latch, L6 and Tandem Interpolator. A separate clear loop is activated by G8 but only if "Coarse" Latch was cleared first. The "coarse" and "fine" clear cycles are thus separate, making possible a "coarse" conversion of a new event, while the "fine" conversion of the preceding event is still in progress. This sequence is important because it leads to a reduction in event processing deadtime.

An internal switch, S, is normally in "1" state and Enable Latch, L2, is "off" during the start event conversion. The start clear pulse thus passes G16, keeping the Buffer Latch reset and also clearing L7. The start event transfer is thus prevented. The start event clear pulse clears the Interpolator terminating T_1. G2 passes the trailing edge of T_2 setting the Enable Latch L2 which, in turn, disables G13 for the rest of the time range. G16 is prevented from clearing the Buffer Latch and, therefore, all subsequent stop events are read-out. L2 also disables the Start "Coarse" Counter and enables the Stop "Coarse" counter. Thus, both start "coarse" and "fine" counters retain the

original start event for the duration of time range.

The start event can be read out when the switch S is in "0" position. G16 is then inhibited all the time, and each event, the start one included, sets the Buffer Latch and a data transfer request. The start event alone represents, in fact, the digitized phase difference between the start pulse and the reference clock pulses. Proper alignment of the Tandem Interpolator is easily achieved by storing and sorting out random events in a data processor. Alignment procedure is described in Chapter 7.

The counters that digitize the start and stop events are shown in a block diagram (Fig. 4.3). In order to satisfy Eq. 9, each term was calculated separately. A complement of the "fine" start event, $\overline{N_{ef}}$, and the stop event, N_{op}, are summed up in the "Fine" Adder and brought as $\overline{N_{ef}} + N_{op}$ to the Adder. Similarly, the complement of the "coarse" start event, $\overline{N_{be}}$, and the "coarse" stop event, N_{1o}, are summed up in the "coarse" Adder" and the complement of the sum brought to the Adder, but shifted by $K_o = 16$ (i.e. by 4 bits). Finally, the content of the Master Counter, N_{b1}, reduced by 2 counts, is also added, but shifted by $K_o^2 = 256$ (i.e. by 8 bits). The subtraction of 2 counts takes care of a major part of the constant C in Eq. 9. After adding 1 (i.e. K_o^{-2}, or 1/256) to the least significant bit of the Adder, only K_o^{-1} or 1/16 remains uncompensated. This means that any time interval will be measured with an error of $+T_oK_o^{-1} = 1.250$ ns. A slightly longer cable in the stop input easily compensates for K_o^{-1}. Leaving both the start and stop cables equal helps the read-out of small, <u>negative</u> phase differences in some experiments.

A separate Range Counter counts each 5.120 μs carry pulse from the Main Counter. The Range Counter is preset by a preselected binary combination of 16 front panel range switches. A master clear initializes the Digitizer each time an overrun occurs, enabling the acceptance of a new start event. A front panel push-button master clear does the same. In either case, an event already stored in the Buffer Register remains unaffected.

The detailed timing sequences in Figs. 4.3.4/5 show a pair of start and stop events at various points in the circuit diagrams (Figs. 4.3.6 through 10). A photograph of the component side of the module is shown in Fig. 4.3.11, and

the component layout in Fig. 4.3.12, followed by the pages of component lists.

4.4 Powered CAMAC Crate

A Standard Engineering Corporation NINMA 400 Series Powered CAMAC crate provides power and housing for the Digitizer. Manufacturer's specifications and drawings are included in this section.

Only half of the available crate space is used. A complete additional digitizer can be placed into the remaining slots covered by blank front panels. Power drain of two digitizers and dissipation ware way below the specifications for the crate and no special cooling precautions other than those required by the manufacturer are necessary.

5. Test Results

Some of the tests performed so far are presented and illustrate the basic functions of the digitizer and a method for quick check-up during operation.

The digitizer was interfaced to a Multichannel Analysis System (Tracor Northern Model TN-1710) which serves, in this case, as a 4,096-channel random access memory with a line display. The memory increases by one the contents of an addressed channel. Four thousand channels cover a very small portion of the Digitizer's range. By dropping higher bits from the 13th on, any distant peak in a spectrum can be displayed. Bear in mind that all 4,096 channel-wide groups in the range will overlap and the results will require some interpretation. A multichannel oscilloscope connected to the Busy and Valid Stop output will help.

In the following examples an external 50 MHz clock was used to drive the calibrator. The external frequency was independent of the Digitizer's internal reference oscillator. The proper Calibrator and Digitizer range was set by the front panel controls.

Typical operation of the digitizer, as seen on an oscilloscope, is shown in Fig. 5.1. A time range of 20.48 μs was selected and the Calibrator rate was set for events 5.12 μs apart. Three accepted events are shown in the time range (top line). Tandem interpolator Busy output (middle line) shows a start followed by two stops. The bottom line shows Logic Module Valid Stop output. Data read-out was disconnected in this case. Consequently, Valid Stop and Interpolator Busy remain low after the acceptance of the second stop until the end of the time range, indicating that any new event cannot be accepted and processed.

In normal operation only stop events are processed. During the Interpolator alignment and some phase-related measurements, the start event is also transferred. This function is enabled by setting START ALIGN switch on the side of the logic module. Processed start events give the phase relationship between the leading edge of the start pulses and the reference clock frequency. For random starts the phase distribution is even (Fig. 5.2). If the interpolator alignment is proper, the histogram, covering 256 channels, should be made as flat as possible. The alignment procedure is described in Chapter 7.

In Fig. 5.3 the distribution of 40.960 μs start-stop intervals produced by the Calibrator is shown. The peak symmetry confirms the intrinsic triangular

channel profile (14). Fig. 5.4 shows the same peak in logarithmic scale. Some events scatter into adjacent channels because of internal noise (start and stop interpolation error) and the contribution of the external sources of noise (Calibrator and frequency source). The two channels to the right of the peak (27 334 counts) contain 4214 and 108 counts, respectively. The two channels to the left contain 5085 and 83 counts, respectively. Total time jitter amounts to about 15 ps, a fraction of the channel width of 78.125 ps. All other channels read zero.

Time jitter contribution of the Calibrator can be evaluated by overlapping a number of stop events following a start. Calibrator noise and frequency instability of more distant stops should result in broadening of stop event distribution. Fig. 5.5 shows a time range of 160 μs. A total of 31 stop events was accepted for each start. All of them merged into a single peak. Linear and logarithmic distribution of the same peak are shown in Fig. 5.6 and 5.7. The peak channel counts wer 384 197. The two upper channels from the peak counted 94 071 and 2937, respectively, and the lower channels counted 98 044 and 2488, respectively. Only slight increases in the distribution spread, compared with the single stop distribution of Fig. 5.3, indicates the very small effect of the Calibrator jitter. When very long Calibrator-generated time intervals are measured, the clock driving the Calibrator has to be of excellent stability and small phase jitter.

Overall linearity of the digitizer was tested by providing starts and stops that were random to each other and to the digitizer's internal reference clock. A Northern Scientific 4,096-channel memory was sufficient only for the shortest time range (5.12 μs). The resolution had to be reduced by a factor of 16 (by dropping the 5 least significant bits) to 1.25 ns/channel. The result is shown in Fig. 5.8. The first 743 channels, i.e. 928 ns, of the spectrum could not be used due to the start event processing deadtime. The droop at the end of the range is due to delayed Range Counter overrun command, caused by the Auxiliary Counter. The number of end channels affected is constant, regardless of the time range. These channels are normally eliminated by the processor during the data storing routine.

An expanded initial portion of the spectrum is shown in Fig. 5.9. Recovery from the preceding event's deadtime is linear and exactly one reference frequency clock wide (20 ns). Since 5 lower bits were dropped, each 16 channels merge into one, as shown in the photograph. This characteristic of the digitizer has to be taken into account when time corrections due to deadtime loss are computed for the peaks in complex time-of-flight spectra.

Laboratory testing of the Digitizer has been only performed to date. High resolution, short deadtime and long time range, which are characteristics of this system, require an access to a fast data storage and a large data processing system. Further testing and use of this system will be performed by the Texas A & M University.

6. Operating and Interface Instructions

6.1 Preliminary Testing

The Time-of-Flight Mass Spectrometry Multiple Stop Digitizer is a modular system housed and powered by a standard CAMAC crate. Prior to power turn-on, it is advisable to check for mechanical damages during shipment. Make sure that all modules are plugged in properly and that the front panel thrumbscrews are tight. Rear panel Interconnections should be checked. The miniature connectors have short threads and tend to lose contact unless tightened properly.

When the power is turned on for the first time, it is advisable to check the voltages at the front panel test points. Only four standard CAMAC voltages are used, i.e., I24V and I6V. Avoid placing the crate over a hot surface or in a stream of hot air.

6.2 Electrical Test

Testing of the basic functions can be performed without any external equipment. The use of an oscilloscope for monitoring BUSY and VALID STOP front panel outputs is helpful. Short coaxial cables are needed to connect CLOCK OUT to Calibrator INPUT on the Clock module. START OUT and STOP OUT should be tied to Tandem Stretcher's START and STOP inputs by two cables of approximately the same length. The clock switch should be on INT and the Interpolator switches pointing up, away from ON position (since no gating pulses are used). Unless the DISPLAY switch (Logic Module) is not in the central (off) position, some display LED will light after the power has been turned on. The LED's monitor the status of the buffer register which has no provision for clearing. Consequently, the status changes each time a new data is strobed into the buffer register.

Set all 16 of the RANGE switches (ON position) and RANGE switch (in Calibrator) to position 2. Both REG RDY and BUF RDY lights on the Logic Module should be on. The lights go off when INITIALIZE push button is pressed. The digitizer starts operating as soon as the push button is released. Next, put the switch under the START input of the Interpolator in its ON position. After pressing the the INITIALIZE push button, the REG RDY and BUF RDY lights go off and remain off, since no start event is accepted. Enable START again by placing the switch in the up position again. The digitizer starts working and the two ready lights are on again.

At the end of the time range after each start, an internal master clear signal is produced, causing continuous operation of the Digitizer, even though no external data read-out is connected. Each time, therefore, the status of the register will be updated, and the change of content, if any, can be seen on the data display. No data lights are on when the DISPLAY switch is in 17-32 position. In 1-16 position, the bit #15 and #5 will be on. Very small differences between the start and stop input cable lengths will result in adding or subtracting their delay time differential on the display.

Switching the Calibrator RANGE switch one step further (Position 3) does not cause a change on the display's lower bits. Only the LSB may change. The highest bit moves upward by 3 bits. Therefore, only the bits #20, #23, #26, #29 and #32 are on when the RANGE switch is stepped from the positions 4 through 8. The DISPLAY switch should be placed in the 17-32 position during this test. In the RANGE position 9 and 10, the spacing between Calibrator pulses exceeds the time range of the Digitizer. However, start pulses are still accepted. REG RDY light flashes each 1.28 second for the RANGE position 9 and each 10.24 second for the position.

6.3 Data Read-out

Data is transferred to an external register or processor via the edge connector at the rear of the Logic Module. Data pins are 1 (LSB) through 32 (MSB). BUFFER READY output (pin 33) and BUFFER CLEAR input (pin 34) provide the data transfer handshake. Pins 35 and 36 are ground return connections. Polarity of the transfer control signal can be selected by setting microswitches showing through the side cover of the module. The switches #4 and #5 should be set for positive signals and the switches #3 and #6 for negative signals. Detailed circuit diagrams are shown on the page 10 x 3061 S-1.

The Buffer output is wired for positive data outputs. If negative outputs are required, however, the output LS 365 drives D8, D9, D10, E8, E9 and E10 should be replaced by complementary chips LS 366 (page 10 x 3061 S-5). It is advisable to delay strobing into the external register until data transients settle down.

7. Alignment Procedure

7.1 Purpose of Alignment

Interpolation is an analog process of stretching small time fractions at the beginning and end of the measured interval in order to increase resolution of the measurement. Tandem interpolation, used in this digitizer, is a process of stretching the same time fraction twice. The final result is equivalent to a single interpolation, with drastically reduced conversion deadtime. The first "coarse" and the second "fine" interpolation expands the time fraction 16 times each. The total stretching constant is thus 16 x 16 = 256. The longest fraction equals one reference clock frequency period which is 20 ns. Since both stretchers are of Wilkinson type, each requires a constant current discharge adjustment. Offset adjustment is unnecessary since the start and stop offsets cancel each other.

7.2 Alignment Set-up

A free-running pulse generator providing start events only is needed. The rate should not be a subharmonic of 50 MHz, as beat effects can affect the results. Random or pseudorandom rates are preferable. The digitizer should be interfaced with a processor that is capable of sorting out start events into at least 270 memory addresses. The microswitch #1 on the side of the Logic Module should be set in order to enable the transfer of start event data.

7.3 Aligment

An alignment histogram for proper adjustment is shown in Fig. 5.2. Start events should be evenly distributed over 255 channels. Number of channels is adjusted by COARSE ALIGN trimpot on the Tandem Interpolator module. A periodic structure in the distribution is corrected by the FINE ALIGN trimpot until a flat histogram is obtained. The "fine" alignment may change the total of 255 channels, which is then corrected by an appropriate "coarse" adjustment. The procedure is reiterated until maximum flatness over a total of 255 channels is obtained.

Generally, an alignment is advised after long operation since some component aging may be expected. Also, if crate voltages have been altered, or if substantial change in ambient temperature has occurred, the alignment should be checked. Since the same interpolator is used for both start and stop events, the tracking error due to temperature and rate change is practically eliminated.

After alignment the distribution of a calibrating stop peak can be measured, following the procedure outlined in Chapter 5. The results should look like the peak in the Fig. 5.3.

8. Specifications Summary

8.1 Clock and Calibrator Module

Internal reference clock oscilloscope: ICM MOE-10	
Frequency	50.000 000 MHz
Calibration	±1 ppm (25°C)
Stability (-10° to 60°C)	±0.0005%
External clock reference input (50 ohm terminated)	1V (peak to peak)
Clock output (on 50 ohm load)	0.8V (fast NIM)
Calibrator input frequency	<65 MHz
Calibrator input (50 ohm input impedance)	0.8V
Start and Stop outputs (dual bridged NIM into 50 ohm	-0.8V (each)
Sync. output (int. impedance 10 ohm)	0.3V (open)

Ranges (for f_o = 50 MHz input frequency)

Pos.	Range	n	2^n	$T = 2^n T_o$
1	A	2	4	80 ns
2	B	5	32	640 ns
3	C	8	256	5.12 µs
4	D	11	2 048	40.96 µs
5	E	14	16 384	327.68 µs
6	F	17	131 072	2.621 44 ms
7	G	20	1 048 576	20.971 52 ms
8	H	23	8 388 608	167.771 26 ms
9	I	26	67 108 864	1.342 177 28 s
10	J	29	536 870 912	10.737 418 24 s
	K	32	4 294 967 296	85.899 345 92 s

8.2 Tandem Interpolator Module

Start input (50 ohm terminated, >5 ns)	-0.8V (NIM)
Start gate input (50 ohm terminated)	-0.8V (NIM)
Stop input (50 ohm terminated, >5 ns)	-0.8V (NIM)
Stop gate input (50 ohm terminated)	-0.8V (NIM)
Busy output (on 50 ohm load)	-0.8V
Coarse align: front panel potentiometer	
Fine align: front panel potentiometer	

8.3 Logic Module

REG RDY	Register ready LED
BUF RDY	Buffer register ready LED
INITIALIZE	Front Panel master clear push button

Display Switch:

1 - 16 position displays bits 1 (LSB) to 16

17 - 32 position displays bits 17 to 32 (MSB)

Calibration and Range:

Bit #	Calibration	Range	Bit #	Calibration
32	167.77216 ms	160 ms	16	2.56 µs
31	83.88608 ms	80 ms	15	1.28 µs
30	41.94304 ms	40 ms	14	640 ns
29	20.97152 ms	20 ms	13	320 ns
28	10.48576 ms	10 ms	12	160 ns
27	5.24288 ms	5	11	80 ns
26	2.62144 ms	2.56 ms	10	40 ns
25	1.31072 ms	1.28 ms	9	20 ns
24	655.36 µs	640 µs	8	10 ns
23	327.68 µs	320 µs	7	5 ns
22	163.84 µs	160 µs	6	2.5 ns
21	81.92 µs	80 µs	5	1.25 ns
20	40.96 µs	40 µs	4	625 ps
19	20.48 µs	20 µs	3	312.5 ps
18	10.24 µs	10 µs	2	156.25 ps
17	5.12 µs	5 µs	1	78.125 ps

Note: Range figures are approximate

Busy output (NIM)	-0.8V (50 ohm terminated)
Valid stop output (NIM)	-0.8V (50 ohm terminated)

Rear panel edge connector pin assignemtn

Pin #	Data	Pin #	Data	Pin #	Data	Pin #	Data
1	1 (LSB)	10	10	19	19	28	28
2	2	11	11	20	20	29	29
3	3	12	12	21	21	30	30
4	4	13	13	22	22	31	31
5	5	14	14	23	23	32	32 (MSB)
6	6	15	15	24	24	33	33 BUF RDY
7	7	16	16	25	25	34	34 BUF CLR
8	8	17	17	26	26	35	35 Ground
9	9	18	18	27	27	36	36 Ground

9. Figure captions

Fig. 2.1 Time-of-flight mass spectroscopy multiple stop time digitizer. A CAMAC minicrate provides housing and power to the modules. The modules are interconnected thin, 50 ohm miniature cables.

Fig. 2.2 Time-of-flight mass spectroscopy multiple stop time digitizer block diagram

Fig. 2.3 Basic timing sequence during a typical operation of the time-of-flight digitizer

Fig. 3.1 Tandem interpolation timing diagram for a pair of start-stop events

Fig. 4.1.1 Clock and calibrator module front and rear view

Fig. 4.1.2 Reference Clock and Calibrator module block diagram

Fig. 4.1.3 Internal reference clock oscillator characteristics and temperature stability

Fig. 4.1.4 Reference clock circuit diagram

Fig. 4.1.5 Calibrator circuit diagram

Fig. 4.1.6 Clock and Calibrator module component side view

Fig. 4.1.7 Clock and Calibrator module component layout

Fig. 4.2.1 Tandem Interpolator module front and rear view

Fig. 4.2.2 Tandem Interpolator block diagram

Fig. 4.2.3 Tandem Interpolator input circuit diagram

Fig. 4.2.4 Tandem Interpolator coarse stretcher circuit diagram

Fig. 4.2.5 Tandem Interpolator fine stretcher circuit diagram

Fig. 4.2.6 Tandem Interpolator power regulator circuit diagram

Fig. 4.2.7 Tandem Interpolator module component side view

Fig. 4.2.8 Tandem Interpolator module component layout

Fig. 4.3.1 Logic module front and rear view

Fig. 4.3.2 Logic module block diagram

Fig. 4.3.3 Logic module control logic block diagram

Fig. 4.3.4 Logic module timing diagram (first part)

Fig. 4.3.5 Logic module timing diagram (second part)

Fig. 4.3.6 Logic module input circuit diagram

Fig. 4.3.7 Logic module auxiliary counter and master counter (first part)

Fig. 4.3.8 Logic module master counter (second part) and range counter

Fig. 4.3.9 Logic module coarse and fine counters and adders

Fig. 4.3.10 Logic module final adder, line drivers and display

Fig. 4.3.11 Logic module component side view

Fig. 4.3.12 Logic module component layout

Fig. 5.1 Digitizer processing a start and two stop events in a typical sequence, as seen on an oscilloscope monitoring start BUSY, event BUSY and VALID STOP outputs

Fig. 5.2 Typical phase distribution histogram of start events Start events are at random with respect to the digitizer's reference clock. The photograph shows proper alignment of the interpolator, containing 255 evenly distributed channels. Calibration of a channel: 78.125 ps.

Fig. 5.3 Measurement of 40.960 μs time intervals. The counts in two adjacent channels indicate total jitter of less than 15 picosecond.

Fig. 5.4 Logarithmic display of the peak of Fig. 5.3 shows negligible spread of step counts into adjacent channels

Fig. 5.5 Measurement of 31-stop event bursts during a 160 μs time range. From top: Start busy (time range), Event busy and Valid stop oscillograms.

Fig. 5.6 Distribution of 31 overlapped stop events from Fig. 5.5 indicate only a slight increase of measured time jitter (compared to Fig. 5.3).

Fig. 5.7 Logarithmic display of stop events from Fig. 5.5. No increase in the width is noticed, although 31 stop events are merged into a single peak.

Fig. 5.8 Random distribution of start and stop events in 5 μs time range. Resolution is 1.25 ns/channel. Initial gap is due to the start event dead time.

Fig. 5.9 Expanded portion of random start and stop event distribution of Fig. 5.8. Recovery from deadtime is linear, indicating that start events were at random with respect to the digitizer's internal reference clock.

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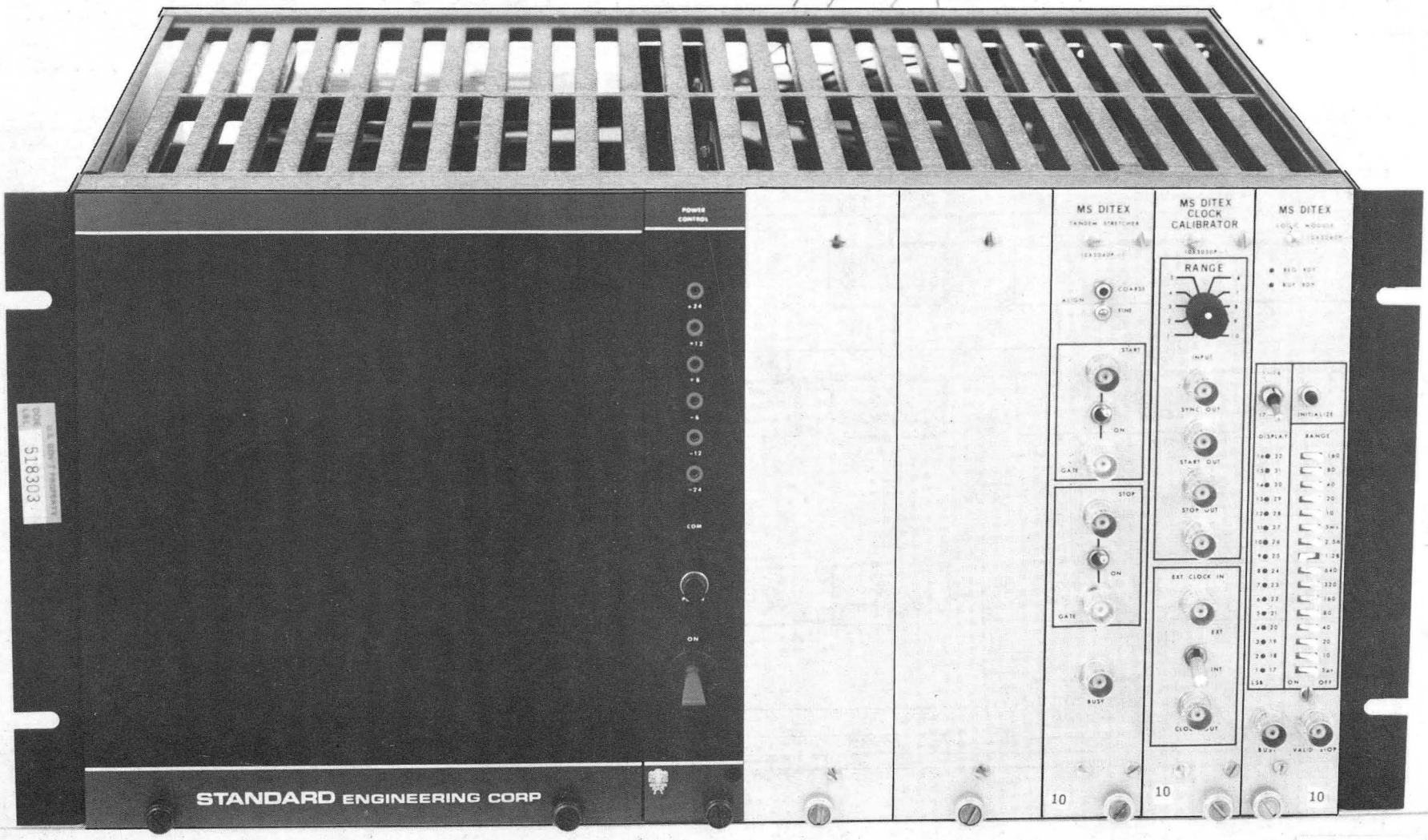
Standard Engineering Corp.
CAMAC Crate with Power Supply
Model No. PS425 or equivalent



XBB 812-1239A

Fig. 2.1 Time-of-flight mass spectroscopy multiple stop time digitizer. A CAMAC minicrate provides housing and power to the modules. The modules are interconnected thin, 50 ohm miniature cables.

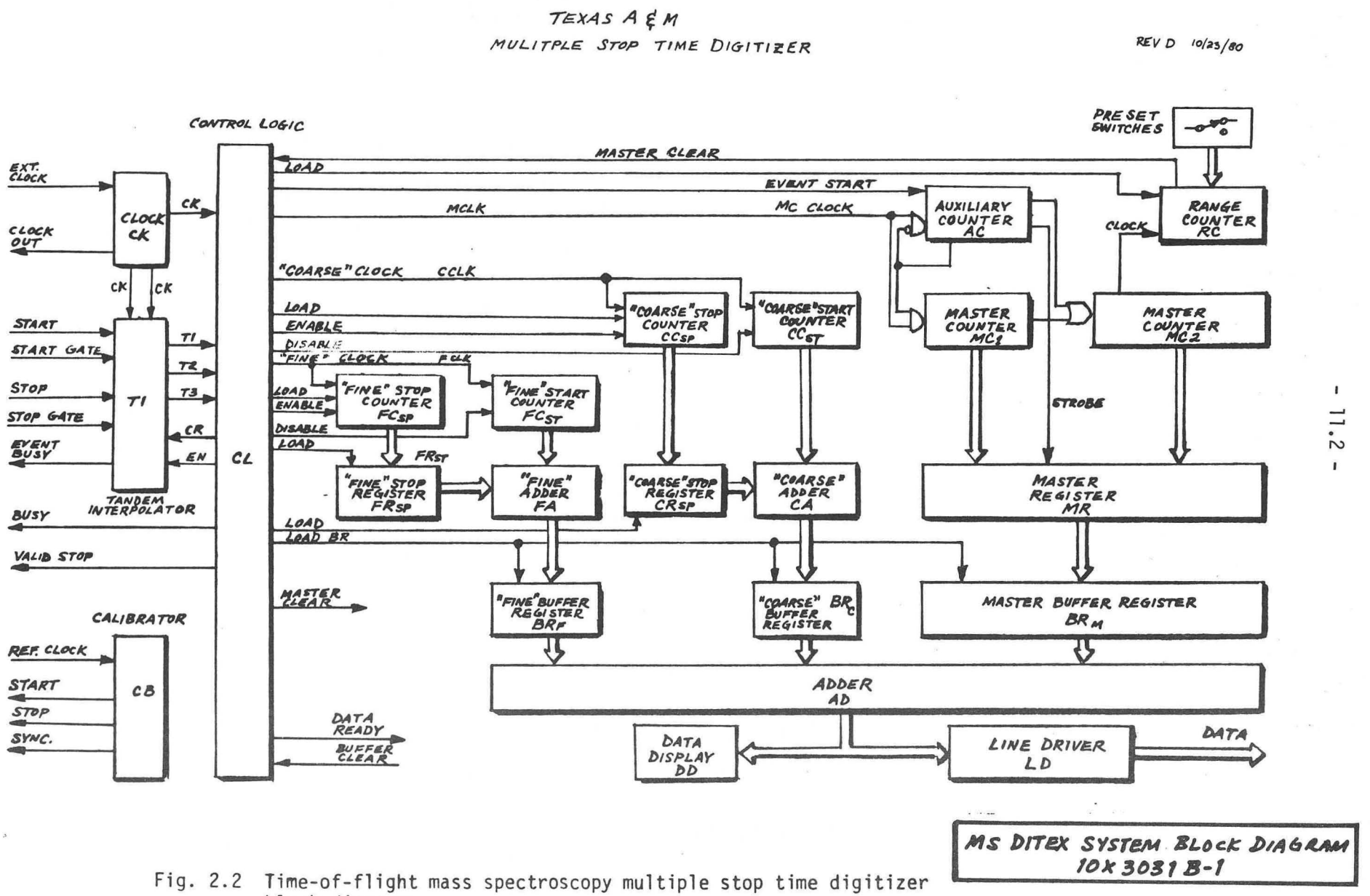


Fig. 2.2 Time-of-flight mass spectroscopy multiple stop time digitizer block diagram

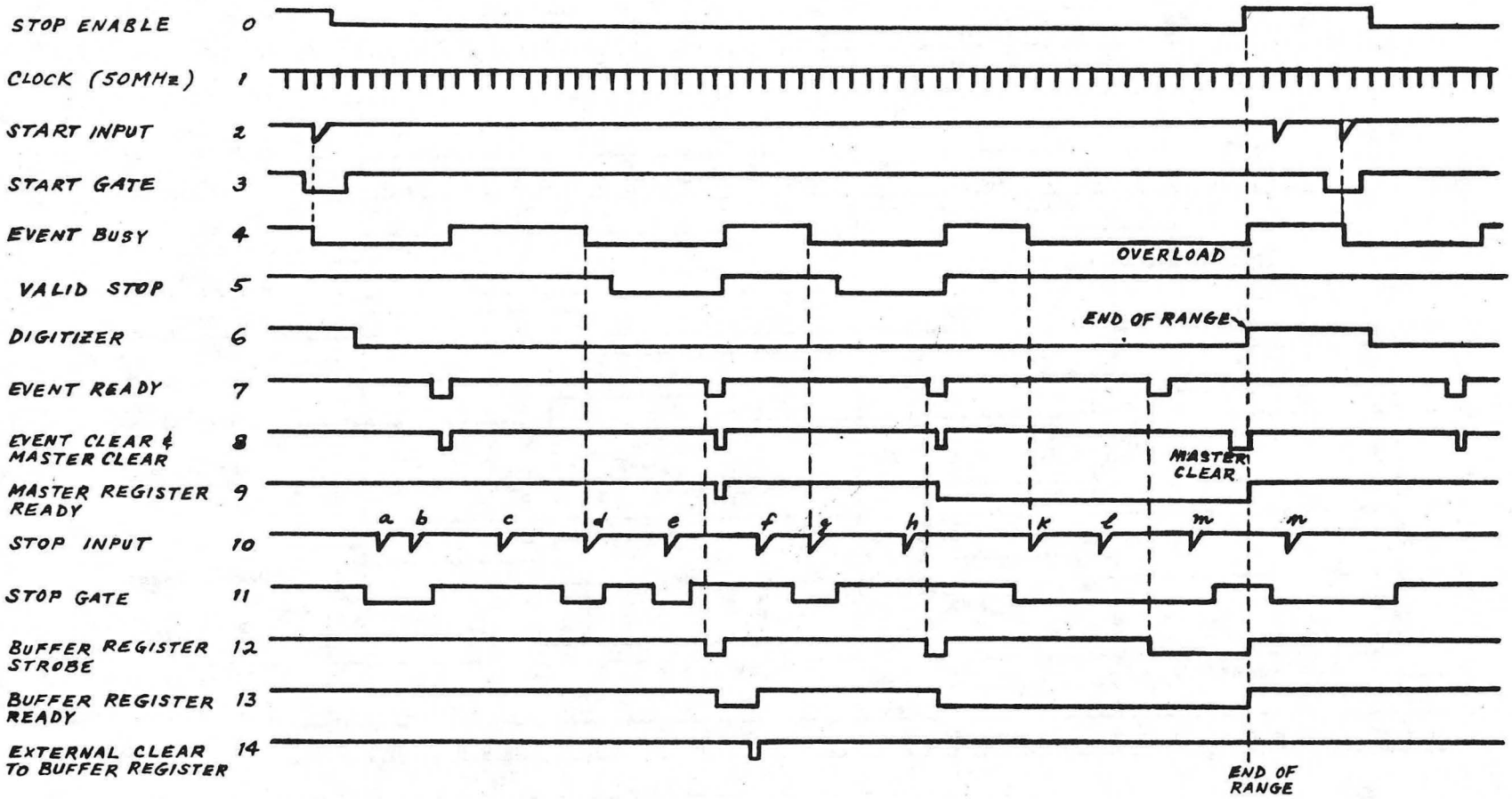


Fig. 2.3 Basic timing sequence during a typical operation of the time-of-flight digitizer

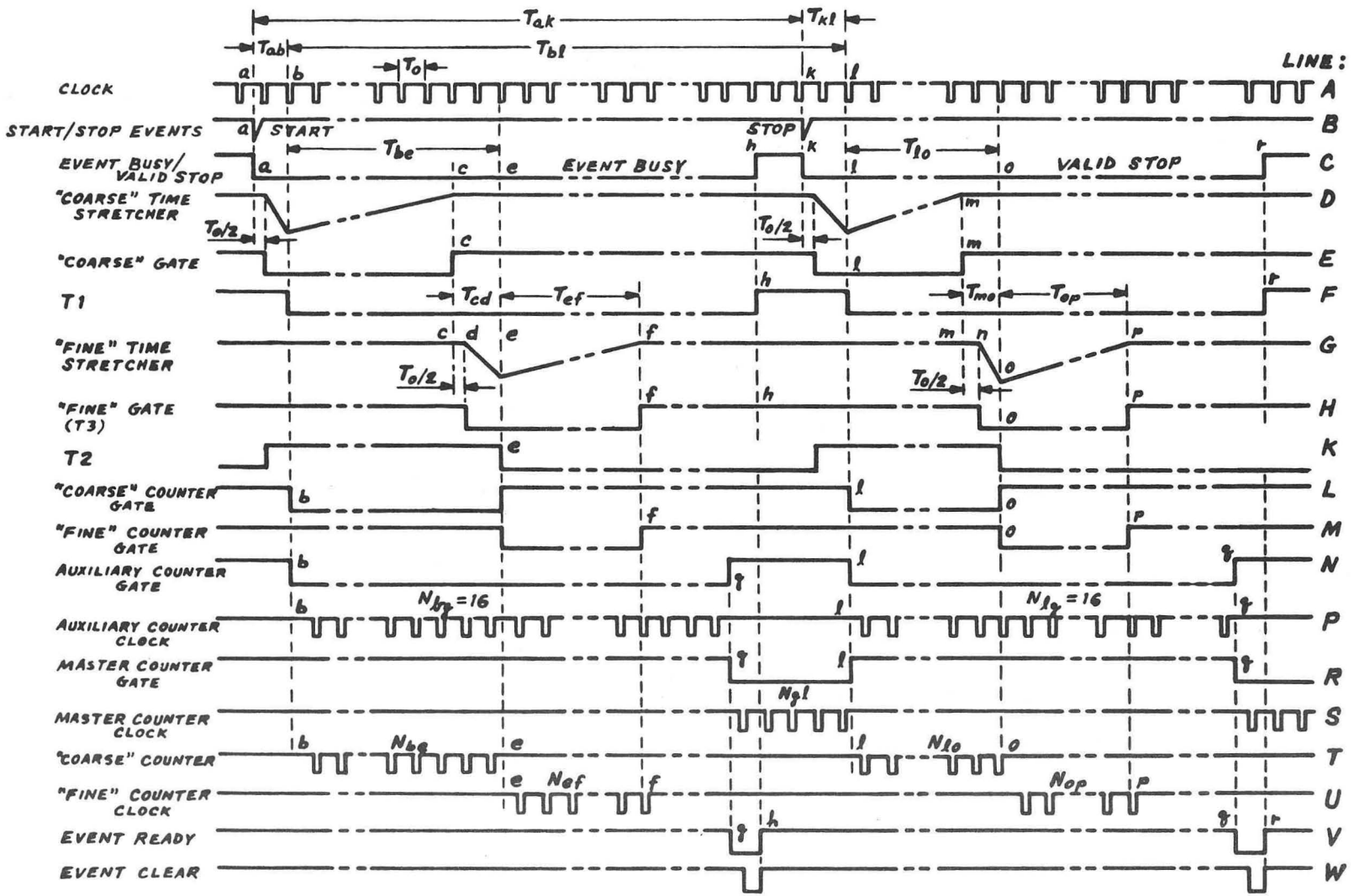
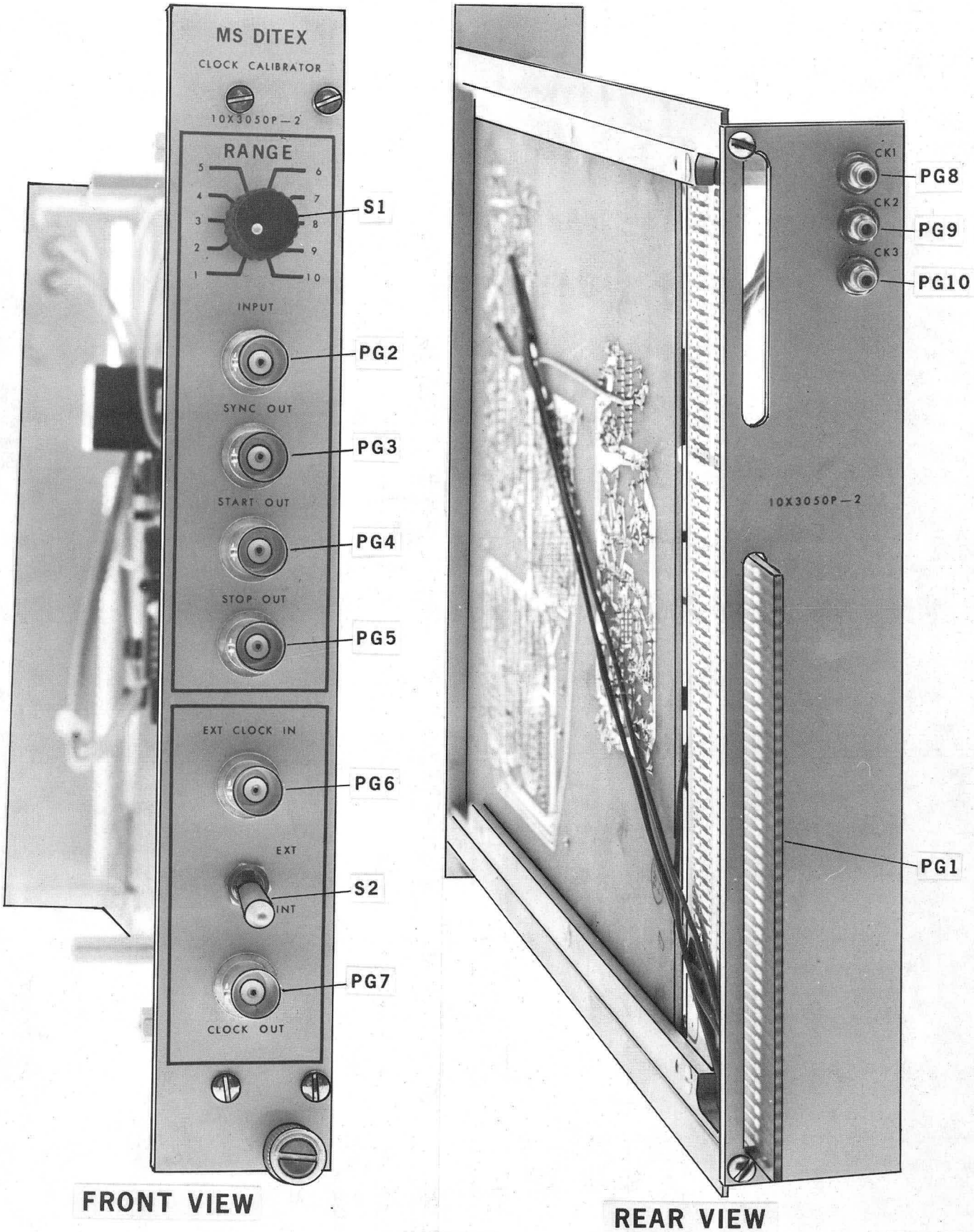


Fig. 3.1 Tandem interpolation timing diagram for a pair of start-stop events



MS DITEX - CLOCK CALIBRATOR
10X3051 A-1
DWG 1 OF 2

Fig. 4.1.1 Clock and calibrator module front and rear view

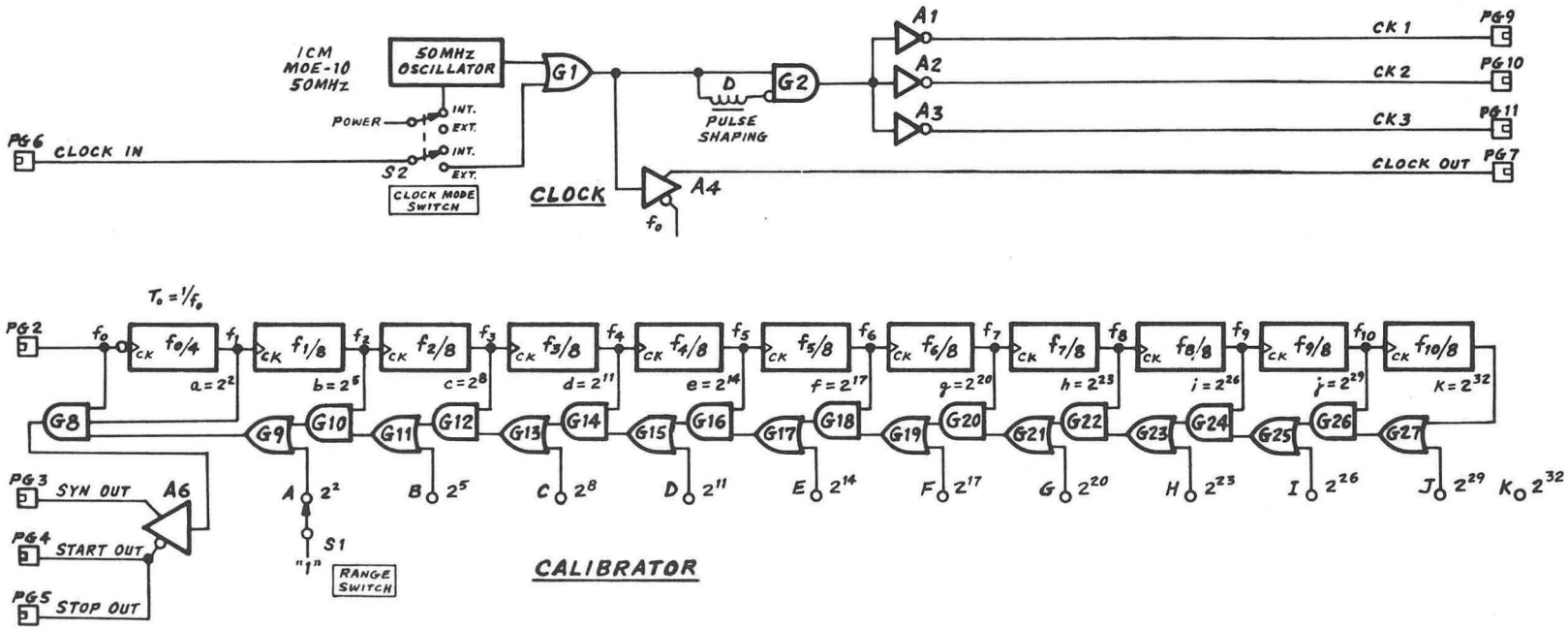


Fig. 4.1.2 Reference Clock and Calibrator module block diagram

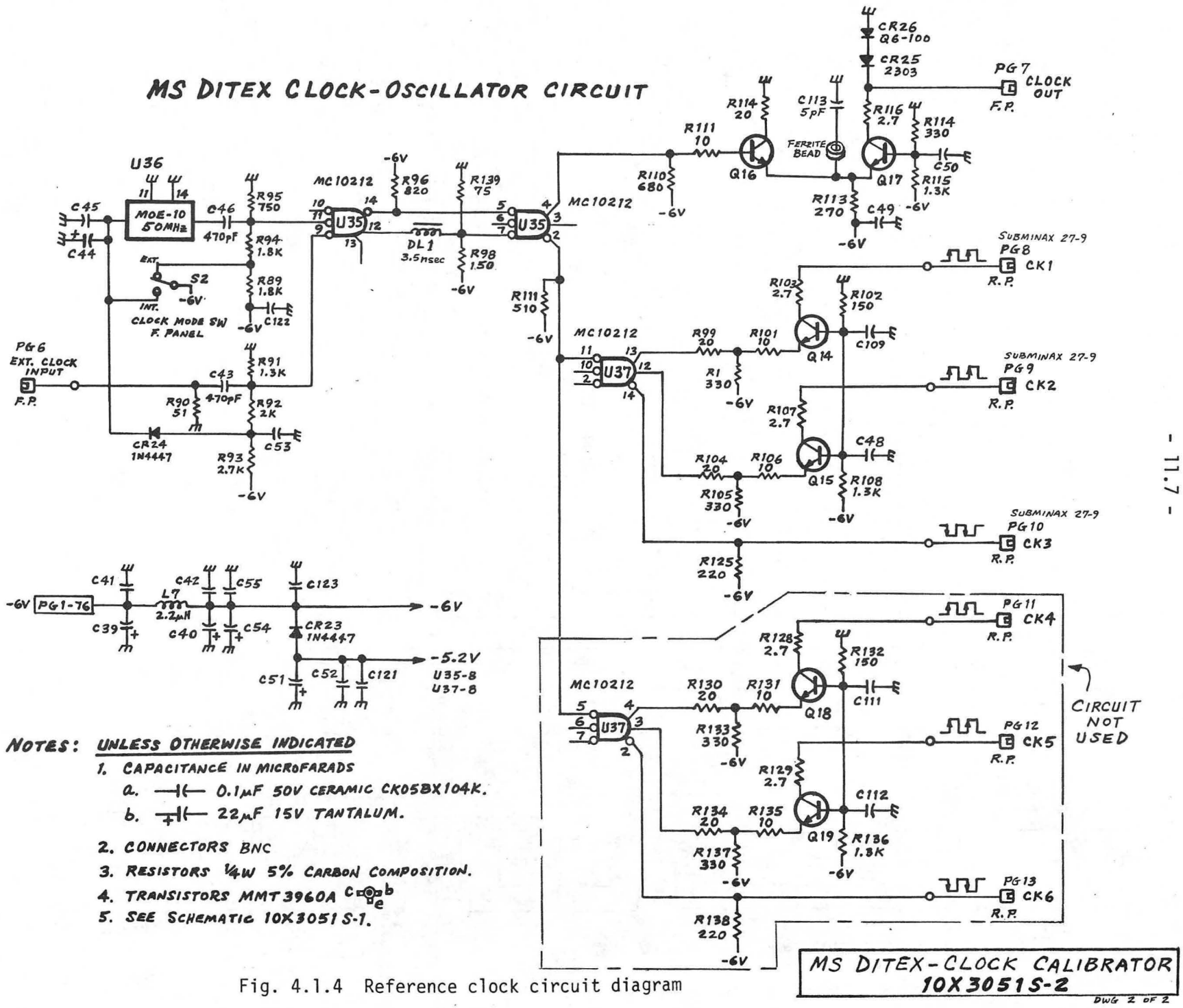
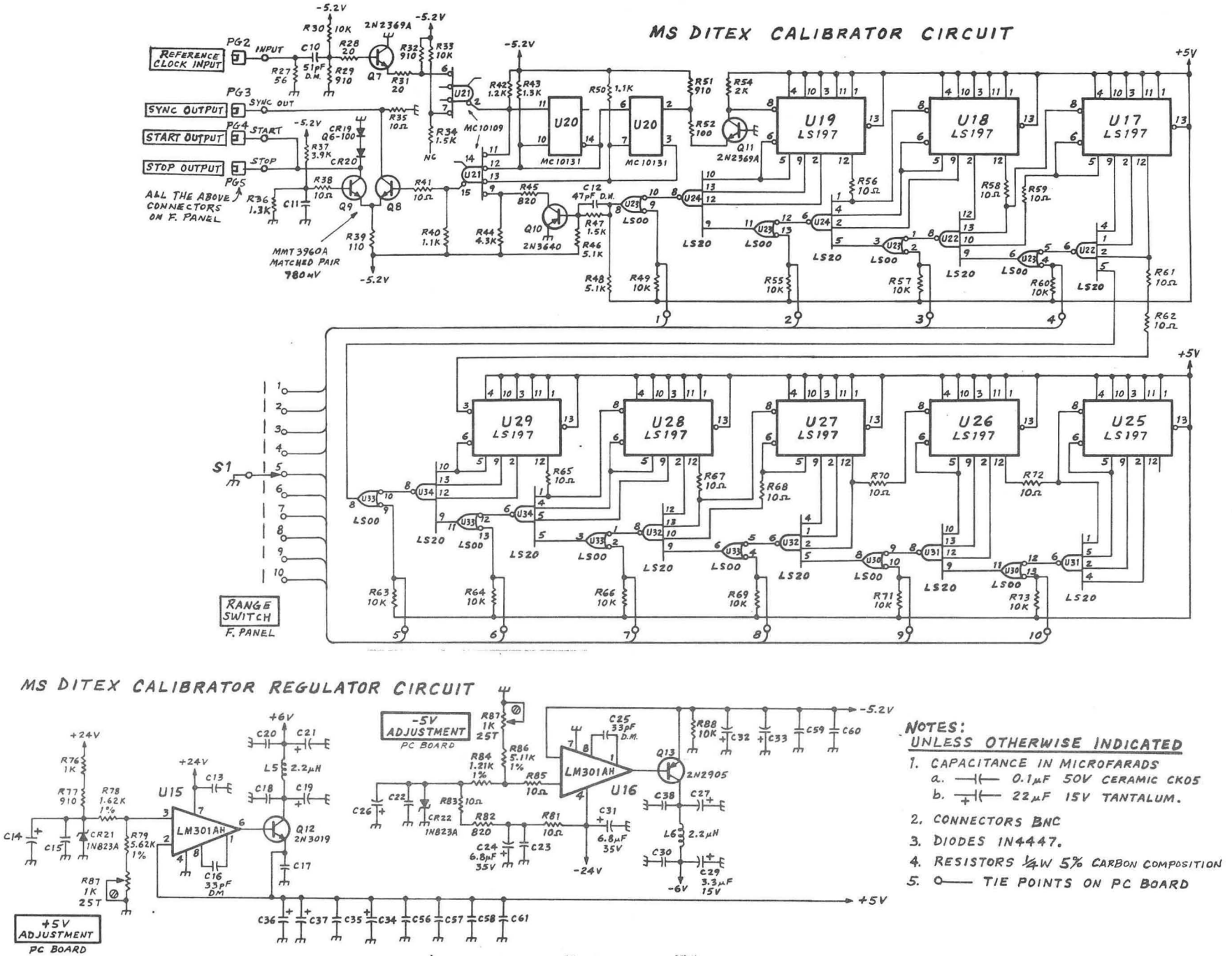
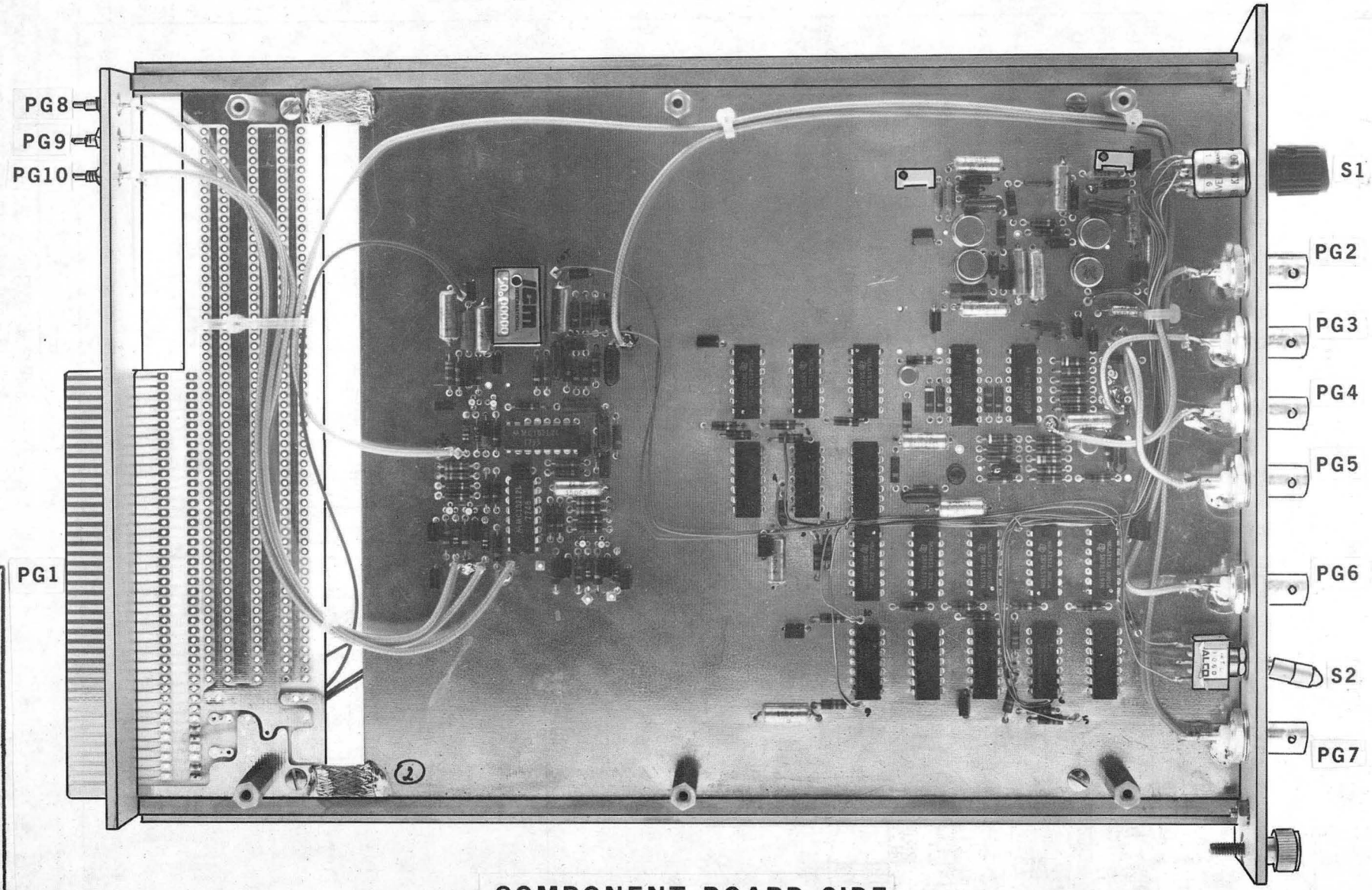


Fig. 4.1.4 Reference clock circuit diagram



MS DITEX-CLOCK CALIBRATOR
10X3051 S-1
DWG 1 OF 2

Fig. 4.1.5 Calibrator circuit diagram



MS DITEX - CLOCK CALIBRATOR
10X3051 A-2
DWG 2 OF 2

COMPONENT BOARD SIDE

Fig. 4.1.6 Clock and Calibrator module component side view

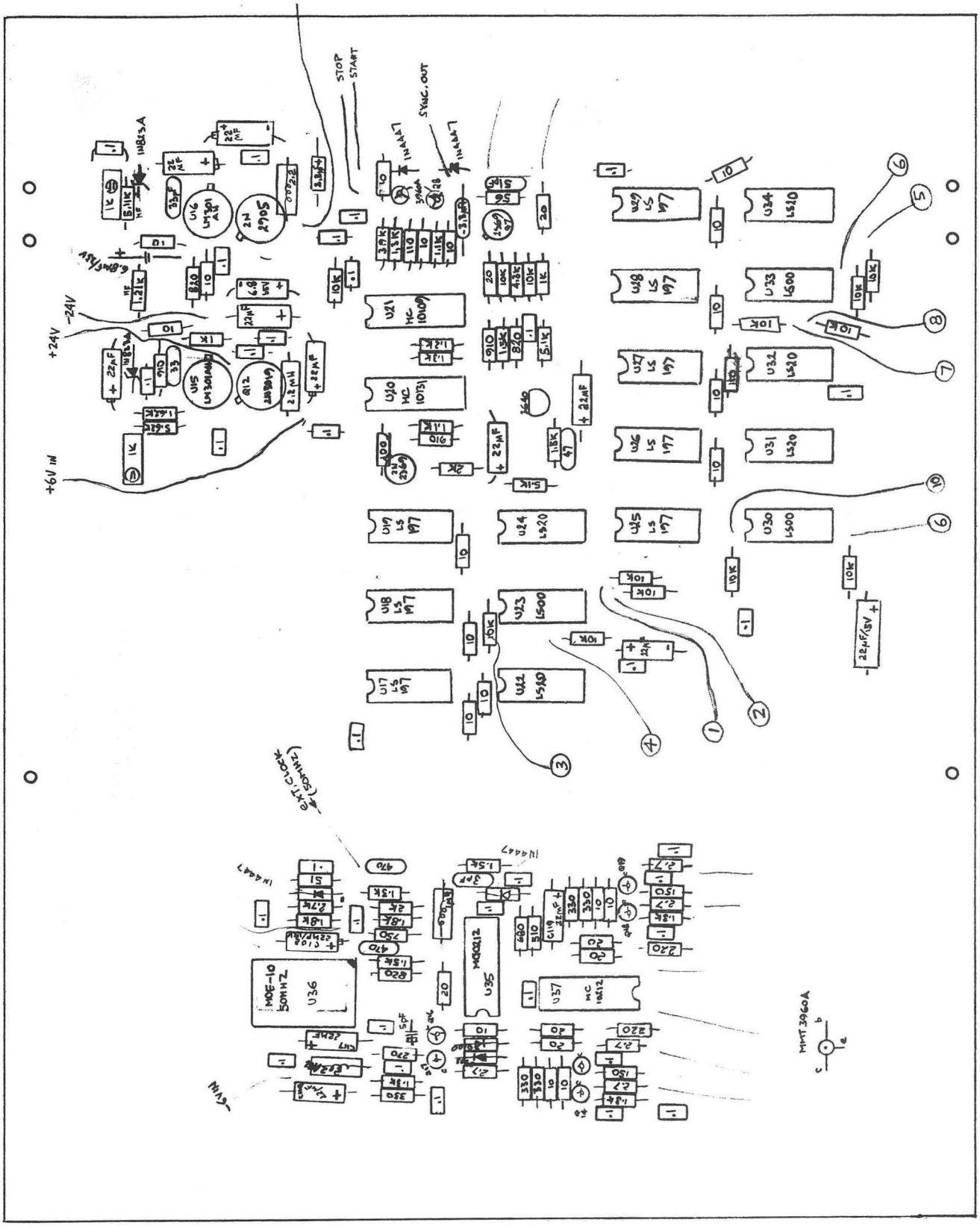


Fig. 4.1.7 Clock and Calibrator module component layout

MS DITEX - CLOCK CALIBRATOR
COMPONENT LAYOUT
10X3051 L-1

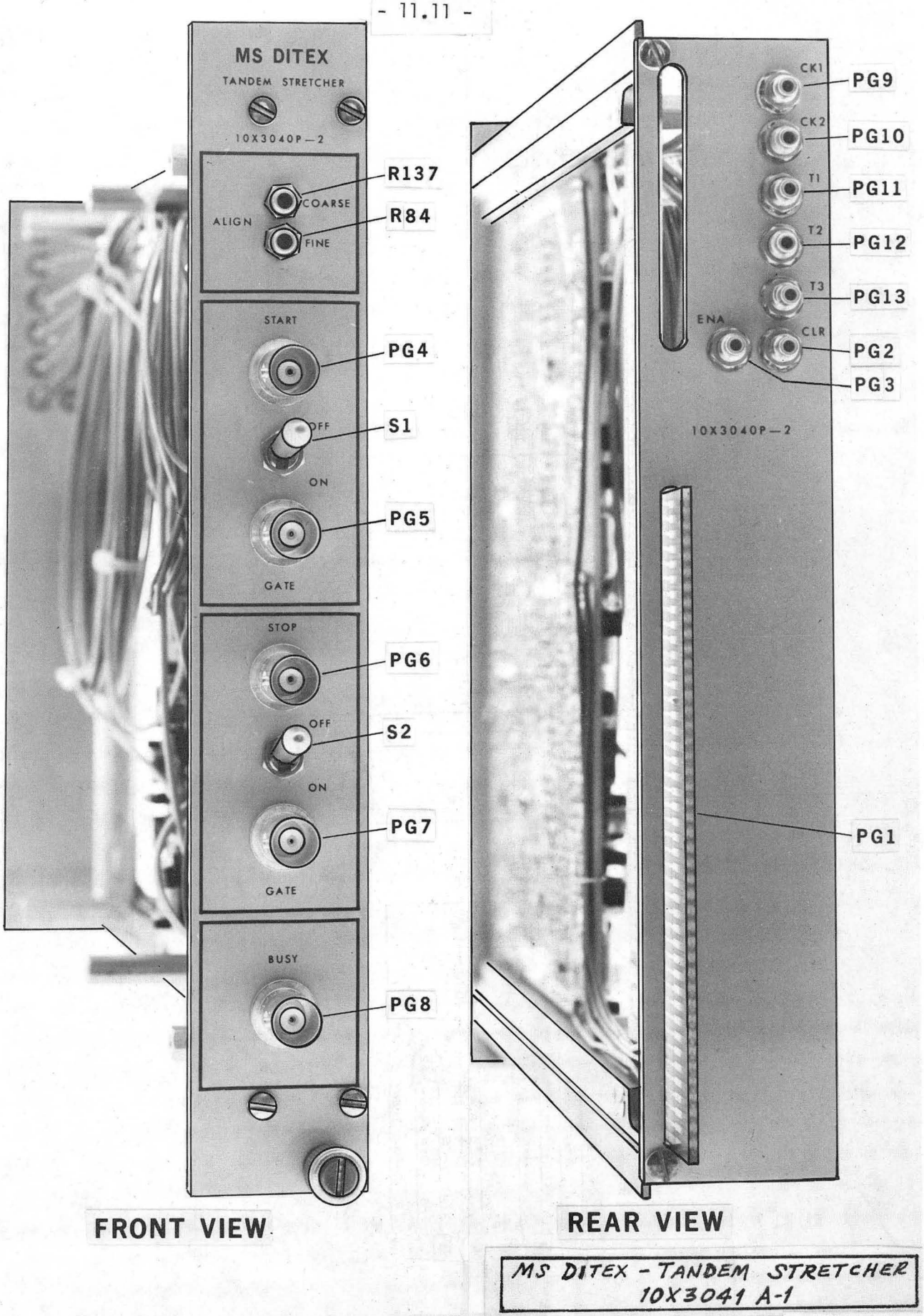


Fig. 4.2.1 Tandem Interpolator module front and rear view

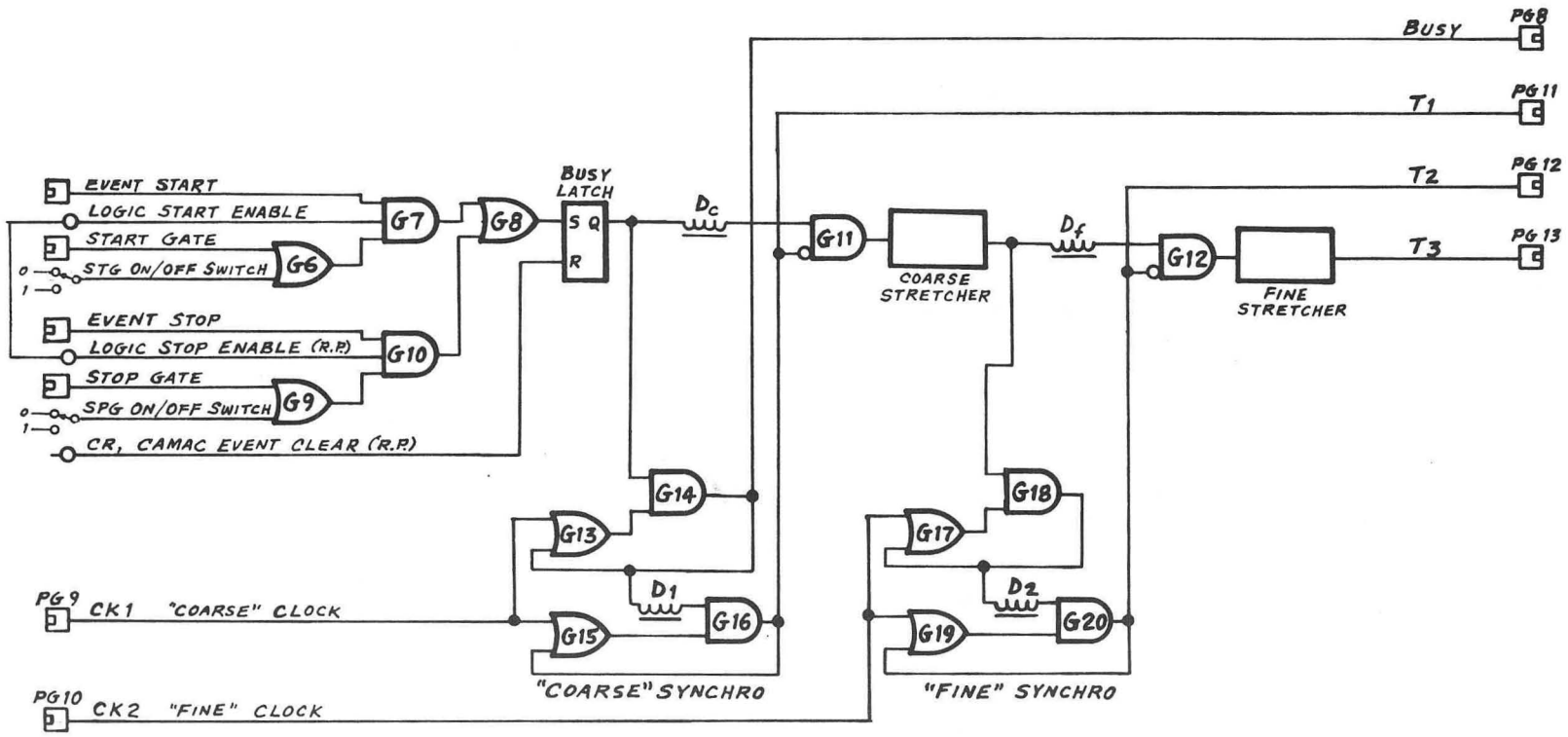
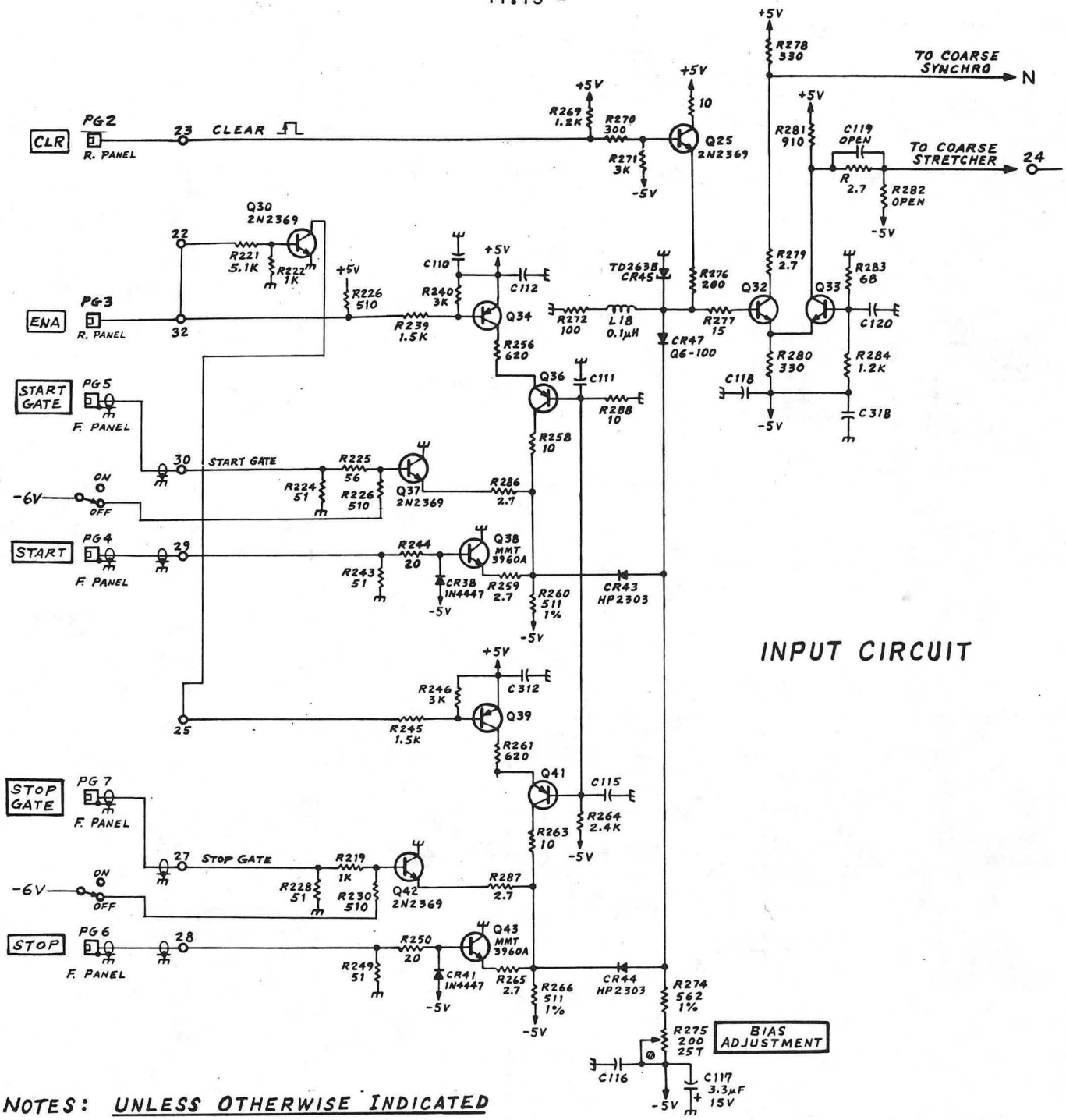


Fig. 4.2.2 Tandem Interpolator block diagram

TANDEM INTERPOLATOR
POWER REGULATORS



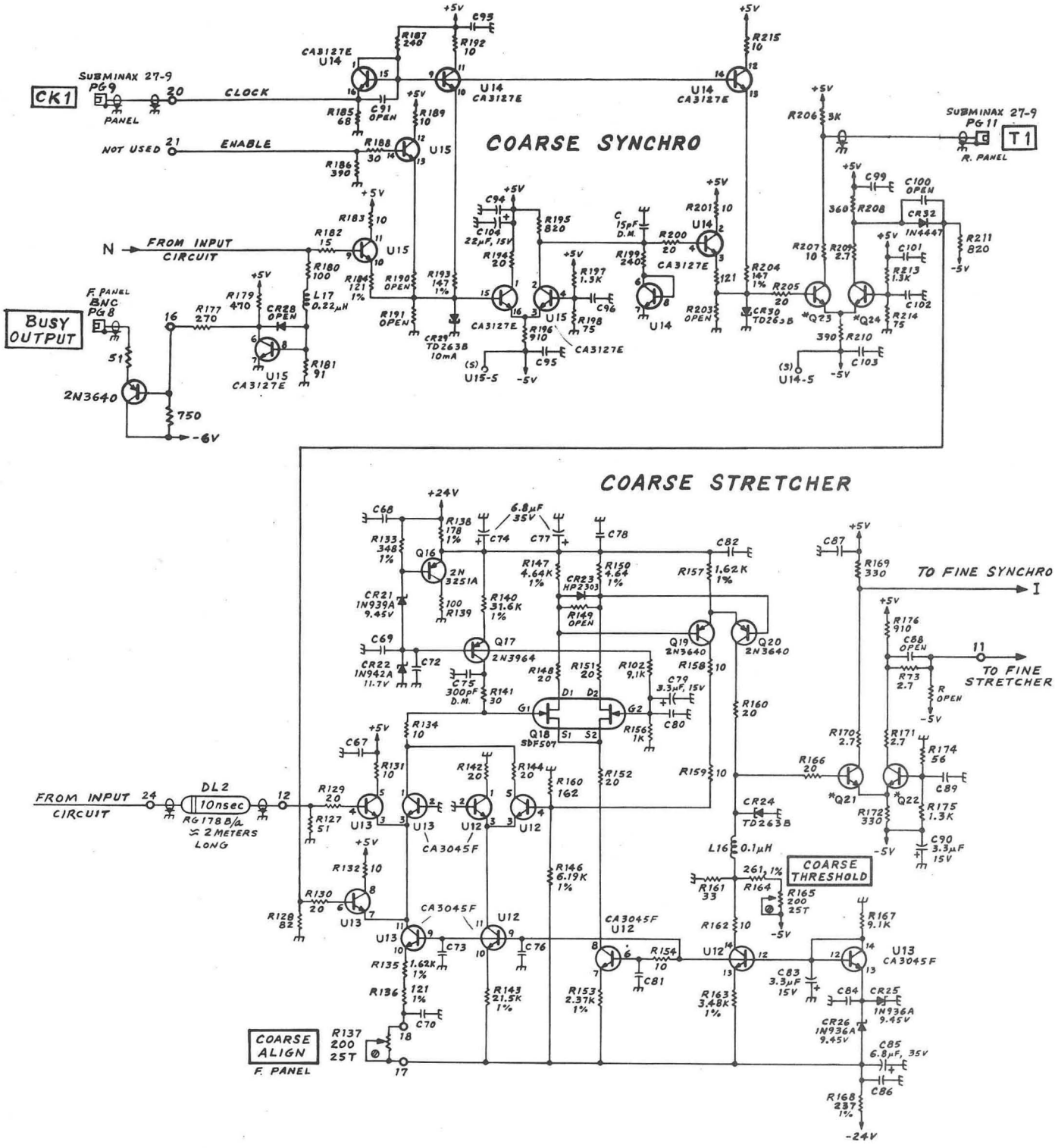
NOTES: UNLESS OTHERWISE INDICATED

1. CAPACITORS 0.1μF 50V CERAMIC CK05BX104K.
2. CONNECTORS BNC.
3. RESISTORS 1/4W 5% CARBON COMPOSITION.
4. TRANSISTORS MMT3960A.
5. NUMBER OUTSIDE o—— ARE TIE POINTS ON PC BOARD
6. BOARD OUTLINE 11X7023M-3E PG1

MS DITEX-TANDEM STRETCHER
10X3041S-1

DWG 1 OF 4

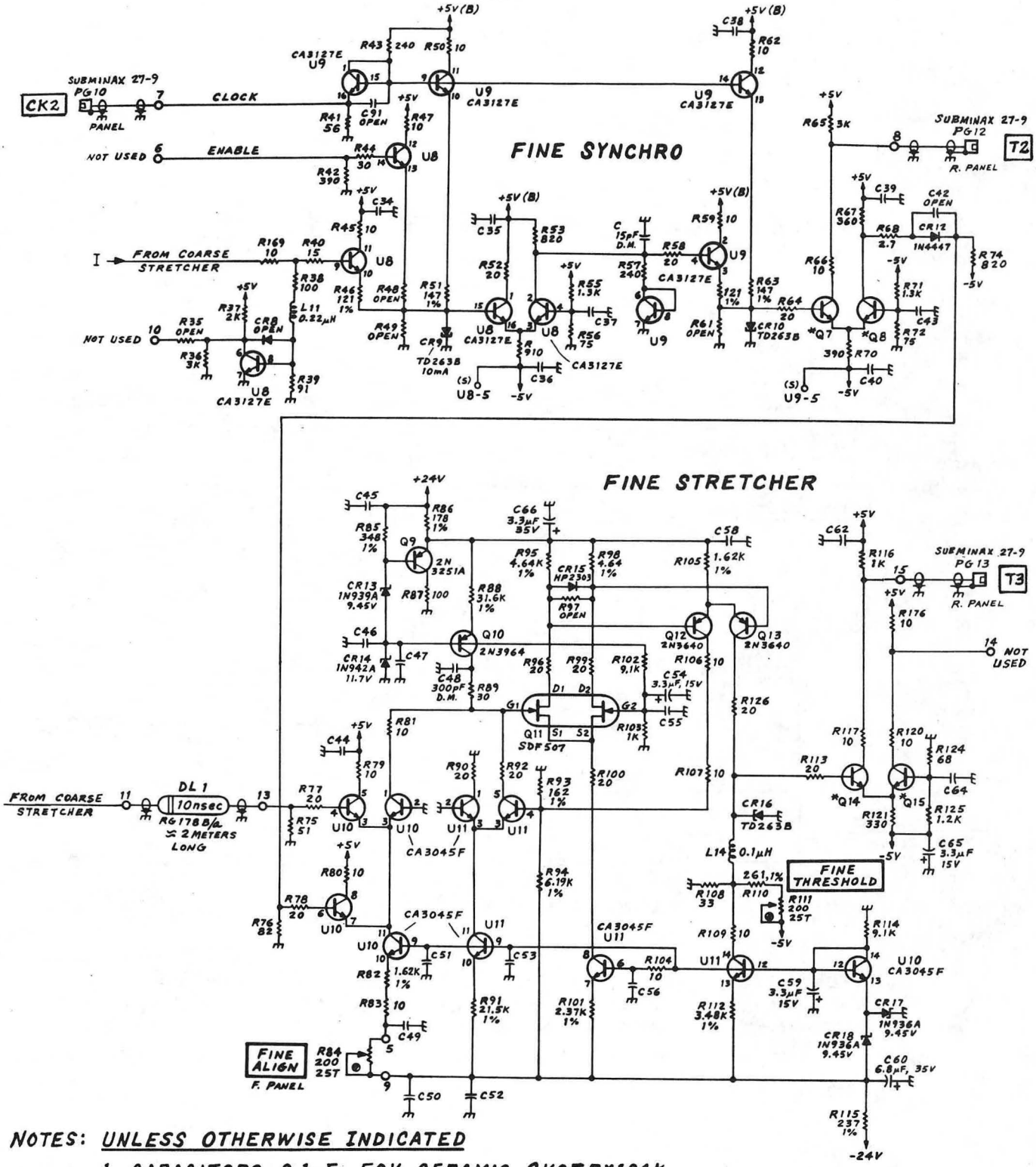
Fig. 4.2.3 Tandem Interpolator input circuit diagram



NOTES: UNLESS OTHERWISE INDICATED

1. CAPACITORS 0.1μF 50V CERAMIC CK05BX104K.
2. RESISTORS 1/4W 5% CARBON COMPOSITION.
3. TRANSISTORS MMT3960A MATCHED PAIRS (Q7, Q8) & (Q14, Q15).
4. NUMBER OUTSIDE o—— ARE TIE POINTS ON PC BOARD

Fig. 4.2.4 Tandem Interpolator coarse stretcher circuit diagram



NOTES: UNLESS OTHERWISE INDICATED

1. CAPACITORS 0.1μF 50V CERAMIC CK05BX104K.
2. RESISTORS 1/4W 5% CARBON COMPOSITION.
*3. TRANSISTORS MMT3960A MATCHED PAIRS (Q7, Q8) & (Q14, Q15).
4. NUMBER OUTSIDE o—— ARE TIE POINTS ON PC BOARD 7U3112.

MS DITEX - TANDEM STRETCHER
10X3041S-3

DWG 3 OF 4

Fig. 4.2.5 Tandem Interpolator fine stretcher circuit diagram

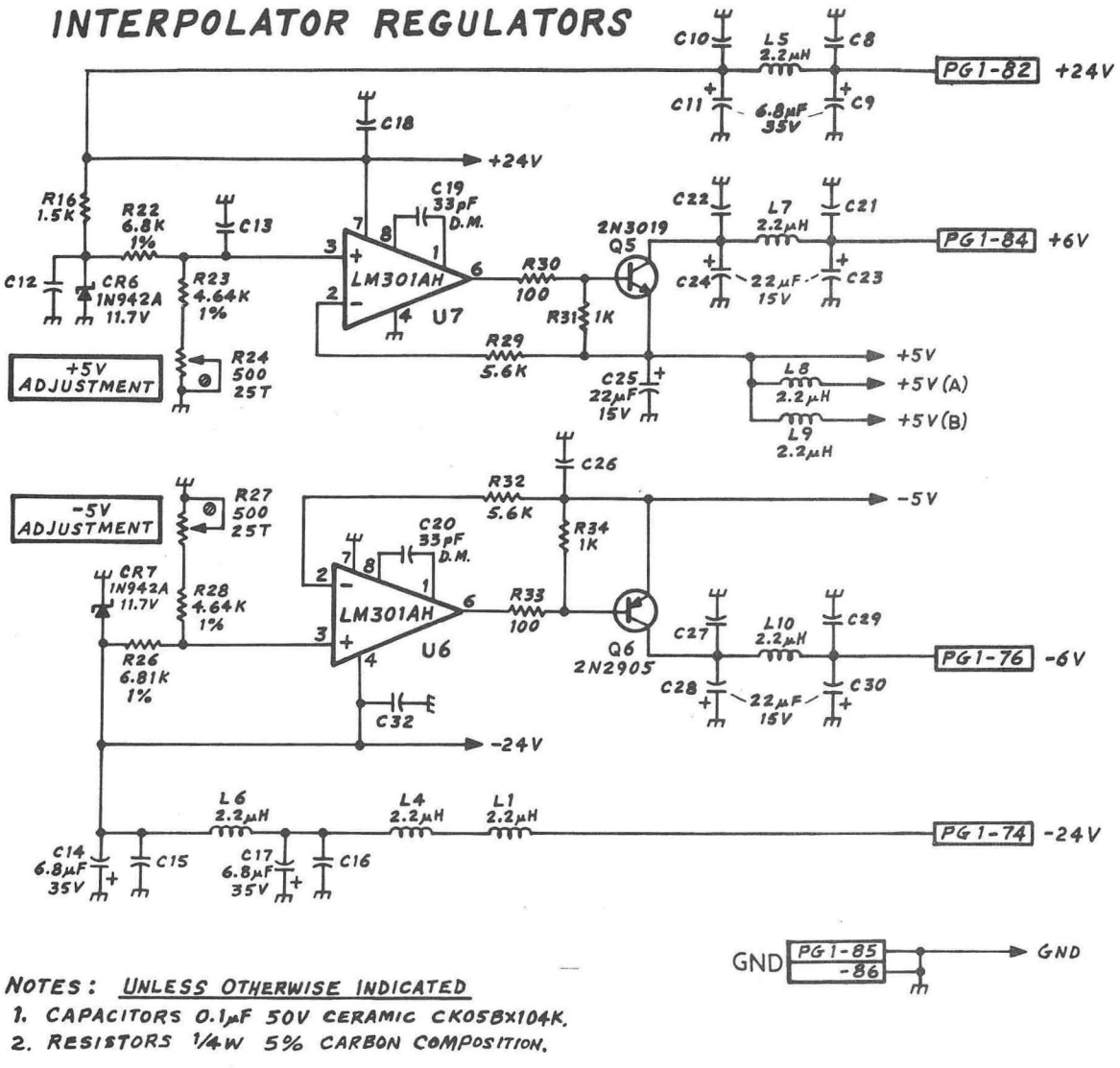


Fig. 4.2.6 Tandem Interpolator power regulator circuit diagram

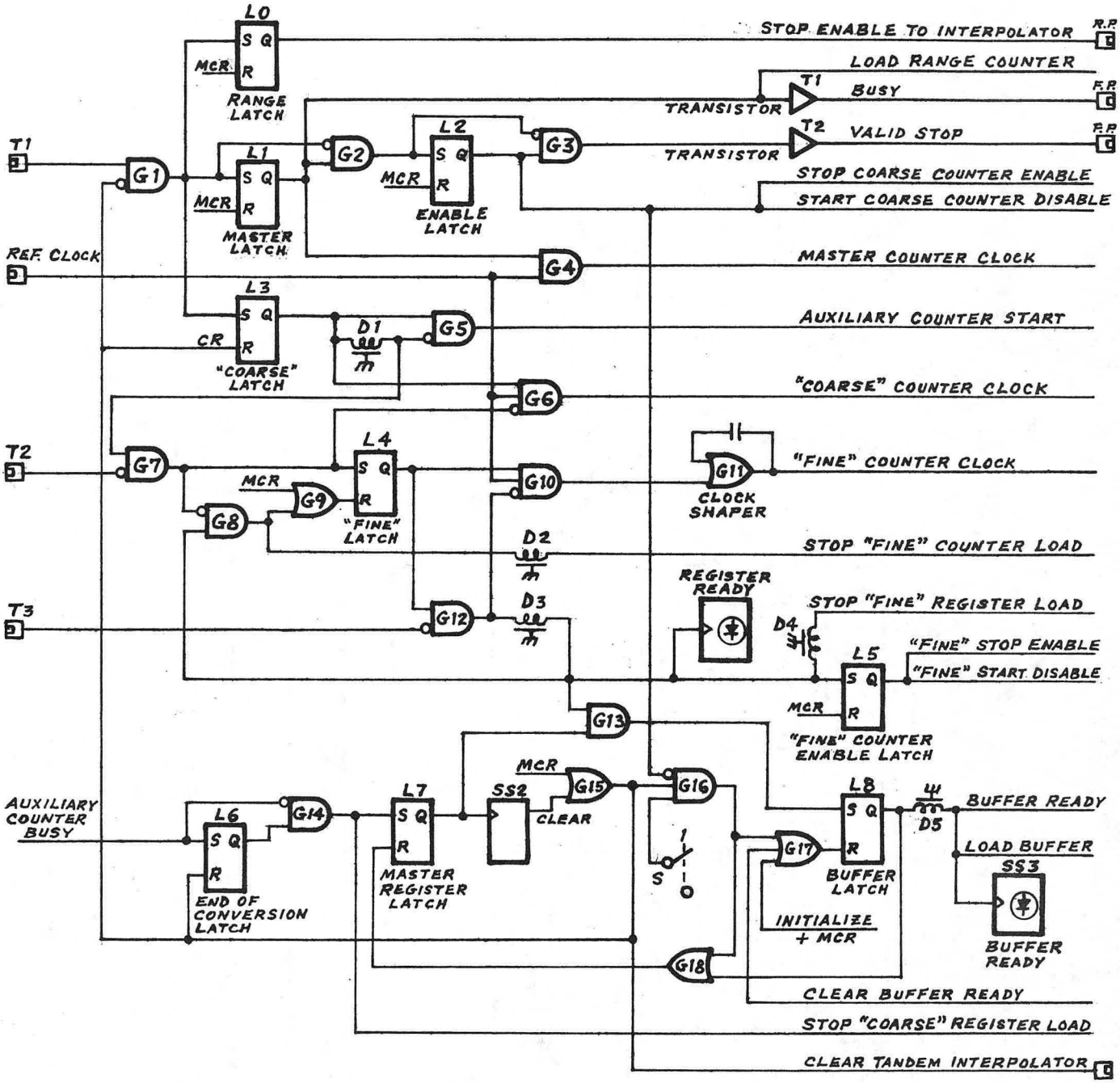


Fig. 4.3.2 Logic module block diagram

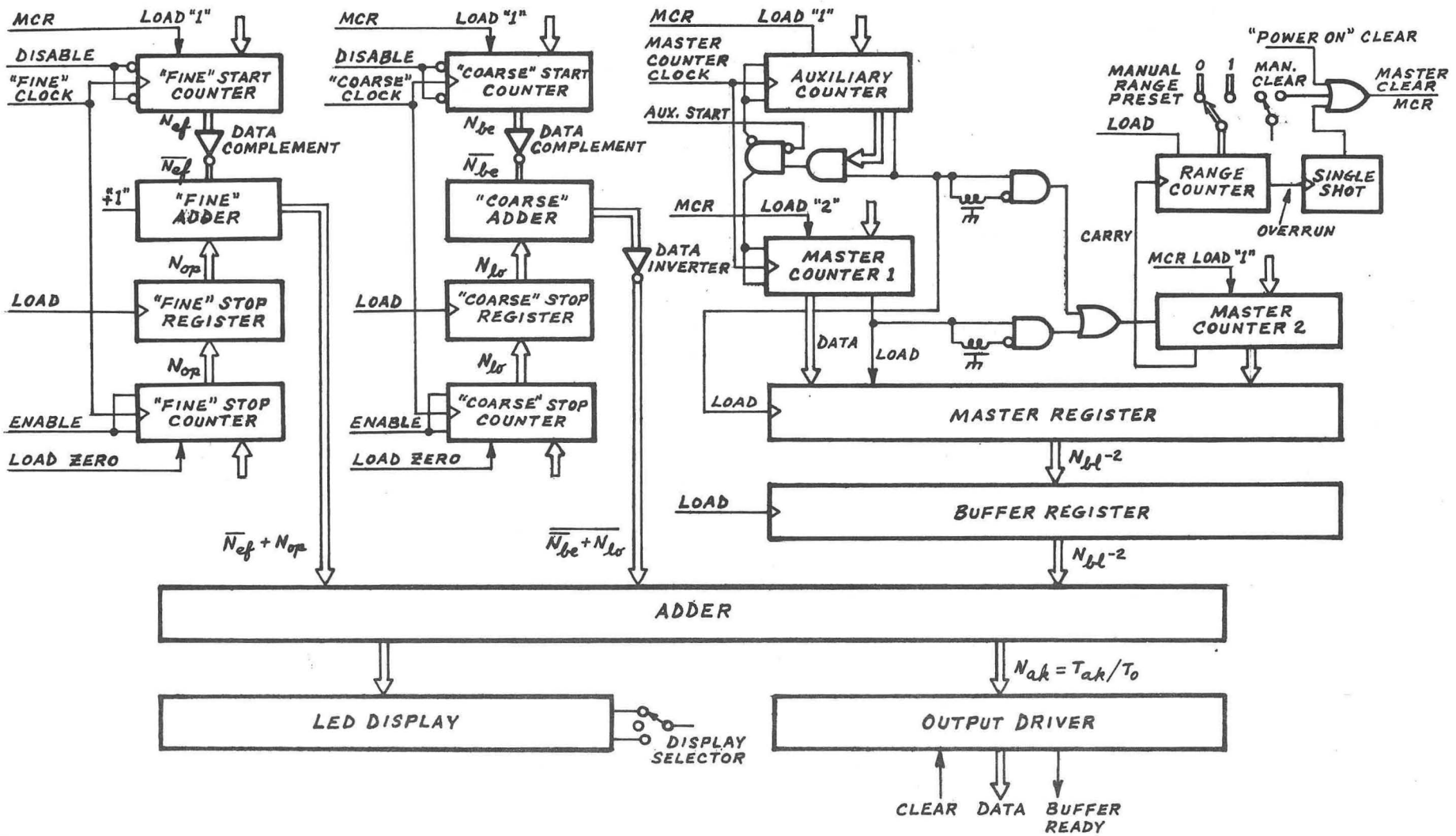
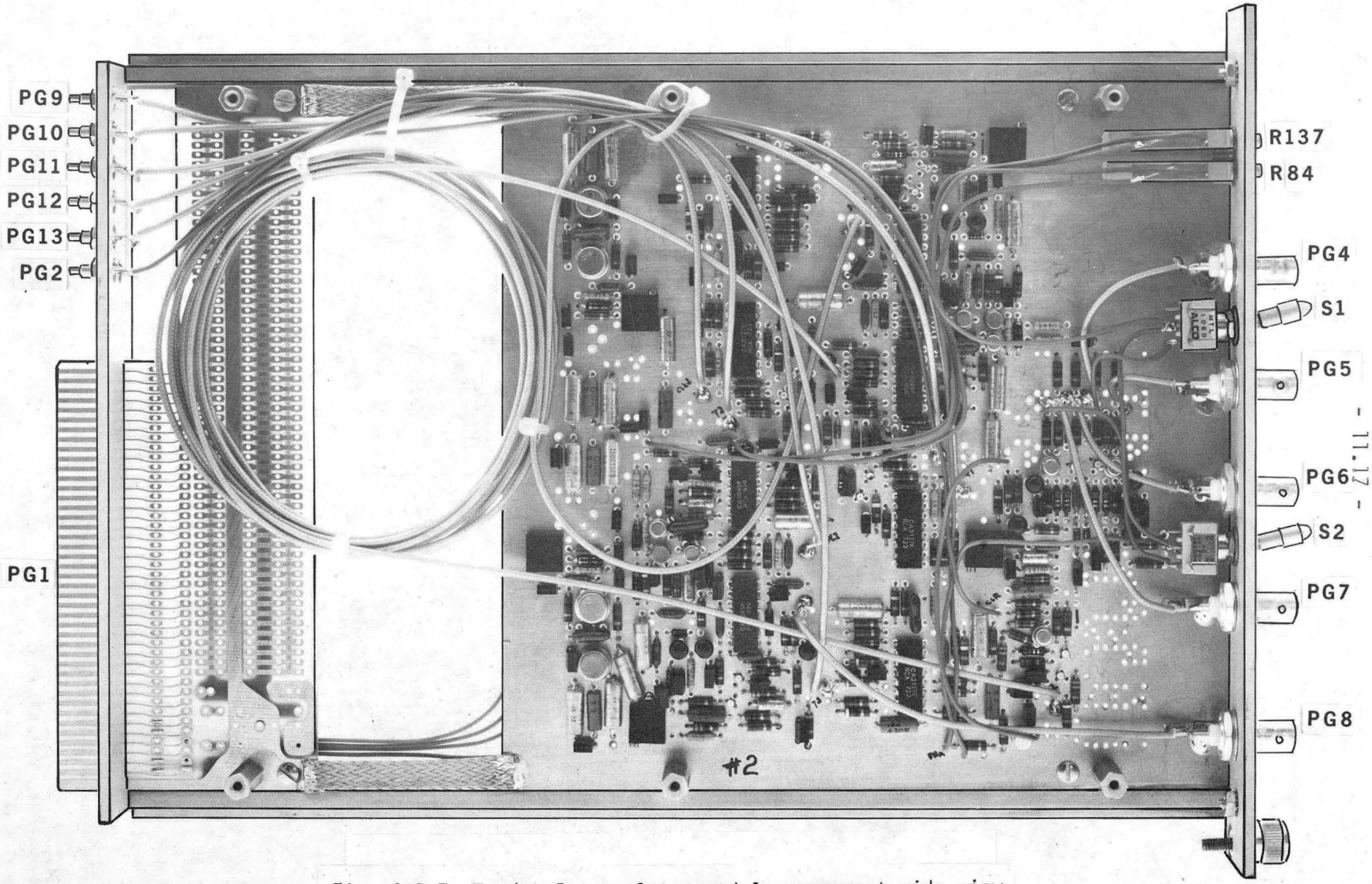


Fig. 4.3.3 Logic module control logic block diagram



MS DITEX - TANDEM STRETCHER
10X 3041 A-2

Fig. 4.2.7 Tandem Interpolator module component side view

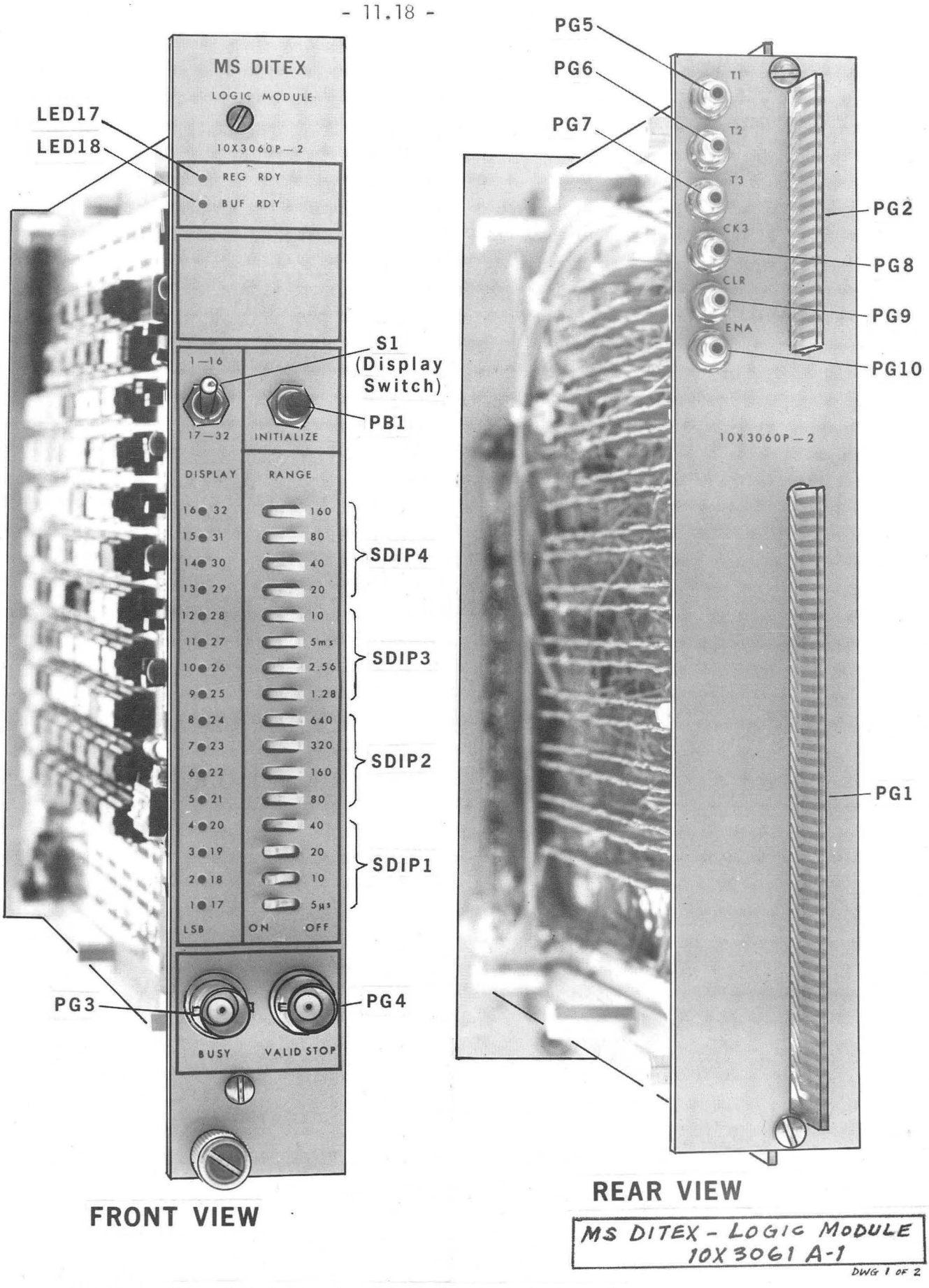


Fig. 4.3.1 Logic module front and rear view

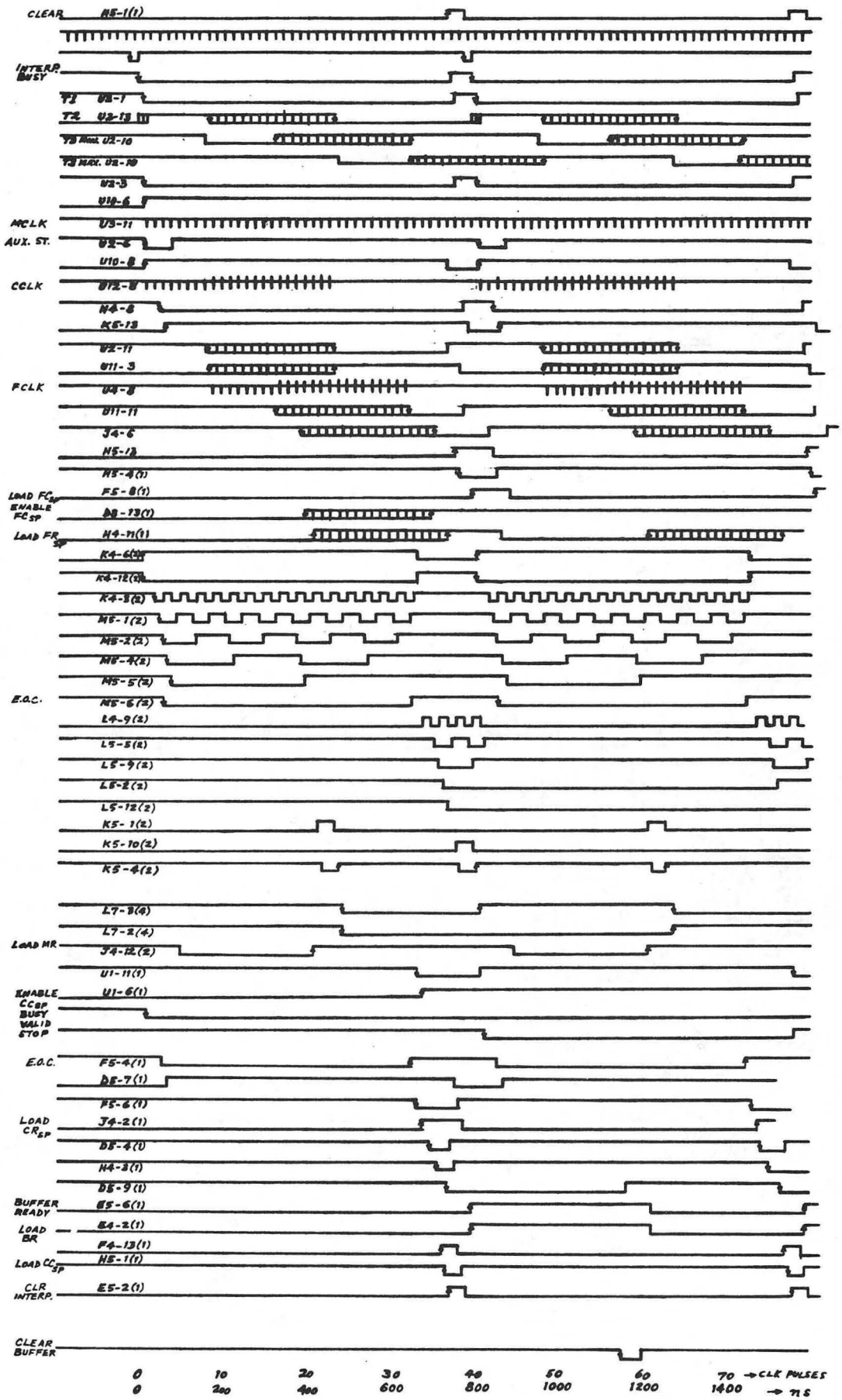


Fig. 4.3.4 Logic module timing diagram

MS DITEX TIMING DIAGRAM
10X3031 T-1

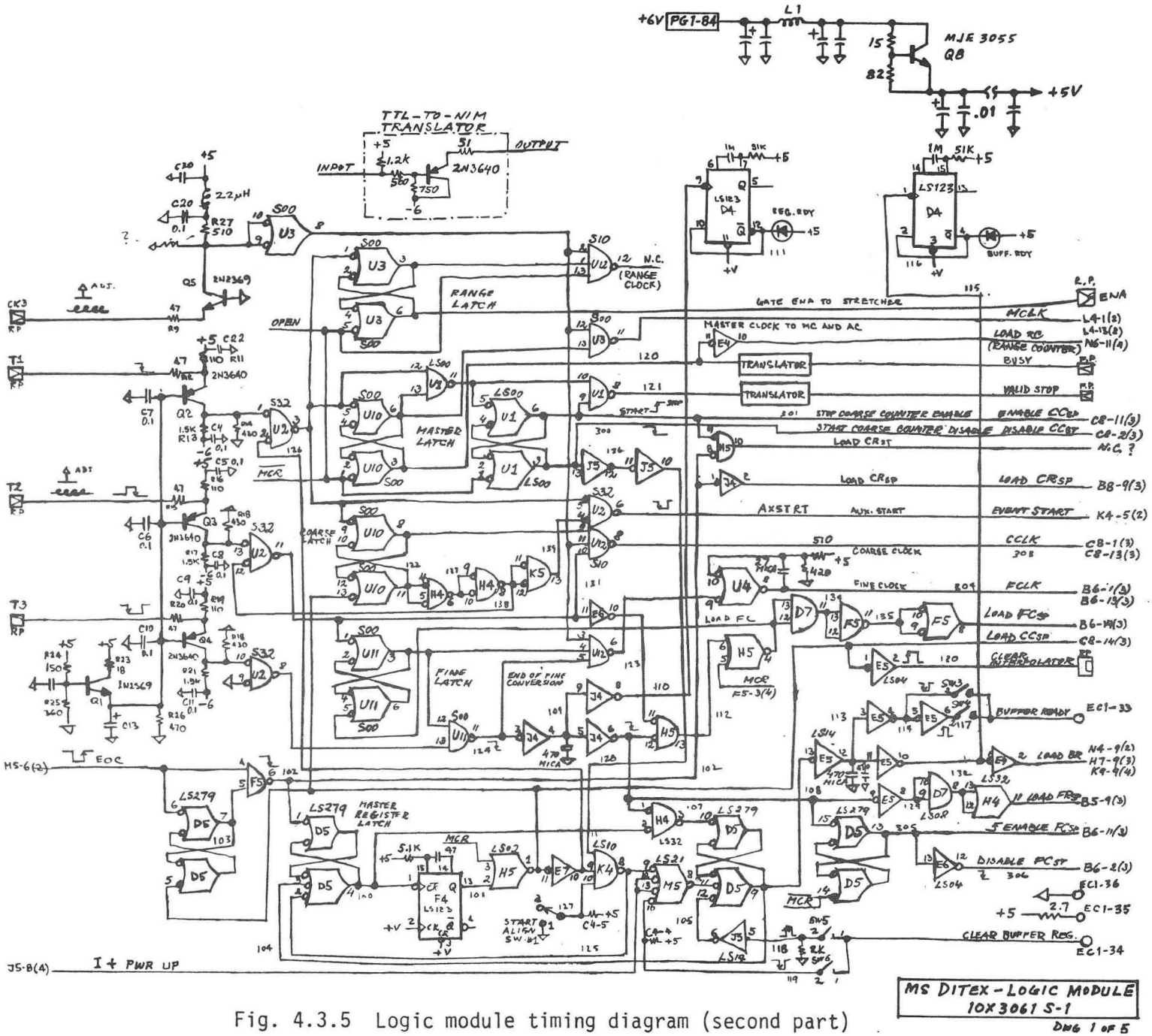


Fig. 4.3.5 Logic module timing diagram (second part)

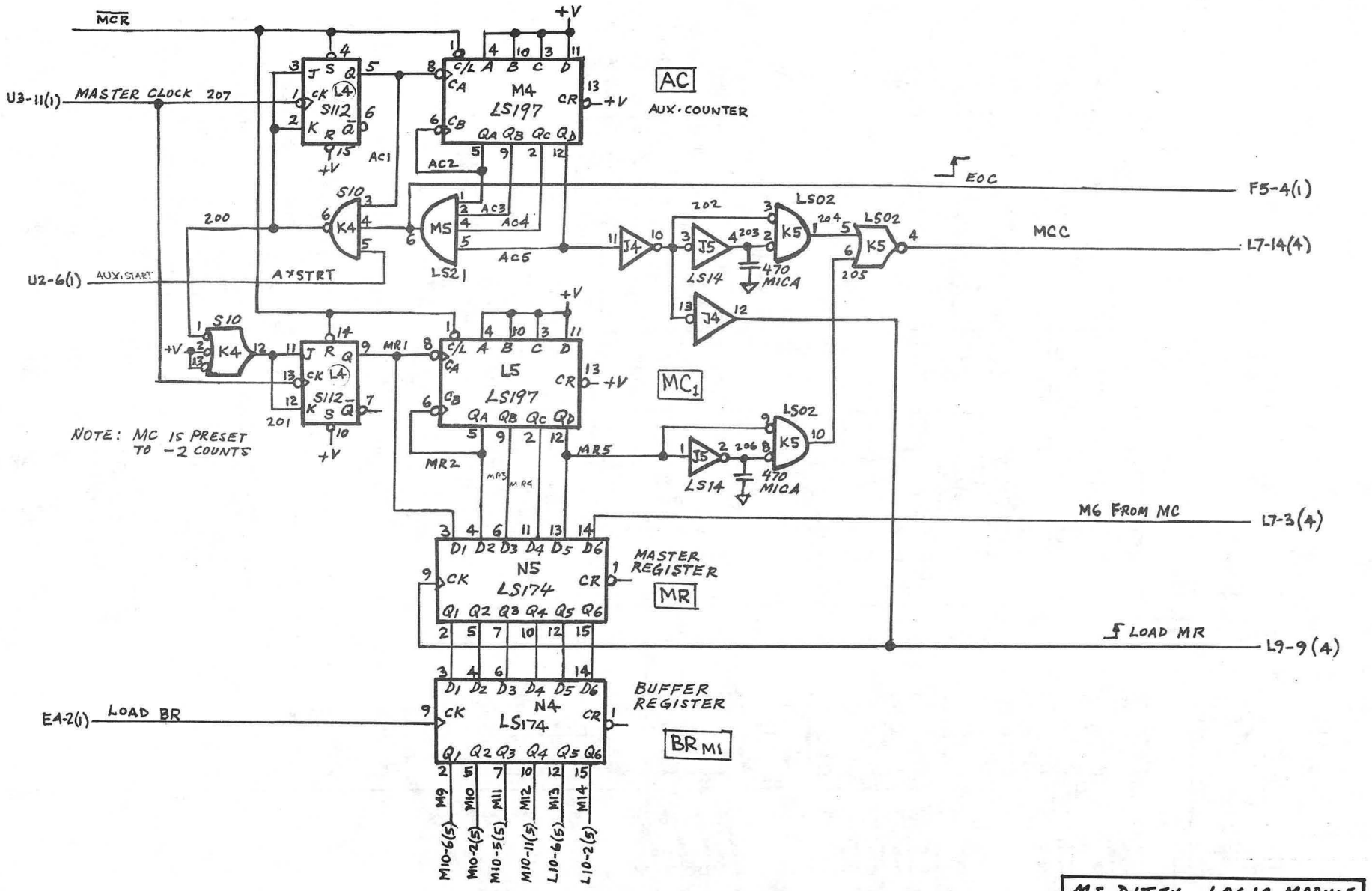


Fig. 4.3.6 Logic module input circuit diagram

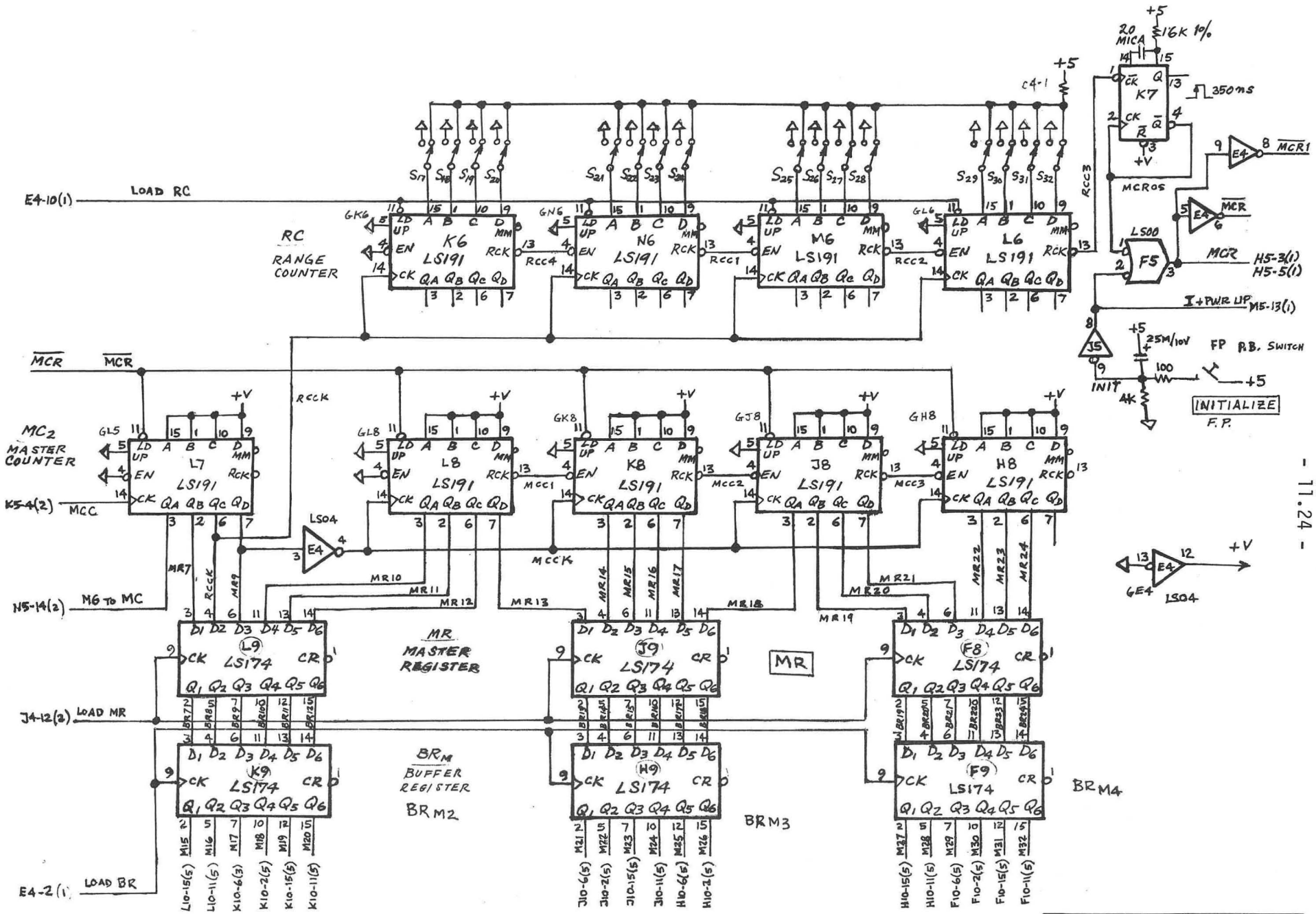


Fig. 4.3.7 Logic module auxiliary counter and master counter (first part)

MS DITEX-LOGIC MODULE
10X3061S-4
DWG 4 OF 5

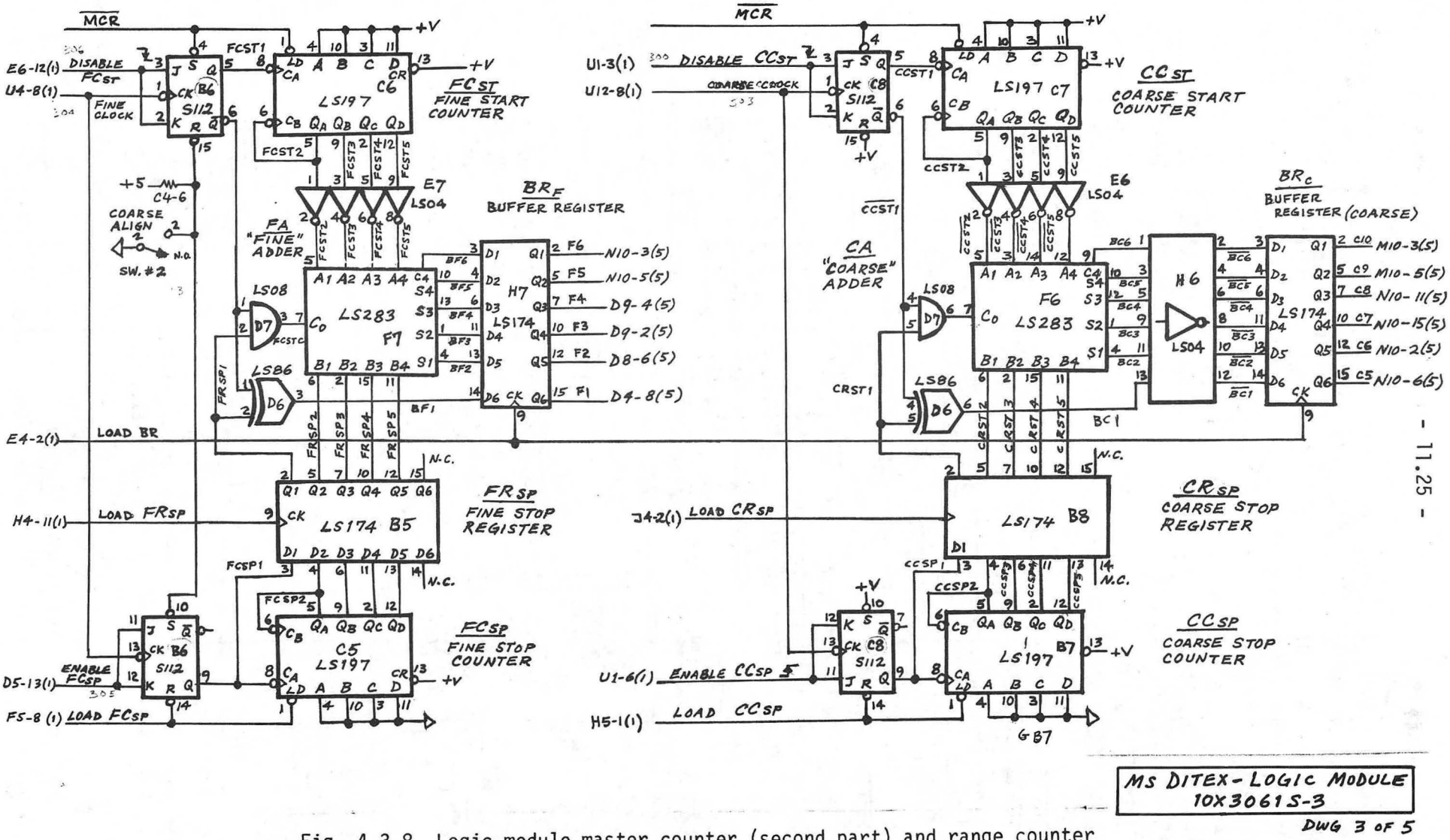


Fig. 4.3.8 Logic module master counter (second part) and range counter

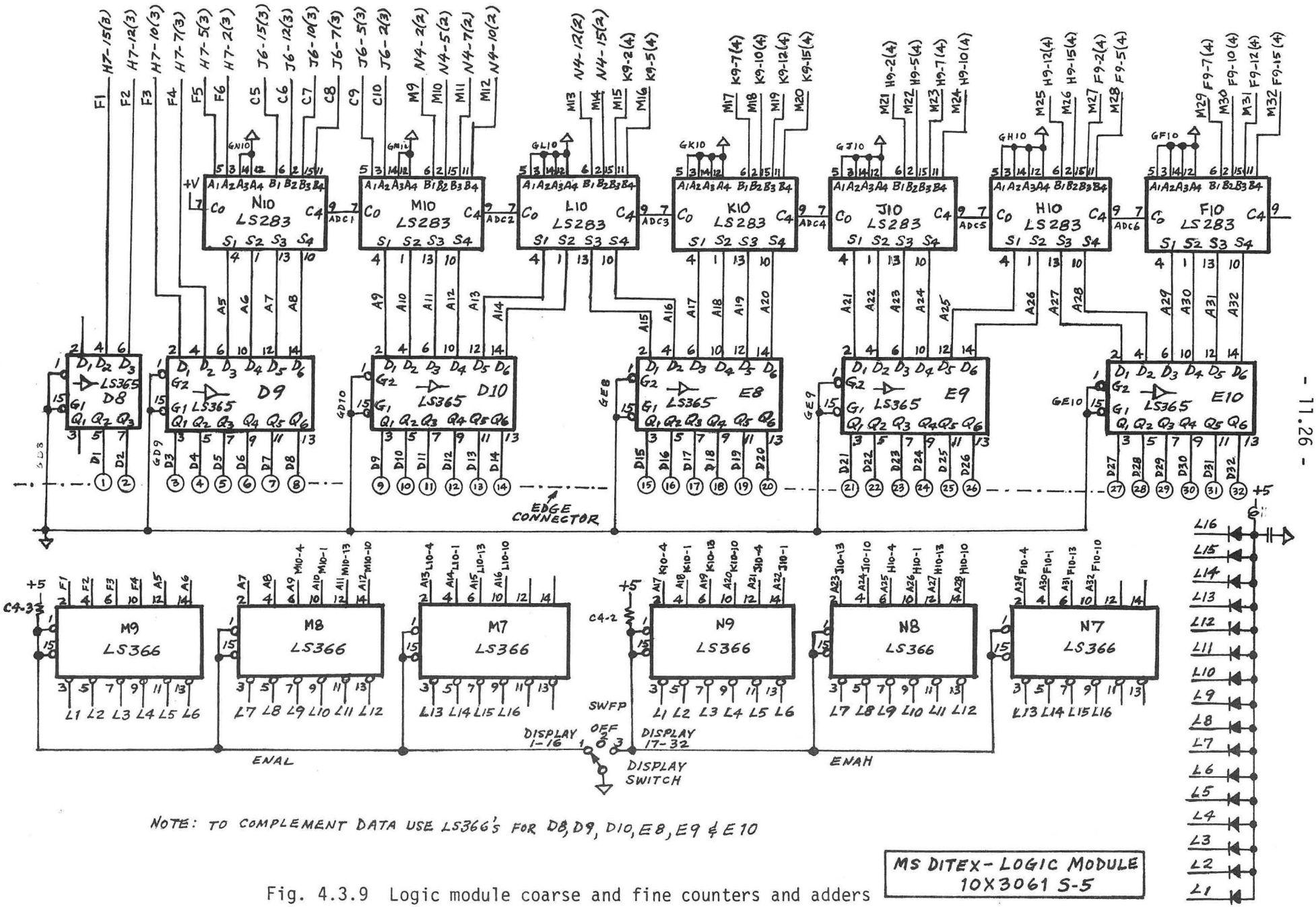
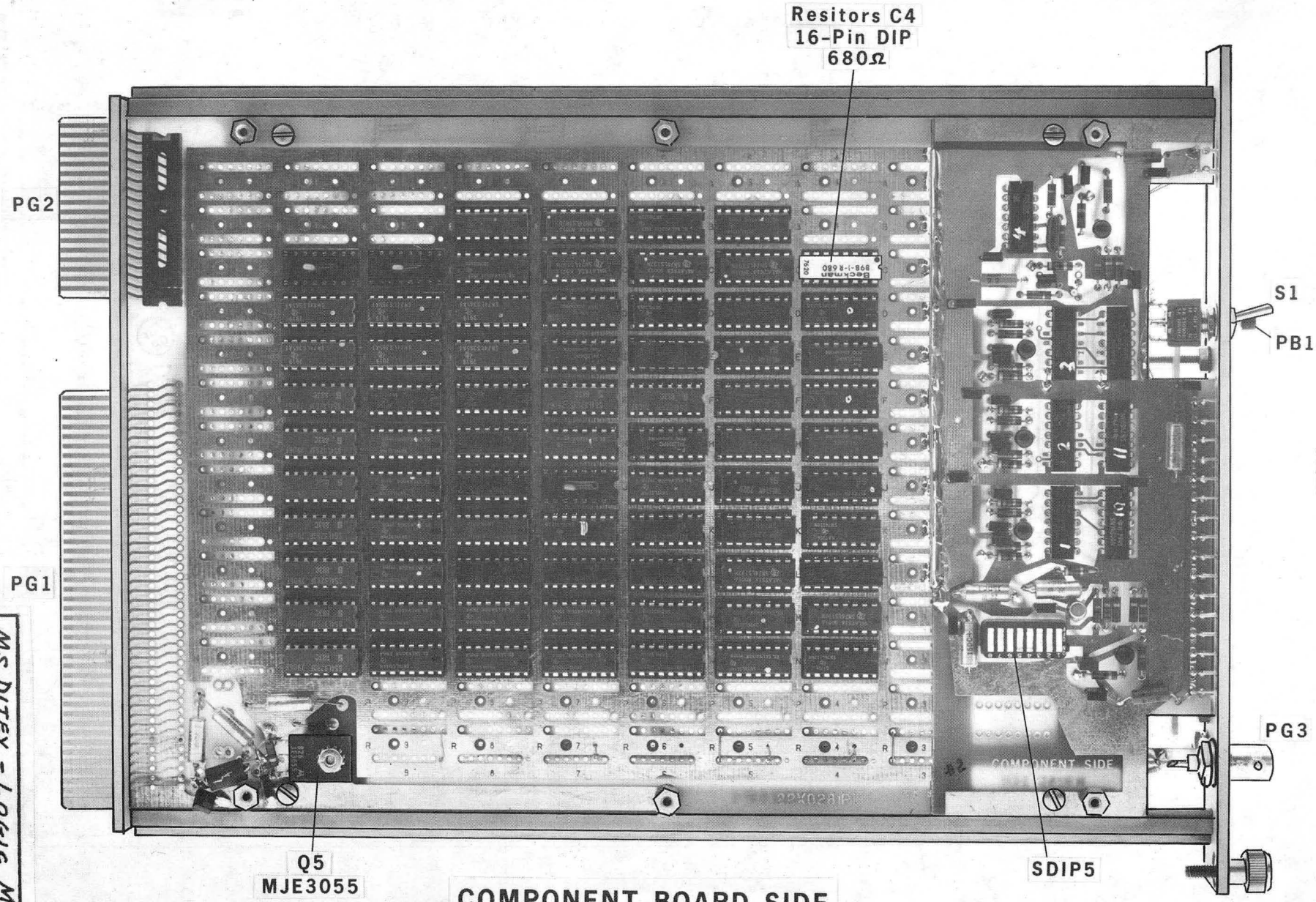


Fig. 4.3.9 Logic module coarse and fine counters and adders



COMPONENT BOARD SIDE

Fig. 4.3.11 Logic module component side view

MS DITEX - LOGIC MODULE
10X3061A-2
DWG 2 of 2

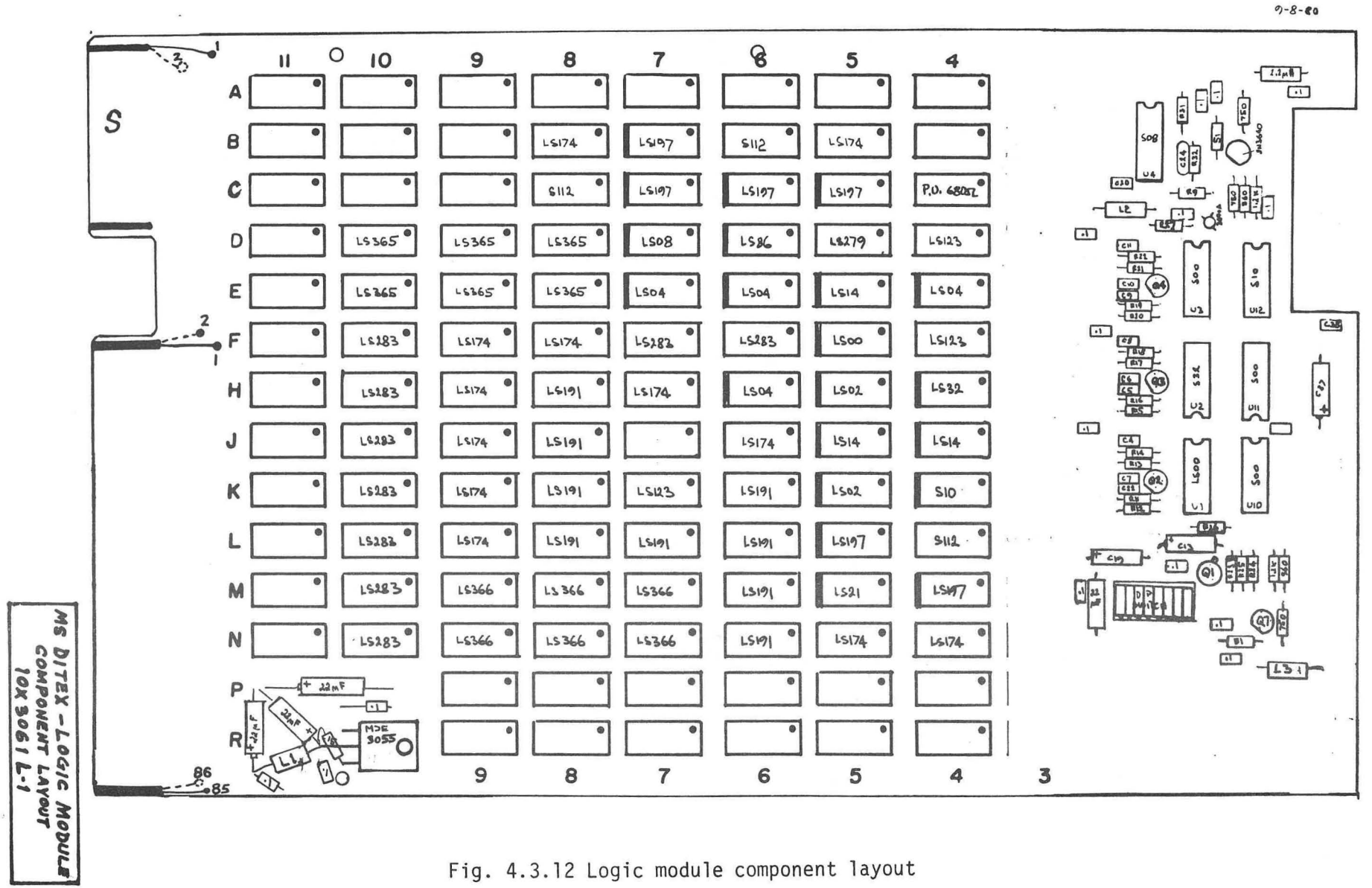


Fig. 4.3.12 Logic module component layout

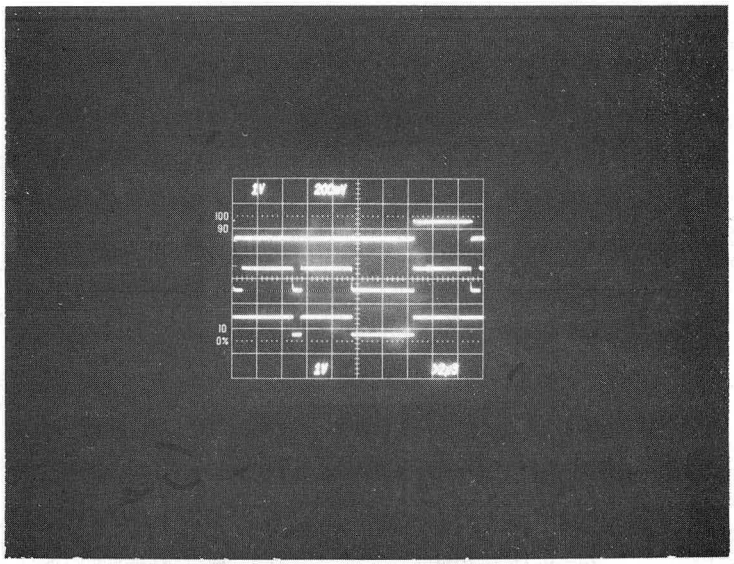


Fig. 5.1 Digitizer processing a start and two stop events in a typical sequence, as seen on an oscilloscope monitoring start BUSY, event BUSY and VALID STOP outputs

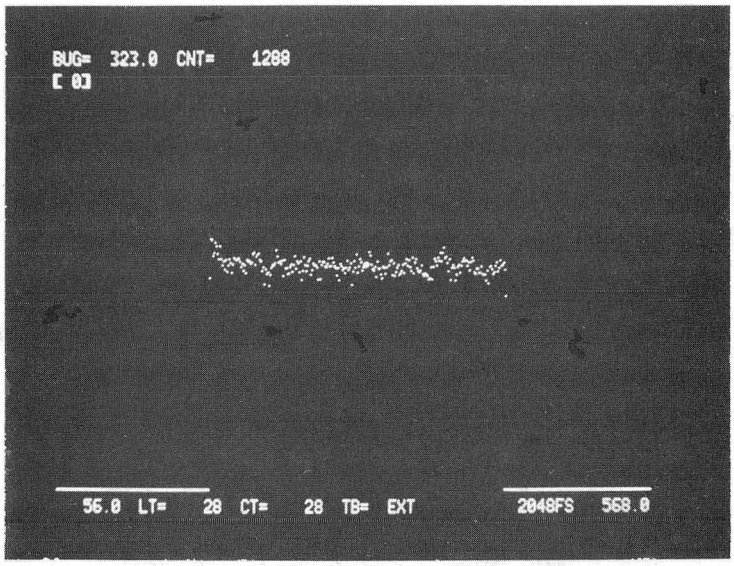


Fig. 5.2 Typical phase distribution histogram of start events Start events are at random with respect to the digitizer's reference clock. The photograph shows proper alignment of the interpolator, containing 255 evenly distributed channels. Calibration of a channel: 78.125 ps.

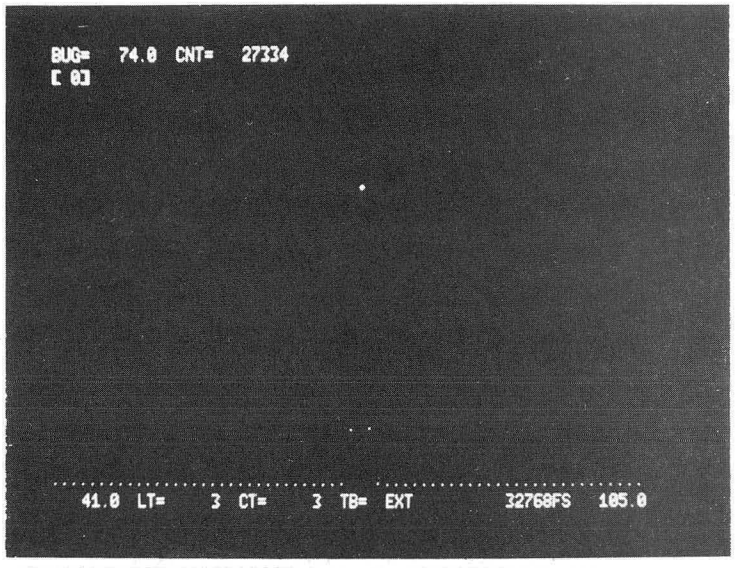


Fig. 5.3 Measurement of 40.960 μs time intervals. The counts in two adjacent channels indicate total jitter of less than 15 picosecond.

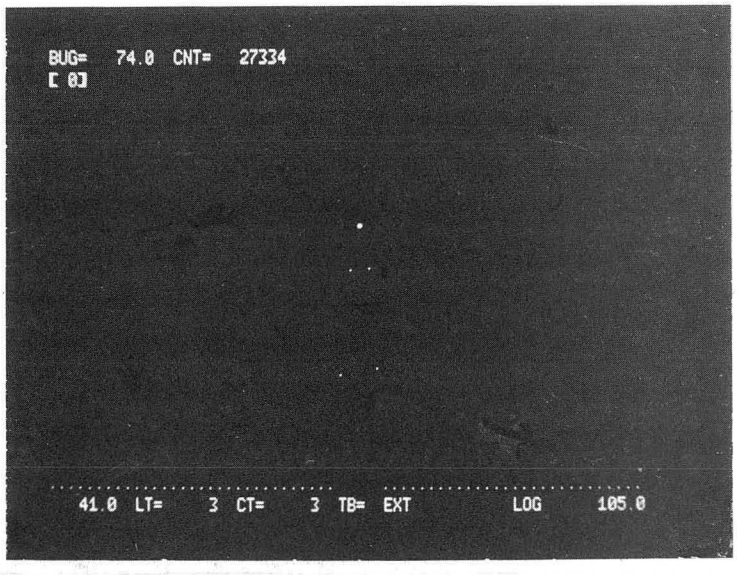


Fig. 5.4 Logarithmic display of the peak of Fig. 5.3 shows negligible spread of step counts into adjacent channels

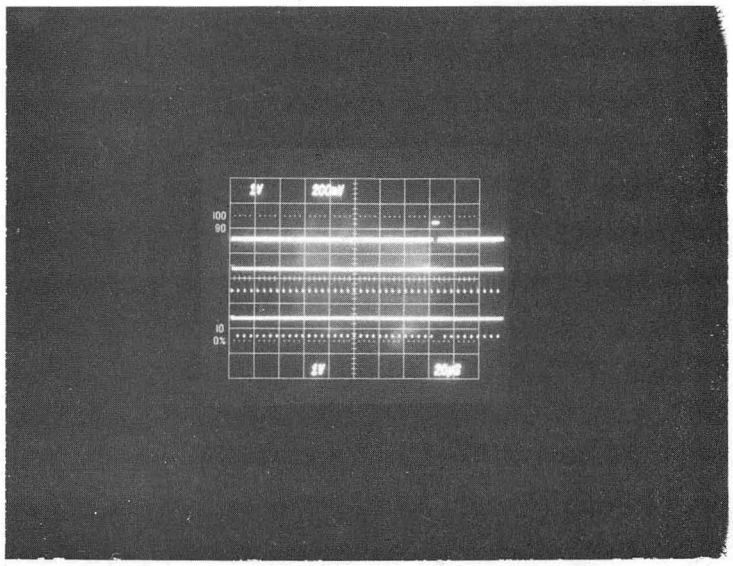


Fig. 5.5
Measurement of 31-stop event bursts during a 160 µs time range. From top: Start busy (time range), Event busy and Valid stop oscillograms.

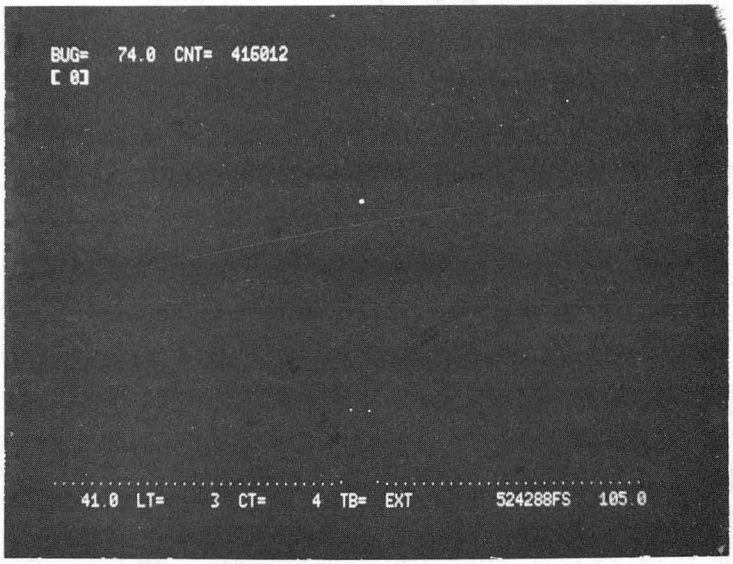


Fig. 5.6
Distribution of 31 overlapped stop events from Fig. 5.5 indicate only a slight increase of measured time jitter (compared to Fig. 5.3).

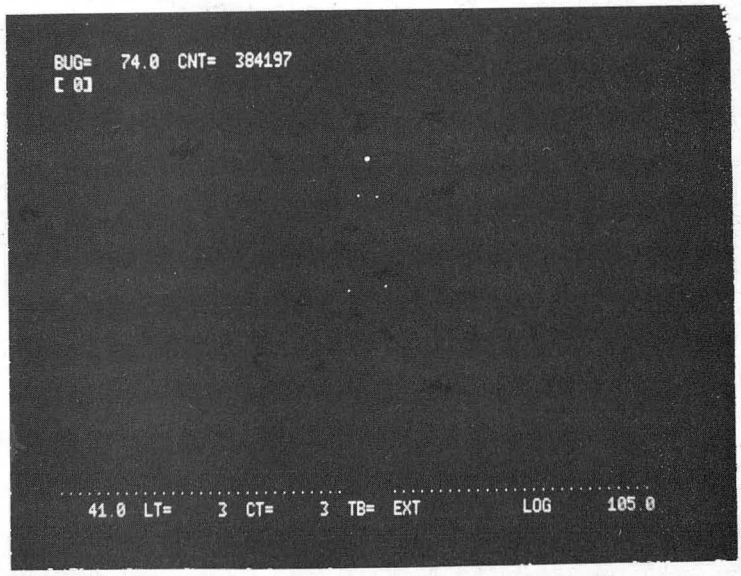


Fig. 5.7
Logarithmic display of stop events from Fig. 5.5. No increase in the width is noticed, although 31 stop events are merged into a single peak.

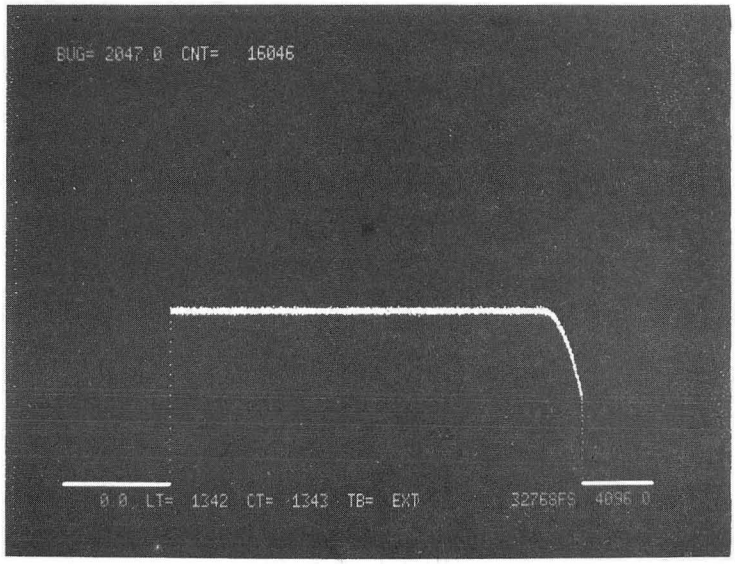


Fig. 5.8 Random distribution of start and stop events in 5 μs time range. Resolution is 1.25 ns/channel. Initial gap is due to the start event dead time.

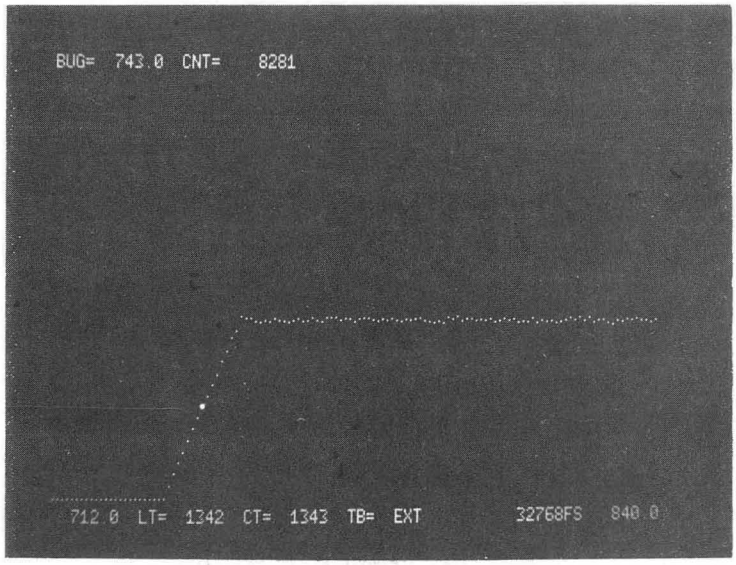


Fig. 5.9 Expanded portion of random start and stop event distribution of Fig. 5.8. Recovery from deadtime is linear, indicating that start events were at random with respect to the digitizer's internal reference clock.

This report was done with support from the Department of Energy. Any conclusions or opinions expressed in this report represent solely those of the author(s) and not necessarily those of The Regents of the University of California, the Lawrence Berkeley Laboratory or the Department of Energy.

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