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ASSESSMENT OF PRESENT AND FUTURE LARGE-SCALE SEMICONDUCTOR DETECTOR SYSTEMS

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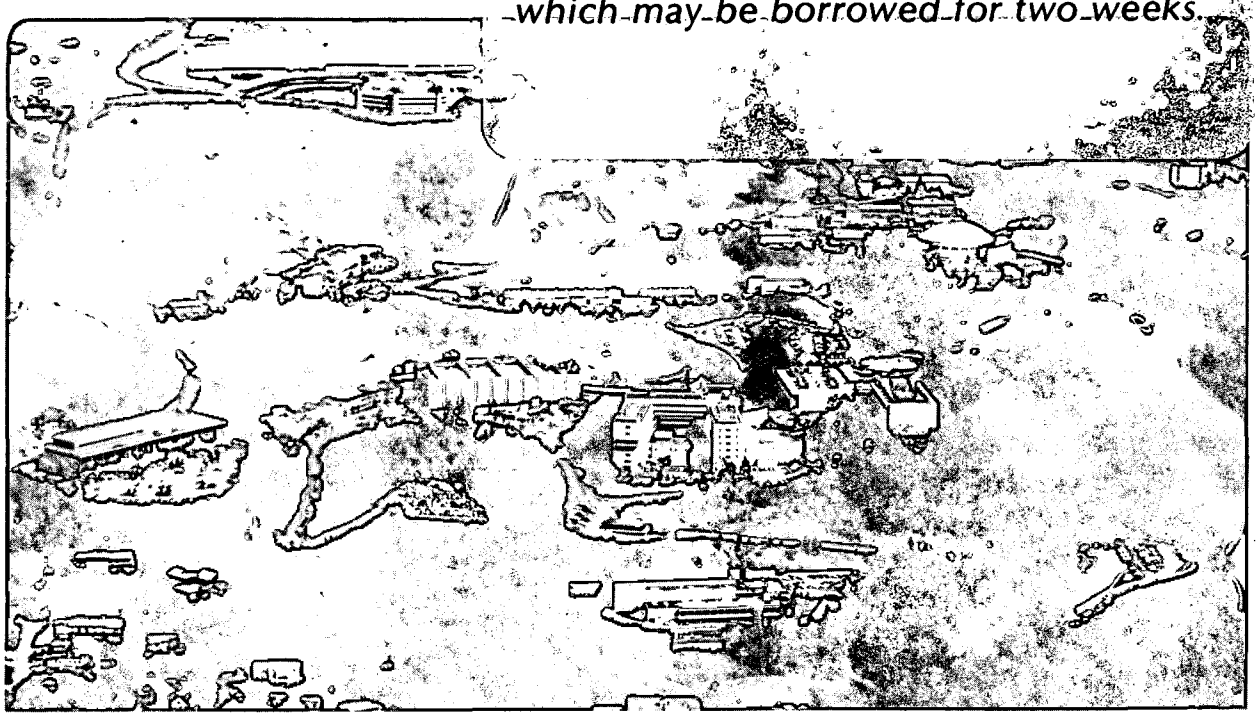

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Abstract

The performance of large-scale semiconductor detector systems is assessed with respect to their theoretical potential and to the practical limitations imposed by processing techniques, readout electronics and radiation damage. In addition to devices which detect reaction products directly, the analysis includes photodetectors for scintillator arrays. Beyond present technology we also examine currently evolving structures and techniques which show potential for producing practical devices in the foreseeable future.

Introduction

The next generation of high-energy particle accelerators will pose great challenges in detector design. Especially the Superconducting Super Collider (SSC), now in its initial design phase, will require significant departures from conventional detector design to provide the event rate capability and granularity needed to exploit the unprecedented capabilities of this new machine.

The use of semiconductor detectors has been proposed as a solution to some of these problems. Collection times in these devices can be in the range of nanoseconds and position resolution of several microns seems to be possible. Furthermore, VLSI technology offers the feasibility of integrating thousands of detector elements on a chip together with their associated readout electronics. These prospects have prompted a considerable amount of attention to semiconductor detectors in the high-energy physics community, especially in the areas of CCD's and strip detectors for high resolution vertex determination [1-9]. Nevertheless, many questions remain to be answered and a multitude of problems needs to be solved before we can state that large-scale semiconductor detectors are not just a promising possibility, but in fact practical devices that can be designed and operated in a high-energy physics environment.

Detector Basics

Figure 1 shows the cross section of a typical multielement detector. The electrode segments at the bottom of the structure represent either strips or individual pixels. As a charged particle traverses the detector a sheath of electrons and holes will form around its track. The diameter of this sheath is determined by the energy distribution of the delta electrons formed in the energy loss process and is not known with any reasonable accuracy. However, for minimum ionizing particles it is probably less than one micron. The number of electron-hole pairs formed along the track of a minimum ionizing particle is about 80 per micron [10]. As electrons and holes drift towards the positive and negative electrode, respectively, they diffuse outwards, thus increasing the diameter of the charge sheath by

$$\sigma_x = \sqrt{2\,D\,t} \qquad (1)$$

where D is the diffusion coefficient for electrons or holes and t is the respective drift time.

If the applied bias voltage is insufficient to fully deplete the detector of mobile charge, the resulting

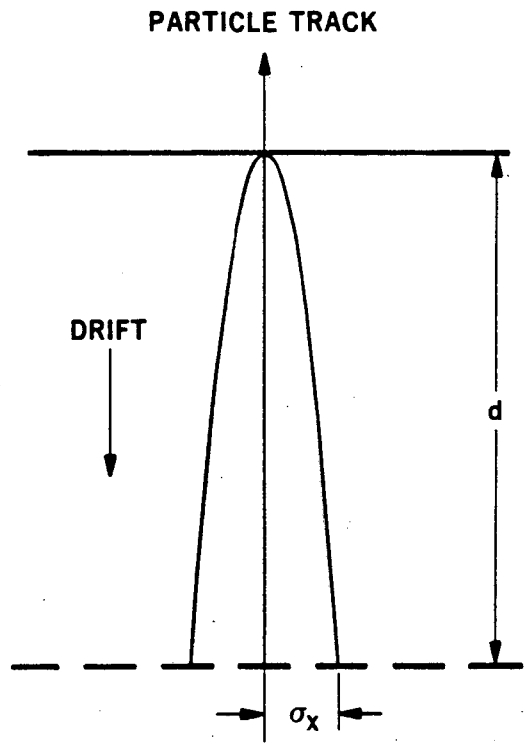

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Fig. 1. Transverse diffusion of charge carriers in the detector during collection. The transverse spread is shown for just one type of carrier. The envelope for the complementary charges opens towards the top.

field is as shown in Fig. 2a. The field vanishes at the depletion edge farthest from the junction, leading to long collection times. Furthermore, charge will tend to bunch up in this region, leading to increased transverse diffusion. This situation can be avoided by applying bias in excess of the depletion voltage as shown in Fig. 2b. The collection times can now be estimated by assuming an average uniform field throughout the detector. For silicon detectors we obtain

$$t_{cn} = 74\,\frac{d}{E} \quad [\mathrm{ns}] \qquad (2)$$

for electrons, and

$$t_{cp} = 210\,\frac{d}{E} \quad [\mathrm{ns}] \qquad (3)$$

for holes, where the detector thickness d is expressed in microns and the electric field in V/cm. These expressions are valid in the regime where the mobility remains constant, i.e. $E < 10^4$ V/cm. For example, a field of 5×10^3 V/cm and a detector thickness of d = 300 μm result in collection times of t_{cn} = 4.4 ns and t_{cp} = 13 ns for electrons and holes, respectively. Since the diffusion coefficient is proportional to mobility, whereas the drift time is inversely proportional to it, the resulting transverse diffusion is the same for both electrons and holes:

$$\sigma_x = 23\sqrt{\frac{d}{E}} \ [\mu m] \qquad (4)$$

where the detector thickness is expressed in microns and the electric field is given in units of V/cm. Again, for simplicity, the electric field is assumed to be constant throughout the detector. For our previous example of d = 300 μm and E = 5 x 10^3 V/cm the maximum transverse diffusion is 5.6 μm. For d = 100 μm and E = 10^4 V/cm, both of which represent practical limits for large-scale detectors, the resulting spread is 2.3 μm.

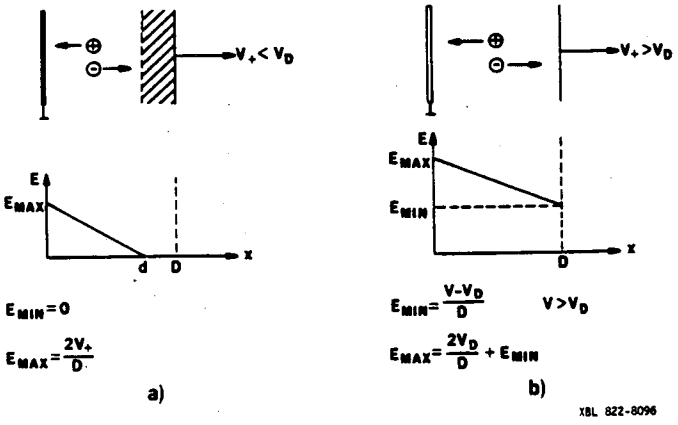

Fig. 2. Electric field profiles in semiconductor detectors: a) partial depletion, b) total depletion with overbias.

The obtainable position resolution is not limited to the magnitude of the transverse diffusion, since the charge induced on several electrodes can be evaluated to determine the centroid of the distribution. Although charge is induced on many strips—over a spatial extent comparable to the detector thickness—the charge will integrate to zero, except on those strips where carriers are actually collected. Thus, transverse diffusion is not necessarily an impediment, but can be a tool to improve position resolution beyond the limits of feature size. In principle, the peak of the signal induced on the other strips could be used for interpolation, but in a large-scale system this is not always feasible, especially for short collection times.

The accuracy of the interpolation is dependent on signal-to-noise ratio. The charge signal increases with the thickness of the detector. However, the allowable thickness of vertex detectors is limited by multiple scattering in the detector, which limits the accuracy of vertex reconstruction. In practice, one therefore has to work with the minimum energy loss commensurate with the noise threshold. A signal-to-noise ratio of five or more is necessary to measure the Landau distribution. Since the total charge is typically distributed over several electrodes, it must be 15 to 20 times larger than the noise level of one channel.

Hyams, et al. [8] have demonstrated 5 μm rms resolution in a silicon strip detector using 12 μm wide strips with a center-to-center spacing of 20 μm. In this measurement only every third strip was read out—the induced charge from the intermediate strips being coupled to the preamplifier by the interelectrode capacitance [11]. The detector was 280 μm thick and the electronic noise was 750 electrons.

In a CCD detector array the thickness of the depletion region is of the order of 10 μm. Therefore, transverse diffusion is of no importance in these devices. Furthermore, the individual elements are isolated from one another—the position resolution is then determined by the pixel size.

The number of data channels in a high resolution vertex detector is formidable. A pp collider with 1 TeV c.m. energy and a luminosity of 10^{33} $cm^{-2}s^{-1}$ has an interaction diamond about 40 cm long and a few mm wide [12]. The vertex detector would typically consist of several layers at radii of 1 to 5 cm. Even in a scaled down scenario the number of electronics channels can easily be of the order of 10^5. Clearly, a compact and efficient arrangement of low noise electronics is essential for these systems.

Electronic Noise

Electronic noise is determined by the equivalent spectral noise density at the input of the system and by the subsequent pulse shaping, which defines the noise bandwidth. For this discussion we shall assume a simple RC-CR shaper, i.e. one formed by a single integrator and differentiator. These results can easily be extended to more complex passive and time variant (e.g. gated integrator) schemes [13,14]. It should be emphasized that the shape of the pulse measured at the input of the ADC is not necessarily indicative of the time constants that determine the noise bandwidth of the system. The pulse decay caused by the input time constant of a current sensitive preamplifier, for example, does not reflect the suppression of low frequency noise.

The optimum signal-to-noise ratio in a RC-CR shaper is obtained for equal integration and differentiation time constants τ. For a step input the output pulse peaks at a time t = τ. The equivalent noise charge is:

$$\langle Q_n^2 \rangle = \left(\frac{e^2}{8}\right) \left[\left(2q_e I_s + \frac{4kT}{R_p}\right) \tau + e_n^2 \frac{C^2}{\tau}\right] \qquad (5)$$

The first term gives the contribution due to input noise current sources: 1) Shot noise, due to detector leakage current and the input current of the input transistor, both lumped together as I_s. 2) The thermal noise current of any resistors (at temperature T) connected parallel to the input, represented by R_p. Since these sources are shunted by the input capacitance C their noise contribution is reduced at high frequencies due to the decrease in capacitive reactance; their importance therefore increases with shaping time. The second term is the contribution due to the equivalent input noise voltage whose spectral density is e_n. The constants in this equation are the electron charge q_e, the Boltzmann constant k and e = 2.718.

This expression for the equivalent noise charge can be more conveniently assessed in the following form:

$$\langle Q_n^2 \rangle = 12 \bullet I_s + 6 \bullet 10^8 \frac{\tau}{R_p} + 3.6 \bullet 10^4 \bullet e_n^2 \frac{C^2}{\tau} \qquad (6)$$

where Q_n is expressed in electrons, I_s in nA, τ in ns, C in pF, R_p in ohms, and e_n in nV/√Hz.

In practice, R_p can usually be selected large enough to make its noise contribution negligible and we shall therefore ignore this term. Then, selection of the optimum input device, its operating point and the shaping time depend on the balance between the first and last terms of Eq. 6.

Knowledge of the detector capacitance is required to evaluate the last term in Eq. 6. In addition to the capacitance of an electrode to ground, we must also consider its capacitance to the neighboring electrodes, since the associated preamplifier inputs present a low impedance to ground to reduce cross coupling (Fig. 3). In an arrangement where the strip geometry is small compared to the thickness of the detector the capacitance is dominated by the strip-to-strip capacitance and is affected only little by the thickness of the detector. Signal-to-noise ratio therefore scales linearly with detector thickness, i.e. energy loss, and not quadratically, as is usually the case.

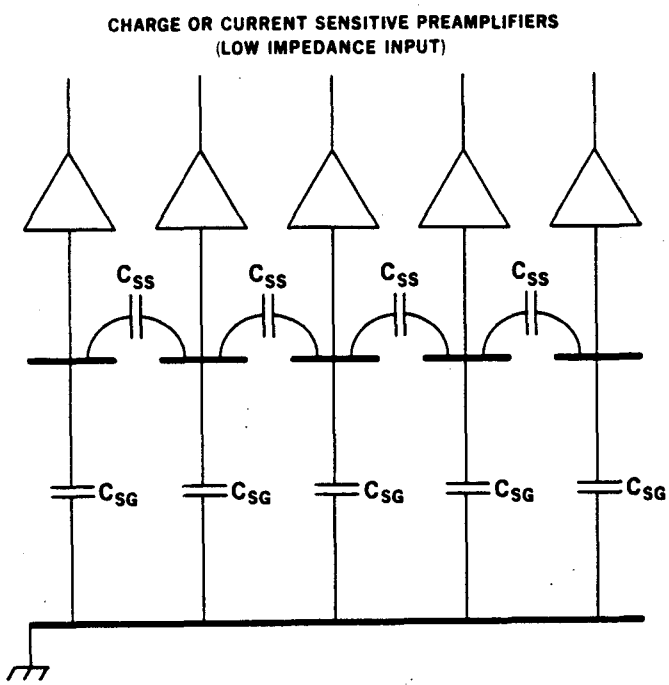

Fig. 3. Capacitive load presented to a preamplifier by a multielement detector. Note that the adjacent strips are effectively grounded by the low input impedance of the preamplifiers.

The capacitance between two isolated 10 μm wide strips with a center-to-center spacing of 20 μm is about 0.9 pF/cm [15]. The total capacitance of an array of many strips is about twice this, i.e. 1.8 pF/cm. A strip length of 4 cm leads to a load capacitance of about 7 pF per strip. If, for example, only every third strip is connected to a low impedance readout channel and the intermediate strips are left floating (for transients), the capacitance is reduced to one third of this value. Decreasing the width of the strip to 5 μm at the same pitch would reduce the capacitance by only 15%. Conversely, increasing the width of the strips to 15 μm increases the capacitance by roughly the same amount and makes the choice of strip geometry rather flexible.

We shall now assess the noise performance of bipolar and field effect transistors. The devices used for this comparison are not necessarily economically feasible, but have been chosen to demonstrate potential performance.

Bipolar Transistors

The optimum operating point of a bipolar transistor depends on the selected shaping time constant and the total capacitance. Besides the detector capacitance, the latter includes the transition capacitances of the base-emitter and base-collector junctions and the emitter diffusion capacitance

$$C_{De} = \frac{I_e}{\omega_o} \cdot \frac{q_e}{kT} \tag{7}$$

where ω_o is a characteristic frequency associated with carrier transport in the base. The optimum emitter current is

$$I_e = \frac{kT}{q_e} (C_D + C_T) \frac{1}{\sqrt{\frac{1}{\omega_o^2} + \frac{\tau^2}{B}}} \tag{8}$$

where C_D is the detector capacitance (including strays) and C_T is the sum of the emitter and collector transition capacitances. C_T and ω_o can be inferred from a plot of $1/f_t$ vs. I_e [16]. The optimum shaping time constant is

$$\tau_{opt} = r_e \cdot (C_{Te} + C_D + C_{De}) \cdot \sqrt{B} \tag{9}$$

where $r_e = kT/q_e I_e$ is the dynamic emitter resistance and B is the DC current gain of the device. As both B and τ_{opt} are functions of emitter current, an interactive procedure is required to arrive at optimum combinations.

For an NE645, a state-of-the-art microwave transistor, the optimum emitter current for a detector capacitance of 5 pF and a shaping time of 12 ns is 110 μA. For this set of parameters the input noise is about 760 electrons. A shaping time of 25 ns, a more realistic value for a large-scale system, results in an optimum emitter current of 60 μA and an input noise of 670 electrons. However, at such low currents the transition frequency f_t has dropped to a marginal value.

We wish to emphasize that optimum noise with bipolar transistors does not generally occur for capacitive input matching [17], since the effect of input current noise can override the emitter noise term, with which the diffusion capacitance is linked. In the first case the diffusion capacitance C_{De} is 3 pF, compared to $C_D + C_T = 5.8$ pF, and in the second $C_{De} = 1.4$ pF. Capacitive input matching would require an emitter current of 250 μA. Then the optimum shaping time of 12 ns results in an input noise of 840 electrons. Capacitive matching is only a valid criterion if $\omega_o^2\tau^2/B \ll 1$.

Field Effect Transistors

In an FET the DC input current is at least 1000 times lower than in the preceding example. For the shaping times of interest here we can therefore neglect the input shot noise current term in Eq. 6. The internal noise of an FET is often represented by an equivalent noise resistance $R_n = 0.7/g_m$, where g_m is the transconductance. This representation is rather specious in that it ignores hot electron effects that play a major role in most high frequency FET's. The equivalent input noise voltage commonly attains values as much as twice as large as the simple constant mobility model indicates. We therefore characterize the device noise in terms of the equivalent input noise voltage density e_n.

The type 2N3821 JFET, for example, exhibits $e_n = 1.4$ nV/√Hz at a drain current $I_D = I_{DSS} = 1$ mA [18]. The input capacitance C_{iss} is 6 pF and therefore provides a good match to the 5 pF detector used in the previous examples. At a shaping time constant of

12 ns, the equivalent noise charge is about 840 electrons. At a shaping time of 25 ns, the noise is 580 electrons. At longer shaping times the FET clearly outperforms the bipolar transistor. The 2N3821 is not a state-of-the-art device and our device modeling indicates the feasibility of even better performance. MOS devices offer high g_m/C_i ratios and also seem well suited for this application since low frequency excess noise is of little importance at small shaping times.

Power dissipation is a prime consideration in high-density, large-scale detector systems. Although FET's tend to exhibit minimum noise at drain currents approaching the saturation drain current I_{DSS}, the operating current can be reduced significantly with only a moderate increase in noise. At a drain current $I_D = 0.1 \times I_{DSS}$, the noise may increase by as little as 30 to 40%. Furthermore, FET's can be specifically designed to reduce power requirements, although this works against optimization of signal-to-noise performance. Table 1 shows the tradeoffs associated with various design parameters, where the ratio of transconductance to input capacitance is used as a figure of merit for low noise. In addition, hot electron effects

Table 1. FET Design Tradeoffs

	Signal/Noise	Power Dissipation
Channel Depth d	$\propto d^2$	$\propto d^5$
Channel Length l	$\propto 1/l^2$	$\propto 1/l$
Doping Level N_d	$\propto N_d$	$\propto N_d^3$

must also be considered, inasmuch as they increase the equivalent input noise by both increasing the intrinsic channel noise and reducing device gain. The electric field in the channel can be kept at appropriately low values by reducing the depth and the doping level of the channel. Fortuitously, these steps also lead to reduced power dissipation.

The viability of large-scale multielement semiconductor detector systems hinges on readout circuitry that does not occupy more space than the detectors. Stray capacitance and signal pickup must be kept to a minimum, precluding remote front ends, and readout must be fast to handle high event rates. These requirements can only be fulfilled by monolithic integrated circuitry in close proximity to the detector.

Readout Schemes

CCD detector arrays are inherently attractive as they furnish their own readout. However, readout times are long: milliseconds to tens of milliseconds in current detectors [4,5]. CCD operation has been demonstrated at pixel transfer rates in excess of 50 MHz [19], but the readout time of a 380 x 488 pixel array still exceeds 4 ms. Amplitude measurement is a problem at these high readout rates, since this requires extremely clean recovery from clock and reset transients.

Linear CCD arrays could be used to read out strip detectors. Readout time might be restricted by using several CCD's, each reading out a subset of the strips. This scheme has the problem of severe capacitive mismatch between the CCD and the detector, so that only a fraction $1/(1 + C_D/C_{CCD})$ of the signal charge is transferred from the detector to the CCD. Typical values are $C_{CCD} = 0.01$ pF and $C_D = 5$ pF, leading to a transfer efficiency of 0.2%. Even an optimally matched arrangement invokes a degradation of signal-to-noise ratio by a factor of two. This penalty can be circumvented in a bipolar transistor CCD [20], where the detector charge is drained into the low input impedance of a common base transistor stage. The discharge time constant is limited, however, by the maximum allowable emitter current commensurate with negligible charging of the detector capacitance, i.e. fluctuations in the number of stored charge carriers between readout cycles.

An alternative approach to detector readout is an input multiplexer. Here, the signal charge is stored on the detector capacitance until its associated input stage is activated. One implementation of this is the gated charge sensitive preamplifier IC designed at the Stanford Integrated Circuits Laboratory [21]. This device is to be used in the proposed silicon strip vertex detector for DELPHI.

A very attractive approach is the two-dimensional multiplexer described by Gaalema [22]. Here a checkerboard array of detector elements is bonded by indium bumps to the readout chip. Since this is a random access array, a coarse position determination can be performed by an auxiliary detector (or possibly by segmenting the opposite face of the detector) and only the relevant pixels have to be read out. Due to the low capacitance of a pixel as compared to a strip, a noise level of 40 electrons has been demonstrated and $Q_n = 10$ electrons should be possible. To a certain extent, position resolution in these devices is limited by the area required by each readout cell, although interpolation could provide better position resolution than the cell size, which is limited to about 25 μm by present technology.

The CCD and multiplexer readouts described above are hybrids, i.e. the detector and the readout electronics are located on separate chips and must be connected by some ingenious means, either by intricately arranged bonding wires, as in the proposed DELPHI vertex detector, or by the indium bump method. Is it possible to avoid these difficulties by integrating front-end and readout circuitry directly on the detector chip?

Kemmer [23,24] has demonstrated the advantages of low temperature processing in detector fabrication. Thus, high temperature processing steps should be avoided when implementing additional circuitry on the detector wafer. Recent developments in low temperature annealing and activation of ion-implanted dopants indicate that MOS or CMOS devices could be successfully incorporated on the detector chip. Bipolar transistors pose some problems due to the high doping levels involved. Conventional epitaxial JFET technology is clearly incompatible, but fully implanted structures should be feasible. An open question in low temperature FET processing is if crystal regrowth and dopant activation are good enough to provide low noise. Considerable work remains to be done in this area. It is also questionable whether the combined yields of the detector and the readout circuitry are sufficient to allow a monolithic approach.

A completely different approach to the readout problem is offered by the semiconductor drift chamber [25]. Here the number of electronics channels required is significantly reduced over strip or multi-pixel detectors. Furthermore, its low capacitance simplifies the task of achieving low noise. However, questions of carrier trapping in low field regions in these devices still remain to be answered [26].

The last point leads to an extremely important consideration for all semiconductor devices operated near high luminosity regions: radiation damage.

Radiation Damage

Semiconductor devices are sensitive to radiation damage. The two effects of greatest importance in this context are:

- Bulk crystal damage: This type of damage results in reduced carrier lifetime. In the detector this leads to increased reverse current, and therefore noise. At higher levels recombination reduces the charge signal. This is especially important in the semiconductor drift chamber, where the collection time is of the order of microseconds. In bipolar transistors reduced carrier lifetime in the base emitter junction leads to a degradation in low current performance, a key aspect in low power front-ends. This also applies to the bipolar transistor CCD described by ten Kate [20].

- Charge buildup in oxides: In the oxide layers of MOS devices radiation leads to charge buildup. This affects the threshold voltage, and therefore the operating point in linear circuits. In logic circuitry this eventually leads to impaired switching performance. This phenomenon is most pronounced in n-channel devices. In a detector, charge buildup in the oxide passivation layers between adjacent strips or pixels could lead to reduced interelectrode resistance and eventual deterioration of input noise.

Conclusive data which are directly applicable to these specific aspects do not exist. Especially the effects of radiation damage on the noise of MOS devices have yet to be investigated in a systematic manner. Nevertheless, some general estimates are possible. Radiation damage in hardened MOS devices generally becomes significant at doses of 10^5 to 10^6 rad, corresponding to about 10^{13} to 10^{14} minimum ionizing particles. A luminosity of 10^{33} $cm^{-2}s^{-1}$ leads to a total flux of 5×10^8 charged particles per second [27]. If we assume a radiation hardness of 10^{14} particles, the lifetime of the readout logic at 1 cm radius would be one month. We should expect analog circuitry to suffer severe deterioration in a much shorter time.

Whereas radiation damage in MOS structures is primarily caused by charge buildup due to ionization processes in the oxide, the lifetime of junction FET's is limited by the degree of displacement damage in the bulk. Thus, they are more affected by heavy particles, e.g. protons and neutrons. The isolation technique used in integrated JFET structures tends to limit radiation hardness; nevertheless, neutron radiation hardness of 10^8 rad has been demonstrated [28]. Clearly, JFET readout technology should be pursued, but it should be noted that its success hinges on the effectiveness of low temperature annealing and activation processes.

The outlook regarding the radiation hardness of semiconductor vertex detectors for high luminosities can be summarized in the following manner (implicitly remembering the appropriate caveats):

- Sufficiently hard integrated readout electronics can probably be implemented in JFET technology.

- Bulk damage in the detector is tolerable to the extent that the reverse current does not exceed several microamperes per electrode. Detector lifetime will probably be limited by deteriorating interelectrode isolation. We expect this to be the process that limits overall detector lifetime.

The problem of interelectrode isolation may indeed be solvable, for example by interleaved guard electrodes. We should also note that the field in the isolation oxide is much smaller and its distribution is quite different than in an MOS capacitor; thus charge buildup should be less. To a certain extent, this type of damage can be repaired by annealing at temperatures of a few hundred degrees Celsius [29], possibly in situ. Additional research is certainly necessary in this area, and it may turn out not to be a problem at all.

Alternative Detectors

In the preceding discussion we have treated detectors that respond directly to traversing particles. However, there is another class of semiconductor detectors which may well have a much greater impact on high energy physics detectors: photodiodes to detect scintillation light.

Fibers of scintillating glass can be drawn to diameters of a few microns and have been suggested as an alternative for vertex detectors [30]. The light from these fibers could be "piped" to arrays of photodiodes, which would be far enough removed from the interaction region to greatly extend their lifetime. Scintillating glasses can be quite radiation hard and good performance at doses in excess of 10^7 rad has been demonstrated [30]. Light absorption is still a problem in these fibers and additional research may be fruitful.

Photodiode readout should also be useful in fast, fine-grained calorimeters using high-density scintillators. BaF_2 has recently caused considerable excitement due to its 800 ps decay component at 220 nm [31]. However, the more intense 310 nm emission has a decay time of 620 ns and limits the rate capability. CsF has only one emission component at 390 nm with an overall decay time of about 5 ns [32]. Its density is 4.1 g/cm^3 and the light output is about 5% as compared to NaI(Tl). A 1 cm thick CsF crystal coupled to a photodiode with 60% quantum efficiency would yield about 8000 photoelectrons. If the photodiode has an area of 1×1 cm^2 and a thickness of 300 μm (C = 35 pF) the electronic noise is about 2000 electrons at a shaping time of 10 ns. The signal-to-noise ratio of four is marginal, especially since light losses have been neglected in this estimate. Clearly, the choice of geometry will greatly affect the obtainable signal-to-noise ratio, but this example does illustrate that a moderate amount of internal gain in the photodiode could provide the "headroom" required in a practical system.

Large-area photodiodes--or arrays of photodiodes--are notoriously difficult to fabricate with good gain uniformity over the detector area. However, as will be shown below, these problems are severely exacerbated at high gains. If the gain is restricted to roughly ten, careful application of current processing technology should provide avalanche photodiodes of several cm diameter with reasonable yields.

The optimum structure for an avalanche photodiode (APD) having a response time of 5 - 10 nanoseconds is the reach-through structure shown schematically in Fig. 4 [33]. Photons impinging on the p^+ contact are absorbed in a very shallow layer, typically not more than a few hundred nanometers thick for scintillation light. The primary electrons drift to the localized high field region established by the internal p layer. Here secondary electrons and holes are created by impact ionization. The secondary holes drift through the low field region to the p^+ contact and contribute the major portion of the total induced charge. This structure has several advantages over other types of APD's:

- Only those primary carriers with the higher ionization coefficient are transferred to the avalanche region. This is essential for low avalanche noise and good stability.

- The field in the avalanche region is primarily determined by the charge in the intermediate p layer. In a proper design the field will be relatively unaffected by doping variations in the bulk material.

- The avalanche field profile can be quite flat, even with realistic charge profiles. This allows use of a lower field for a given gain, which further improves stability.

- The detector can be made much thicker than the avalanche region to reduce capacitance.

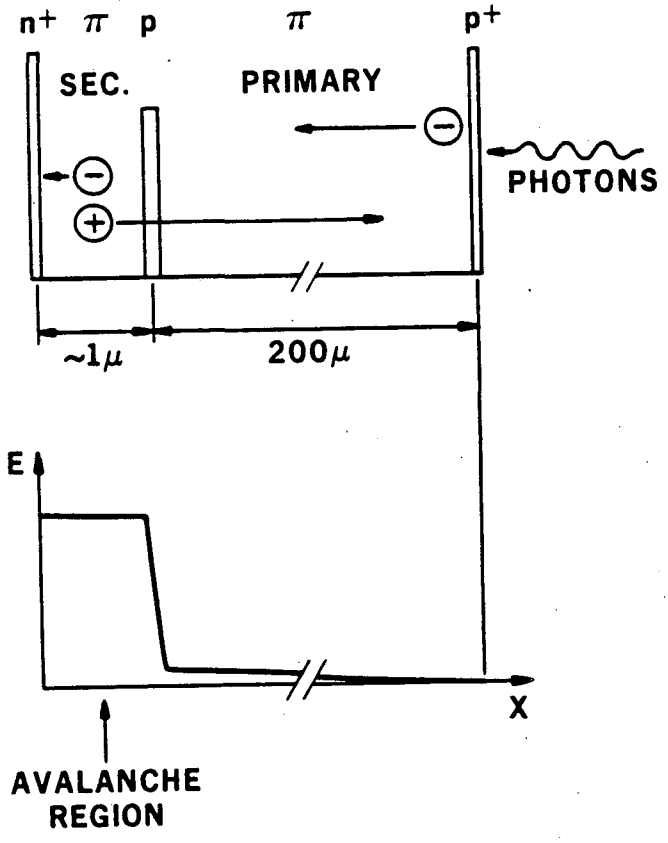

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Fig. 4. Schematic representation of a reach-through avalanche photodiode.

Breakdown will occur as the gain is increased to the point where the gain of the secondary holes approaches two. Thus, the obtainable gain is limited by the ratio of electron to hole ionization coefficients. Only in silicon is this ratio significantly greater than one.

The gain is an exponential function of the width of the avalanche region times the ionization coefficient. The ionization coefficient in turn is an exponential function of field. Thus, both the width and the field, i.e. the charge deposition in the intermediate p layer, must be precisely controlled to obtain good gain uniformity.

Most work with reach-through APD's has been done on devices where the high field region is formed by deep p and n diffusions [34], which are difficult to control accurately. At LBL work is proceeding on a fully ion-implanted structure where the high field region is defined by a deep boron implant. By carefully considering geometrical effects and the interleaved Lissajous patterns formed during scanning, the nonuniformity of an ion implanted layer can be kept to 0.5%. We are investigating both low temperature and flash annealing techniques to activate the implanted dopants without significant diffusion. This should considerably reduce the susceptibility to diffusion spikes and other variations caused by lattice imperfections.

Figure 5 shows the doping profile in the avalanche region of a fully implanted reach-through APD as calculated by the process simulation code SUPREM III [35]. Figure 6 indicates the relative gain variation vs. gain for a doping variation of 0.5%. It also shows the relative variation of gain with a change in width of the avalanche region, again as a function of gain. Both curves illustrate the severe demands imposed on process control. However, fabrication of moderate gain devices with reasonable yields does indeed seem to be feasible. Considerable work remains to be done in this area, also with regard to additional problems associated with segmentation [34].

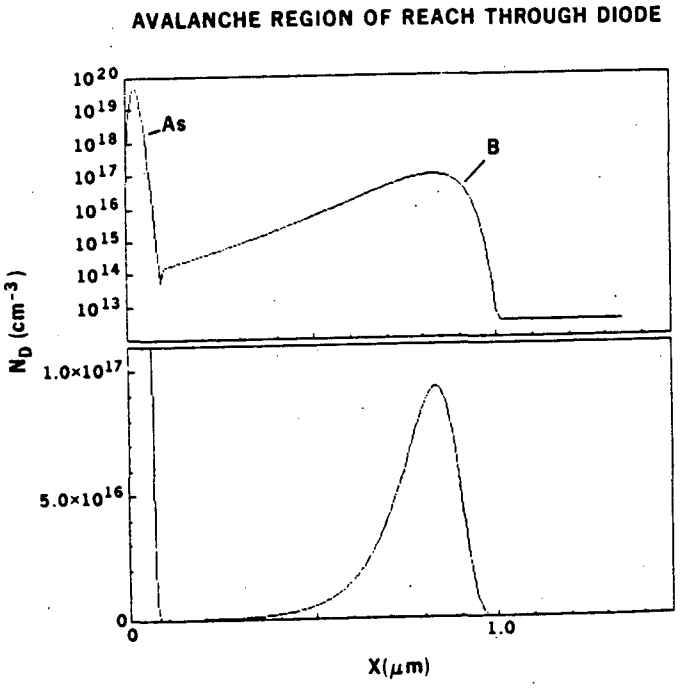

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Fig. 5. Doping profile in the avalanche region of a fully implanted reach-through avalanche photodiode. The intermediate p layer is formed by implanting boron ions with an energy of 400 keV.

Conclusion

Semiconductor detectors can provide a position resolution of several microns or less. In this respect they surpass other detector types currently known. However, in a vertex detector this advantage can only be exploited if compact and fast readout IC's are available and if the detector and readout can withstand high radiation doses for a reasonable time. Although the lifetime could be prolonged by placing the detector at a greater distance from the interaction region,

this becomes self defeating at radii greater than 5 or 10 cm, since high pressure drift chambers then provide adequate resolution with a lower level of technical sophistication. Nevertheless, we wish to emphasize that these problems are not necessarily insurmountable; we just don't have enough data to assess the magnitude of the problem in this specific application.

There is a wide range of applications for semiconductor photodiodes with moderate gain. These would provide much greater geometrical flexibility than photomultiplier tubes and would also be unaffected by high magnetic fields. We believe that the fully implanted structure described above could be fabricated with sufficiently high yields for large-scale detector systems. This will require a significantly higher degree of control over processing steps than is customary in commercial device fabrication, but this can be achieved.

We have discussed the potential and the problems of semiconductor devices for large-scale detector systems in high-energy physics. The problems which need to be solved have been identified. The questions which need to be answered in order to establish whether these systems can be viable are well defined and could be answered in the near future. Although the talented amateur can contribute in this area, it will take the combined efforts of materials scientists, device physicists, process engineers, systems designers, and experimentalists to solve the problems on the path towards a useful detector system.

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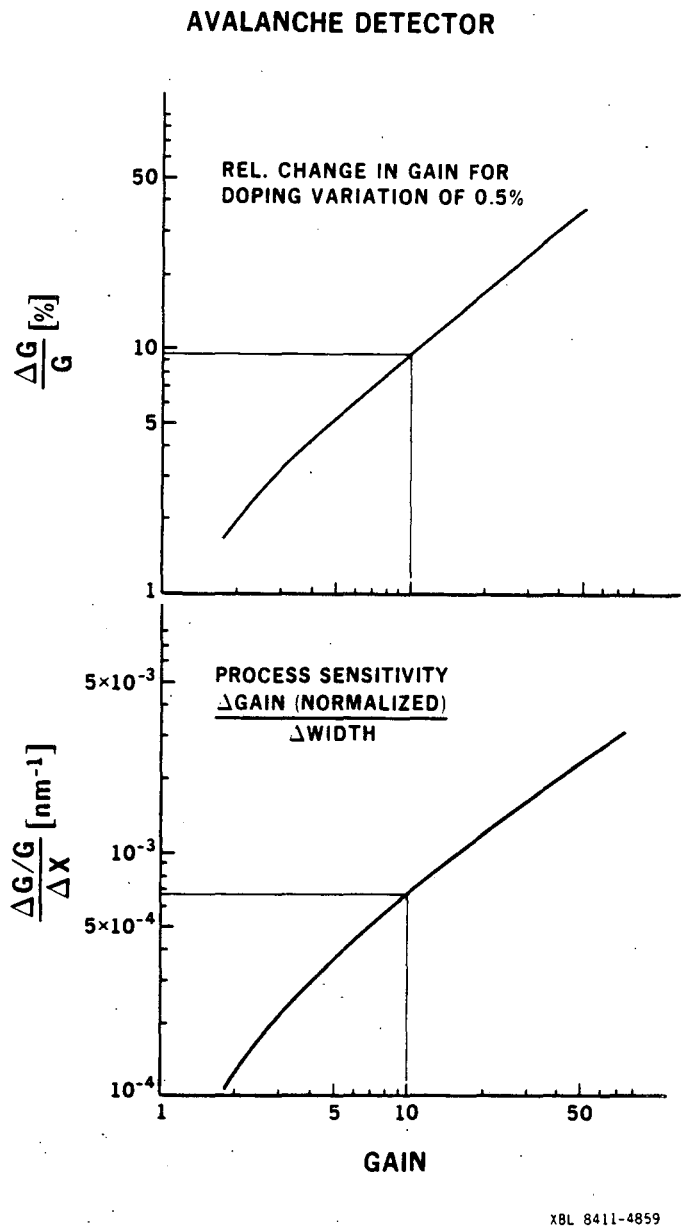

Fig. 6. Sensitivity of gain with respect to changes in dopant deposition and width of the avalanche region for the APD structure shown in Fig. 5. The change in gain ΔG is normalized to the gain G.

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