LBL-2053
c.1

A MULTIWIRE PROPORTIONAL CHAMBER (MWPC) COINCIDENCE MATRIX

Michael G. A. Harms
(M.S. Thesis)

June 1973

Prepared for the U. S. Atomic Energy Commission
under Contract W-7405-ENG-48

For Reference

Not to be taken from this room

LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
BERKELEY

LBL-2053
c.1

DISCLAIMER

This document was prepared as an account of work sponsored by the United States Government. While this document is believed to contain correct information, neither the United States Government nor any agency thereof, nor the Regents of the University of California, nor any of their employees, makes any warranty, express or implied, or assumes any legal responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by its trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof, or the Regents of the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof or the Regents of the University of California.

A MULTIWIRE PROPORTIONAL CHAMBER (MWPC) COINCIDENCE MATRIX

Michael G. A. Harms

June 1973

ABSTRACT:

A brief explanation of the physics of multiwire proportional chambers and their uses in high energy physics experiments is given. This particular project attempts to resolve "coincidently" pulsed wires on different chambers for five physically different experimental configurations. It employs three general types of circuits, each functionally distinct. Driver units provide line termination, signal regeneration, and fixed time delay insertion. Matrix boards govern the "valid coincidence pairs" as determined by the physical arrangement of two sets of MWPCs and the experimenter's target. Receiver boards counteract crosstalk while providing a "coincidence" output only when the predetermined pairs of wires from separate MWPCs are activated. A prototype model is discussed, and results from the completed boards are explained in their relationship to the project requirements.

TABLE OF CONTENTS

	Page
INTRODUCTION	1
Multiwire Proportional Counters	2
Scope of This Project	3
PROJECT REQUIREMENTS	5
Timing	5
Noise Immunity	6
Flexibility	7
Size and Cost	7
CIRCUIT SELECTION	9
Valid Coincidence Pairs	9
System Overview	11
BREADBOARD MODEL	13
Timing	13
Signal Jitter	14
Crosstalk	14
DRIVER UNITS	15
Functions	15
Matrix Location	16
Variable Time Delay	17
Power Considerations	17
MATRIX BOARDS	19
Physical Description	19
Programmable Matrix Board	21
Pull-Up Resistors	22

Page

Fuses 23

Component Testing 23

RECEIVER BOARDS 25

Differential Receiver 25

Wire-Wrapping 26

Propagation Delay Time 26

Load Resistance 27

Fuses 28

POWER SUPPLY UNIT 29

Unused Power Supply Connectors 29

Power Supply Selection 30

PROJECT RESULTS 31

Progress to Date 31

Lab Check Out 31

Future Applicability 32

FIGURES 33

1 Acceptable Signals 33

2 Matrix Generation 34

3 Block Diagram 35

4 Schematic Diagram 36

5 Breadboard Photos 37

6A Driver Unit Power Dissipation 39

6B Driver Unit I 40

6C Driver Unit II 41

7 Dual Matrix Boards 42

Page

8A Artwork, Layout I, Front 43

8B Artwork, Layout I, Back 44

9A Matrix I, 5' Focus 45

9B Matrix II, 5' Focus 46

10 Receiver Board 47

11 Matrix Power Supply 48

TABLE 1 Matrix Hardware Cost Estimate 49

INTRODUCTION

Often, in the macroscopic world in which we live, observation (detection) and interpretation (data reduction) of an event is accomplished by the use of the human senses and is relatively straightforward. But in the sub-microscopic world of high energy physics, the contrary is true. Physical sizes and elapsed times are so small that the human senses are completely useless, and electronic instrumentation must be completely relied upon.

In most high energy physics experiments a beam of subatomic particles is directed electromagnetically or electrostatically onto an experimenter's target. By varying any of many parameters, e.g. target dimensions and location, interacting magnetic fields, and detector sensitivity and location, an experimenter may carry on a search for new knowledge about the physical world. Early in the design of his experiment he must decide on the appropriate detectors required by the constraints of his system.

Detectors are one of the most important parts of any measurement system. For this reason, a great deal of research has been directed toward producing better detectors. Spark chambers filled with an inert gas and bubble chambers filled with liquid hydrogen have been used for years to detect the "spray" of subatomic particles emitted from the target as a result of an incident beam. Recently a new type of detector, named the multiwire proportional chamber (MWPC), has begun widespread use.

Physically, an MWPC is a structure consisting of a square box a few centimeters high. Through the center space is strung a plane of cylindrical wires equally spaced a few millimeters apart. The space is filled with an appropriate gas allowing cylindrical equipotentials around the wires. When an incident charged particle, in this project a proton, passes through the chamber near one of the wires, it avalanches a small amount of charge into the wire. This charge, which is represented in time as a pulse, is amplified to a usable level. With chambers oriented in two axes along the path of the proton beam, both spatial and time resolution may be easily determined.

When a negative pulse is generated on a wire by the development of avalanches, then the neighboring wires simultaneously experience positive pulses. This is independent of the wire spacing. Thus the sensing amplifiers are made sensitive only to negative pulses and, therefore, the wires act as independent proportional counters with a sensitivity, or resolution, equal to half the inter-wire spacing. A rigorous derivation of the mechanism responsible for this automatic decoupling between adjacent wires is given by G. Charpak in "Evolution of the Automatic Spark Chambers", 1970 Annual Review of Nuclear Science.

This project is part of an experiment which employs several MWPCs. Although the methods used are applicable to practically every use of MWPCs, this project is designed for the requirements of this particular experiment. It is part of the detector instrumentation and, as such, may be used with many different physics experiments with the same physical constraints.

The upstream end of this experiment consists of a set of MWPCs with 2mm wire spacing. A set of MWPCs is one horizontal and one vertical chamber corresponding to the X axis and Y axis respectively. These upstream chambers are referred to as P I chambers. Thirty-eight feet downstream is another set of MWPCs, the P II chambers, with 1mm wire spacing. All chambers consist of 64 equally spaced wires. The target, a 10mm square, is movable and may be positioned at a distance downstream of the P II chamber of 5 feet, 8 feet, 14 feet, 26 feet, or 38 feet. This 10mm square is a "virtual target" that the beam is focused to pass through. The actual target is a stationary chamber filled with liquid hydrogen or deuterium, or it may be replaced by a carbon block for other experiments. It is placed immediately downstream of the P II chamber.

When the proton beam is turned on, a particle travels through the P I and P II chambers before arriving at the target location. Depending upon its angle of projection and spatial position it may or may not strike the target. The experimenter needs to know that a "valid event" has occurred when a particle passes through the MWPC chambers with the necessary angle and position so that it would pass through the square "virtual target" if it was not deflected by the actual target. When a valid event has occurred, additional parts of the experiment are activated. The path of flight of the particle is recorded by sending the amplified signals from the P I and P II chambers to flip-flops acting as memory elements.

As will be shown later, one may predetermine all of the coordinates for all possible valid events by using a geometric argument with the chamber

locations and wire spacing. So one could place all the possible valid coordinates in the memory of the PDP-11, used by the experiment for data reduction, and when a particle traveled through the system, the computer could read the coordinate flip flops and determine whether or not the path could produce a valid event. There are 8 signal wires from the chamber amplifiers for each 16 bit computer word. This word gives the wire status and address (chamber location). Through the use of a decoding scheme at the wire amplifiers, the proper word for each event is apparent to the computer. There are a total of 6 chambers in the experiment, although the coincidence matrix only uses 2 of them. Thus, the 12 X and Y planes and some other required experimental data require a total of 20 words per event. To read these words would take about 5 μsec each. Thus, a total of nearly 100 μsec would be required for the computer to analyze each event. Due to the very low ratio of valid to invalid events that the experimenter expects, this dead time is too long. This time <u>will</u> be required to read the coordinates of valid events, but much less time must be wasted in the determination of invalid events. This is where the need for a very fast coincidence matrix to determine event validity arises.

PROJECT REQUIREMENTS

One of the most important constraints on the coincidence matrix is that it produce a decision as to event validity or non-validity as rapidly as possible. During the time required to make this decision, the entire experiment is disabled. If another event occurs during this time, even though it may be valid, it is ignored because the matrix is busy with a previous event. The experimenter has determined that a decision delay time of less than 70 nsec is desirable.

Another time that is of importance to the coincidence matrix is the overlap time required of the two signals to recognize them as being coincident. The matrix will accept signals from both the P I and P II chambers. Designed into the matrix are the coordinate pairs on which signals must exist to produce validity. If signals do exist on any of these pairs of wires in coincidence with each other, then an output pulse indicating validity is issued. Thus the proper P I and P II wires must both exhibit signals that are present together at the matrix for a definite amount of time. This constitutes the required overlap time needed by the matrix components.

The amount of time that the signals may jitter in relation to each other directly affects the amount of time that they overlap one another. The signals from the chambers are negative 40 nsec pulses. The existing jitter between signals coming from corresponding wires of adjacent chambers, i.e. discounting any time-of-flight delays, results from two causes. First, there is up to a 15 nsec wire-to-wire difference depending on the ionization distance.

That is, a signal generated from the avalanche of a particle equidistant between wires may be as much as 15 nsec later than that from a particle which struck the wire directly. And secondly, there may be as much as a 30 nsec time difference due to different input levels to the wire amplifiers. Particles which travel slowly through the chamber impart more energy to the wires than do faster ones. Thus a particle may induce increasing energy levels in subsequent chambers. The amplifier output may vary in time due to the difference between minimum and overdriven inputs. Therefore, the 40 nsec signals may jitter up to 45 nsec, leaving no overlap whatsoever. The matrix must deal with this possibility appropriately.

A final time constraint concerns the passive delays in the system due to the time-of-flight through 38 feet of air and propagation delays through 38 feet of wire. The matrix must, therefore, induce a fixed delay so as to bring the signals together at the same time. The job of the coincidence matrix is not to determine that the particle arrived at the P I chamber first, that is apparent. Its job is to determine that an appropriate pair of P I, P II wires were excited. By "coincidence" in the name "coincidence matrix" it is meant that a single particle excited an appropriate pair of wires. That is, after the matrix eliminates, by fixed delays, the time of flight of the particle from the P I to P II chamber, is an appropriate pair of wires coincidently excited?

Since the amplifier output is at TTL levels, noise immunity over the 38 feet of cables between the chambers must be considered. The matrix is constrained to withstand only 0.4 volts of noise margin unless some TTL to MECL conversion is implemented. Noise margins must also be considered

within the matrix itself because capacitively coupled crosstalk may be present between physically close conductors.

As with most systems, a certain degree of flexibility is required. With this system, flexibility must be present in two forms. First, it must be relatively easy to change the set of "valid coincidence pairs" when the experimenter changes his focal position. It is anticipated that this may be done as often as hourly. This requires that any manual operations performed must be fast, uncomplicated, and easily mastered. If components are removed, they must be readily available and protected from loss or damage while not in use. Also, the contacts interconnecting frequently removed parts must be highly reliable. The second form of flexibility required for this system is that the "valid coincidence pairs" be alterable for any given focal position. If, after the experiment has progressed for a short period of time, the experimenter decides to slightly alter the size of his virtual target, the changes required for the coincidence matrix should be minimal. This stipulates that the available space and power be considered with a safety margin for future possible changes.

And the final demand upon the coincidence matrix by the experimenter is that it be small and inexpensive. There are definite tradeoffs to be considered between size and cost. Engineering time required to fit everything into a small space can easily outweigh the advantages of smaller and cheaper mounting facilities. Crosstalk increases with closer conductors which would be necessary with a smaller system.

All of these constraints influence the circuit configurations employed to determine event validity. Using them, various possibilities may be discarded or weighed objectively. The final circuit configuration selected will be the one which best fulfills them. In the next section, Circuit Selection, they will be a constant guide.

CIRCUIT SELECTION

As stated earlier, all of the "valid coincidence pairs" may be derived geometrically once the chamber locations and wire spacings are known. Since the entire system is identical in both the X and Y axes, the following discussion will only deal with one axis with the understanding that a direct analogy exists with respect to the other one. Figure 1 shows the method used to generate the coordinate pairs that constitute all of the valid or acceptable signals for a given target position.

The basic wire selection criteria is to reject all wires that don't absolutely require particles traveling through them to enter the 10mm square target. An excitation of the P I chamber wire 1, for example, may be caused by a particle traveling through the chamber anywhere within the region from A to B. These points correspond to half the distance between adjacent wires, which is the maximum distance over which an avalanche will occur to a given wire. Therefore, to design for the worst case condition, this discussion will always assume that the particles are the maximum allowable distance from the wire in the direction that results in the smallest set of valid pairs. The price paid for this conservative approach is that the set of valid pairs must be easily alterable in small amounts if, after system operation, the experimenter decides we were conservative to the point of eliminating otherwise valid events.

Again referring to Figure 1, we see that the middle of the P I chamber occurs at point D, exactly midway between wires 32 and 33. Points C and E are each 5mm from D, thus making the CE distance equal to the target height of 10mm.

The maximum P II wire must be below point B' and the minimum wire above A'. Notice that these result from projections coming from 1mm, or half the inter-wire spacing, away from the P I wire 1.

$$\text{MAX} = B'D' - 1/2 \text{ P II wire spacing} = (B'C' + 5\text{mm}) - 0.5\text{mm}$$
$$= B'C' + 4.5\text{mm}$$

$$\text{MIN} = A'D' + 0.5\text{mm} = (A'E' - 5\text{mm}) + 0.5\text{mm}$$
$$= A'E' - 4.5\text{mm}$$

Similar triangles exist between B-C-target and B'-C'-target, and between A-E-target and A'-E'-target. Therefore:

$$\frac{B'C'}{BC} = \frac{X}{38 \text{ feet} + X} \qquad B'C' = \frac{(BC)(X)}{38' + X}$$

Now: BD = (31 wire spaces)(2mm per space) = 62mm
BC = BD − 5mm = 62mm − 5mm = 57mm

Therefore: $$\text{MAX} = \frac{(57\text{mm})(\text{target location})}{38' + (\text{target location})} + 4.5\text{mm} \qquad (1)$$

And: $$\frac{A'E'}{AE} = \frac{X}{38' + X} \qquad A'E' = \frac{(AE)(X)}{38' + X}$$

Now: AD = (32 spaces)(2mm per space) = 64mm
AE = AD + 5mm = 64mm + 5mm = 69mm

Therefore: $$\text{MIN} = \frac{(69\text{mm})(\text{target location})}{38' + (\text{target location})} - 4.5\text{mm} \qquad (2)$$

For the first target location, 5 feet from the P II chamber, the maximum P II wire that may be excited must be below 11.1mm and the minimum wire above 3.52mm for a valid signal to result when P I wire 1 is excited. These are distances from the center of the P II chamber. Counting wires in the chamber leaves the following valid pairs: from (1,22) to (1,29). Wire 64 in the P I chamber will lead to the same P II distances since the chambers are symmetric about their centers. Counting wires, this results in valid pairs from (64,36) to (64,43).

Figure 2 shows the logical extension of this approach into a matrix on which valid (P I, P II) pairs may be shown. Since the system is linear, only two points need to be calculated and then connected by a straight line.

Now the problem is to implement such an array. Conceivably a huge arrangement of AND-OR gates could be used. But aside from the questions of cost is the increasing delay time through each gate. The delay time for the entire project would quickly be consumed in the matrix alone. A faster and more straightforward approach would be to use a receiver into which were coincidently applied only those P I and P II signals that were valid coincident pairs. These pairs could be generated by using a large switching matrix similar in layout to the one in Figure 2. These are, in fact, the guidelines used in designing the coincidence matrix.

A general block diagram for the project is shown in Figure 3. The P I and P II signals come directly from the amplifiers at the wire chambers. Since this system is near the P II chamber, the P I signals must travel through 38 feet of cable. The driver units provide line termination, signal regeneration, and fixed time delay insertion to counteract the passive delays in the system. Passive delays are caused by the chamber positioning, and do not include the signal jitter. The P I signals go through a pair of matrix boards which determine where valid pairs may occur. Thus a single P I wire will enable several of the P I lines to the receiver board. The P II signals are applied directly to the receiver board, one signal per receiver. If a P II signal is applied to a receiver that has been enabled by one of the P I lines, then an output is issued to the remainder of the experiment.

All of the circuits are built using TTL components on CAMAC hardware. The CAMAC equipment is a standardized set of breadboards, called modules, that are housed in a bin, called a crate. The standardization applies to sizes and voltages, not circuits. The use of this standard hardware provides compatability with the rest of the experiment as well as a source of ready-made system hardware.

BREADBOARD MODEL

The matrix has very high speed pulses traveling over wires that are close together. Therefore, capacitively coupled crosstalk may prove to be a severe limitation in the speed of operation for the project. Since it is easier to measure than predict the amount of crosstalk that may be present, a breadboard prototype was constructed. Using the prototype, answers to the following questions were anticipated. Is the delay time through the project small enough? How much crosstalk is present? Is a ground plane or shielding wires between the matrix conductors required? How susceptible to noise pulses is the circuit?

The breadboard model consists of a 5 x 6 diode matrix with 5 possible "chamber" inputs and 6 receivers. It is similar to the receiver and matrix boards of Figure 4. The actual circuit operation will be discussed later. Basically, one board contains the receivers while the other one contains the diodes whose arrangement was generated from Figure 2. The "chamber" inputs come from a function generator with two independent outputs. Thus the passive delays and effects of jitter may be simulated by delaying one signal, e.g. P II, with respect to the other one.

To give the breadboard results credibility, it was built to closely approximate the final circuit selected. Since the matrix system will be placed near the P II location, the P I "chamber" input travels through 38 feet of cable before entering the matrix. As seen from photograph 1 of Figure 5, the time difference between trace 19 and trace 20 results in a fixed delay of about 70 nsec. The propagation delay time through the circuit may be calculated from the same photograph. The P I input arrives at the

matrix board, trace 20, 10 nsec after the center line. The final output, trace X, exits the receiver board about 40 nsec after the center line, thus yielding a propagation time of approximately 30nsec. This time, however. is dependent on signal amplitude and time variations.

Photographs 2 and 3 show the results of simulated signal jitter and hence the required overlap or coincidence time. In these pictures, the P II input is varied from its earliest to its latest time that still results in an output from the circuit. By noting the difference in trace E times, the maximum jitter allowable is calculated to be 110 nsec for 60 nsec input pulses. Since two pulses may occupy 120 nsec and the maximum jitter may be 110 nsec, the minimum coincidence time is 10 nsec. A larger than minimum overlap time results in a stronger output, i.e. larger amplitude and width.

To calculate the amount of crosstalk generated into an unpulsed line, the receiver's P I input, after the last diode in the diode array, is observed. This is the first line that results in an invalid pair. This line should remain at V_{cc} or 5 volts due to the pull-up resistor. However, on near-by lines a 1.5 volt pulse is present. Although this is a sizeable pulse, the receiver has a variable reference allowing it to ignore pulses of up to 2.4 volts. The penalty paid for this increased noise immunity is about a 5 nsec increase in propagation time.

The results of the breadboard indicate that the circuit selected is indeed feasible. The propagation time is less than the maximum allowed, the crosstalk between wires is small enough to be easily overcome thus eliminating the requirement for shielding wires or ground planes, and the passive delays are small enough to be handled effectively, yielding sufficient overlap times for correct operation.

DRIVER UNITS

As indicated by the block diagram, Figure 3, the driver units I and II act as interfaces between the proportional wire chambers and the receiver and matrix boards respectively. They provide three general functions - line termination, signal regeneration, and passive time delay insertion.

The wire amplifiers at the chambers drive the output signals over flat ribbon cables to the matrix system. To prevent signal reflections in the cable, the driver units which receive these signals provide line termination at the characteristic impedance of the cable. The flat cable is driven at TTL levels instead of MECL levels. This results in a lower noise margin but allows compatibility with the rest of the system.

A certain amount of signal amplitude is lost in the flat conductor. This produces signals at the driver unit I and II boards that are weaker than desired. The driver units provide signal regeneration by converting these weak signals back to full TTL levels.

The velocity of relativistic particles in free air is approximately 1 nsec per foot. The velocity of a pulse in a wire conductor is approximately 1.5 nsec per foot. As was seen in the breadboard model, the delay time for the negative pulse in the 38 feet of wire between chambers is 70 nsec. The particle reaches the P II chamber about 38 nsec after it leaves the P I chamber. The pulse applied to the wire at the P I chamber reaches the P II chamber 70 nsec later. The optimum matrix placement is found to be 31.67 feet

from the P I chamber by the following calculation:

Let X = distance from P I chamber

$$1.5\,X = 38 + 1.5\,(38 \text{ feet} - X)$$

$$3X = 38 + 57$$

$$X = 31.67 \text{ feet}$$

This requires the P I pulse to travel through 31.67 feet of cable. The P II pulse time is the sum of the time of flight to the P II chamber and the transit time back through 6.33 feet of cable.

$$\text{P I}: \left(1.5\,\frac{\text{nsec}}{\text{ft}}\right)(31.67 \text{ feet}) = 47.5 \text{ nsec}$$

$$\text{P II}: 38 \text{ nsec} + \left(1.5\,\frac{\text{nsec}}{\text{ft}}\right)(6.33 \text{ feet}) = 47.5 \text{ nsec}$$

However, these exact distances are not physically realistic since the experimental area is typically filled with other equipment. The system will be quite near the P II chamber, but the exact time delays will be determined when the experiment is set up.

The driver unit for each chamber is composed of two wire-wrapped boards, one for each axis. The cost for all 4 boards is detailed in Table 1. The P II driver unit boards, Figure 6C, are simpler than those for P I. They are similar to the P I boards except that they cannot introduce a variable amount of signal delay. Each board consists of 8 sections of 8 signal wires each. Figure 6A shows the circuit associated with one such signal wire. The 100Ω termination resistor is contained in a 14 pin DIP module. This allows a large savings in installation costs since 7 resistors may be inserted into a socket at a single time rather than soldering them onto the board individually. The power dissipated in these resistors is much less than the rating for the

module. The 4 diodes are used for level shifting so that the voltage across the terminating resistor is 2.2V rather than 5V. Each of the 64 SN74S04 inverters uses 10 ma of current. This 0.64 amp requirement is substantially less than the fused level of 2 amps.

The driver unit I boards, Figure 6B, include the ability to introduce a variable amount of delay via a one-shot. This is required for two reasons. First, the signal jitter may possibly be large enough to eliminate any overlap time. Secondly, the P I signal must be delayed so that it arrives at the receiver coincidently with the P II signal. This is, of course, dependent on the location of the matrix system with respect to both chambers. Here it is assumed that the P I signal arrives before the P II signal. However, if the reverse is true, the P I and P II driver units may be interchanged since they are pin-for-pin compatible. The only difference is the use of one-shots instead of inverters on the P I boards. The P I signal will be stretched via the one-shot so that signal overlap is assured.

The timing for these one-shots is set by using an external 5.1KΩ DIP resistor. This yields a 50 nsec pulse. Changing the voltage on this timing resistor changes the "on" time of the one-shot. This is accomplished with a 50Ω potentiometer. By turning the pot clockwise, the voltage may be dropped from 5V to 3.2V (yielding a 150 nsec pulse) while retaining stability. The 51Ω fixed resistor in series with the pot provides current limiting in case the pot is mistakenly turned to 0Ω.

The power consumed by the current limiting resistor, assuming the pot was turned to minimum resistance (worst case), is:

$$P = \frac{E^2}{R} = \frac{(5V)^2}{51} = 0.49W$$

Each of the 32 one-shots consumes 66 ma thus yielding a total current requirement of 2.1 amps. A 3 amp fuse mounted on the power input to the board provides protection against current surges above normal requirements.

The one-shots used are retriggerable; however, this feature is not required for this application. So the "clear" input is always held at a "1" level. The additional unused inputs are also held at a "1" level. Each "clear" input requires 80μa and each unused input requires 40μa for the high state. As a standard guideline, we will not allow the logic "1" to drop more than 2V. Therefore, a single high level is applied to 16 one-shots simultaneously (16 one-shots @ 120μa each through a 1KΩ pull-up resistor = 1.92V drop). Four pull-up resistors achieve this high level for all 64 one-shots on the board. The power dissipated across the line terminating resistors, as calculated in Figure 6A, is the same for both driver unit types.

MATRIX BOARDS

As shown in Figure 3, the matrix boards receive signals from the driver unit I board and send them along to the receiver board. Only the P I signals are affected by the matrix boards. When a pulse occurs on one input wire, all wires which may form a valid coincidence pair with some P II wire are pulsed, thus presenting several pulsed P I wires to the receiver board. The P II wire which is coincidently pulsed from the driver unit II board must form a valid pair with one of these wires for an output to occur.

There are twenty different interchangeable matrix boards that may be plugged into the system depending on the virtual target location. There are 5 foci each with different sets of "valid coincidence pairs", 2 axes for each focus, and, as will be shown later, 2 boards are required for each axis. This large number of identical boards justifies the expense of having special artwork designed on a piece of substrate rather than using a general breadboard with discrete wire interconnections. However, the number of components on each board must be kept to a minimum. For example, any components required by the circuit that may be placed on the driver unit or receiver boards should be put there since there are fewer of these boards. These components would then be common to all foci.

A count of signal wire width and spacing reveals that the matrix cannot fit on one CAMAC board. If the 64 signal wires in the matrix itself were each 100 mils wide and separated by only 50 mils, the total area needed would be 9.6 inches. The useable area of all CAMAC boards is 10.5" x 6.5".

Clearly the matrix must be divided between 2 boards. As shown in Figure 7, when dividing the matrix, care must be taken to preserve the set of valid pairs. Although most of the diode array occupies the second and fourth quadrants, it does extend slightly into the first and third. Assuming that the array were divided between horizontal wires 32 and 33, some overlapping vertical wires would be required on each half. The condition requiring the most overlap, the 5' focus, requires 4 additional wires on each side of the vertical center wire. To allow for future possible alterations, 2 more wires on each half have been provided. This was deemed advisable earlier since the experimenter may wish to alter the set of valid pairs after taking some initial data. Thus, corresponding wires 27 through 38 on both matrix boards must be interconnected in the crate connectors.

The front and back of one board is shown in Figures 8A and 8B. The diodes are mounted in holes, represented by dark circles, in the matrix. The wires are 150 mils wide and spaced 150 mils apart. This large separation helps to reduce crosstalk and eliminate the need for shielding or ground wires between signal wires. As may be seen in Figure 8B, with the grid and connecting wires there is no space left for a ground plane. The actual number of diodes needed on a matrix board depends on the focus. It varies from 190 for the 38' focus to 511 for the 5' focus. There are a total on all 20 boards of 3600 diodes. Components M 7 through M 12 are hex inverters used to invert the inputs and drive negative pulses through the diodes. Positions M 1 through M 6 may be used for line terminating resistors if the matrix and driver unit boards are later separated by an appreciable amount of cable.

Figures 9A and 9B show the matrix schematics for one axis of one focus. The inputs from driver unit I are positive pulses. The inverters produce negative pulses which pull certain output lines low through the diodes. The diodes provide a unidirectional correspondence between input and output lines by preventing backward sneak paths. Thus the valid pairs for a given P I wire are guaranteed to be limited to those output lines connected to the input via diodes.

In addition to the "artwork generated" approach above, another matrix implementation was considered. It involved a programmable matrix breadboard where diodes contained in small pins could be inserted into the matrix where an interconnection between input and output was desired. Schematically it is very similar to the method above. Although less expensive, this approach produced several disadvantages over the 20 independent boards. Every hour the focal position may be changed. When this is done, hundreds of diode pins may have to be removed and reinserted in new locations. This is a time consuming and error-prone operation. Also, the repeated removal and insertion of diode pins will reduce the connector reliability and eventually lead to connection failures.

In addition to the considerations which determine artwork design, other criteria guide the component selection. First, of course, is the propagation time through the matrix. Each signal goes through only one inverter, one diode, and the interconnecting wire. The total time delay is approximately that for the inverter alone. Therefore, high-speed Schottky inverters with a delay time of 5 nsec are used.

When the input pulse is finished, the output lines which were pulled "low" through the diodes must now be restored to their quiescent "high" state. This is accomplished by pull-up resistors on the output lines. These are physically placed on the receiver board so that the resistor on a particular output line may be common for that line on all matrix boards.

This resistor should be small enough to restore the line to its high state quickly and large enough so that too much current does not flow back into the inverter and damage it. When an input is applied, all output lines connected to it via diodes will combine currents to provide the maximum sinking current of the inverter. Although the maximum number of diodes anticipated on an input line is 8, the resistance required is calculated on the basis of 12, thus allowing for possible future changes.

Maximum current though each resistor (Figure 4) $= \dfrac{\text{maximum inverter sinking current}}{\text{maximum number of diodes (resistors)}}$

$$= \frac{20 \text{ ma}}{12}$$

$$= 1.67 \text{ ma}$$

Voltage across each resistor $= V_{cc}$ - (Voltage across diode + inverter output low voltage)

$$= 5v - (0.7v + 0.3v)$$

$$= 4v$$

$$\text{Resistance} = \frac{\text{voltage drop}}{\text{current}}$$

$$= \frac{4v}{1.67 \text{ ma}} = 2.4K\Omega$$

An available resistance of 2.2KΩ is used. The actual current through this resistance is: $I = \dfrac{4V}{2.2K\Omega} = 1.8$ ma

A final consideration in component selection is cost. If 3600 diodes are to be used, their cost must be very low or the 20 board concept is not feasible. A simple switching diode, at a cost of 3¢ each, is used. A complete hardware cost estimate for the project is given in Table 1.

Each board is individually fused to prevent component damage from inadvertent shorts or power surges. The maximum current required by all the active devices is 10 ma per inverter multiplied by 32 inverters, or 0.32 amps. A 1 amp fuse is employed to give adequate protection.

Using inexpensive components requires some form of testing to insure that none of them are defective. Since this procedure, for the matrix boards, is very repetitive, it lends itself nicely to a computer controlled exhaustive search. The search used for this error checking actually checks for three errors:

(1) Components that are defective when purchased.

(2) Components inserted into the matrix backwards (reversed polarity).

(3) Components damaged by overheating during wave soldering.

The method used for this checking involves holding an input line high via a standard CAMAC interface and reading the state of all the output lines. The high-low pattern of all these lines for each input is compared with the desired pattern as determined for all foci from layouts such as Figure 9. If all outputs for each input agree with the patterns desired, a "board OK" message is issued. If an error occurs, the input line which was pulsed and a binary representation of the output pattern is printed. From this output pattern the states of the individual lines are determined and by

comparing them with the desired pattern from a layout like Figure 9, corresponding to the focus in question, the erroneous output line may be determined. This procedure inherently checks both diodes and inverters.

RECEIVER BOARDS

As shown in Figure 3, the receiver board receives both the P II signals from the driver unit II board and the P I signals from the matrix boards. It is designed around a dual differential line receiver as shown in Figure 10. The truth table for the typical SN75108 receiver shown at the bottom of Figure 10 is:

Pin 1 P I	2 Ref	5 P II	4 Output
+		H	H
+		L	H
	+	H	L
	+	L	H

If the P I signal on pin 1 is at least 25 mv more positive than the reference voltage on pin 2, then the output remains high for any P II input on pin 5. However, if the P I input drops more than 25 mv below the reference voltage, the output is an inverted P II input. The reference may be varied via a 1KΩ potentiometer. A nominal setting of 2 volts was determined by the breadboard to be sufficient to eliminate the effects of crosstalk.

The P I inputs, from the matrix boards, enter the receiver board via an auxiliary connector since the regular edge connector has only 86 pins and the board has 128 signal inputs. When a P I line is negatively pulsed, the matrix array simultaneously pulses all the P I inputs to the receiver board

that may form a valid coincidence pair. This enables certain receivers. Now if a corresponding P II input is coincidently pulsed, the receiver reacts by pulling its output low. This is inverted by the SN74S20 acting as a negative OR. The MC1582L is a line driver used to drive the output signal to the executive controller, part of the remainder of the experiment.

Since there are only two receiver boards for the entire project, one for each axis, designing artwork for the board is not justified. Instead the interconnections are made by wire-wrapping individual wires between the pins of the component sockets. If more than 300 wires are to be connected, a computer generated paper tape which controls an automatic wire-wrapping machine is made. In this case there are 680 wires, counting both boards, so the tape was made. This involves formatting the board into data for a system program which sorts the interconnections, finds a shortest path, prints a pin connection listing, and punches the paper tape.

As with the previous sections of the project, the propagation delay time is critical. The longest single delay is in the receiver, 25 nsec, and the time through the entire board is 50 nsec. This compares favorably with the project requirements and is easily understandable since the comparison process and output line driving are performed on this board. Unlike the other TTL components, the receiver and line driver are not Schottky devices. No such components using Schottky techniques are presently available.

The receivers require a logic "1" on pin 6. This is accomplished by wire-wrapping a small 1KΩ, 1/8w resistor between pins 6 and 14 ($+V_{cc}$). They also require a load resistor since they are open collector devices.

The value of the load resistor is calculated using Ohm's law as follows:

$$R \text{ load resistor} = \frac{\text{Voltage across resistor}}{\text{Current through resistor}}$$

Voltage across resistor = $V_{cc} - V_{out}$ low for receiver

Current through resistor = I_{out} low for receiver - I_{in} low for NAND

$$R_L = \frac{5v - 0.4v}{16ma - 1.6\ ma} = 320\Omega$$

A 500Ω load resistance is achieved by connecting two of the existing 1KΩ resistors in parallel and connecting the pair to the open-collector output. This increases the pull-up time slightly but also provides a safety margin in maximum applied current and is convenient.

Using this load resistance the maximum current through the load resistor in the high state is:

$$I_{R_L} = \frac{V_{cc} - V_{out} \text{ high for receiver}}{R_L}$$

$$= \frac{5v - 2.4v}{500\ \Omega} = 5.2 \text{ ma}$$

This 5.2 ma is evenly applied to all receivers that are collector ORed together. Each requires a minimum of 0.25 ma in the high state.

$$\text{Number of gates} = \frac{5.2 \text{ ma}}{0.25 \text{ ma each}} = 20 \text{ gates}$$

Therefore, a maximum of 20 receivers may be collector ORed to one 500Ω load resistor. Only 16 are actually connected together, thus yielding another margin of safety. This forms 4 groups of 16 gates each, which are designated 'A', 'B', 'C', and 'D' on Figure 10.

The power requirements for the board are calculated using the low state

current requirement and the data sheets.

The low state current requirement for the receiver board is found by calculating the current through the load resistance for the low output state of the receivers.

$$I_{R_L} = \frac{V_{cc} - V_{out\ low\ for\ receiver}}{R_L}$$

$$= \frac{5V - 0.4V}{500\Omega} = 9.2 \text{ ma}$$

Load Resistor	4 x 9.2 ma	=	37 ma
Receivers	64 x 30 ma	=	1920 ma
NAND	1 x 10 ma	=	10 ma
Line Driver	1 x 10 ma	=	10 ma
			1977 ma

To protect against current surges while still supplying these requirements, a 3 amp fuse is mounted in each receiver board.

POWER SUPPLY UNIT

All of the circuits in this project are built on CAMAC modules. These are housed in a CAMAC crate which is powered by a separate power supply unit. The crate has space for 25 modules, so some of the matrix boards that are not in use for a particular focus may be stored in the same crate. But connectors and circuit power only exist for the positions used for active circuits. When the focus is changed, the appropriate matrix board is moved from a storage slot to the active slot, and the formerly active matrix board is placed into the storage position.

Standard CAMAC modules have available on their connectors a variety of power options ($\pm$ 6V, $\pm$ 12V, $\pm$ 24V, + 200V, 115 VAC, in addition to 0 volts or power return). The modules for this project do not require these levels; however, the pins reserved for them have been left open so that if one of these modules is absent-mindedly inserted into a CAMAC crate with standard power, the module will not be damaged.

Figure 11 shows a block diagram of the power supply unit used to power the crate. Both power supplies ($\pm$ 5 VDC) include overvoltage protectors and are current limited. The meters provide a quick check on the supply unit's operation. The size of power supply needed is determined from the following tabulation for a complete set of modules for one focus, two axes. This includes 4 driver units, 4 matrix boards, and 2 receiver boards.

$+V_{cc}$ (+ 5VDC):

Inverters (74S04)	192 @ 10ma	1.92
One-shots (74123)	32 @ 66ma	2.11
Pull-up Resistors (2.2KΩ)	128 @ 1.8ma	.23
Receivers (75108)	128 @ 30ma	3.84
NAND (74S20)	4 @ 10ma	.04
Drivers (1582L)	2 @ 10ma	.02
		8.16 amps

$-V_{cc}$ (- 5VDC):

Receivers (75108)	128 @ 15ma	1.92
Drivers (1582L)	2 @ 30ma	.06
		1.98 amps

A 5 volt, 12 amp supply is used for $+V_{cc}$, and a 5 volt, 3 amp supply is used for $-V_{cc}$. These two supplies and their meters are built into a separate rack that is mounted directly beneath the CAMAC crate.

PROJECT RESULTS

The experiment that utilizes the MWPC coincidence matrix has not yet been performed. The ultimate test of the operation of the matrix will come when it is integrated into the whole experiment and the proton beam turned on. Until then, its performance may only be checked in the laboratory under simulated conditions. This has been done and the results show every sign of complete success.

The receiver boards are finished and debugged. The only problem found was in the wire-wrapped wires. One wire was shorted to a post around which it made a 90° bend. A pair of matrix boards has been fabricated and loaded with components. The computer "check out" program works as planned and found a solder bridge on one of the boards which was not found in a visual inspection of the board. The program is saved on the disk so that it may be used as new boards are completed. The other 18 boards are under construction. The driver unit I and II boards are finished and have been checked for correct operation. The power supply is made and works properly.

The operation of the matrix board/receiver board combination was carefully checked in the lab since crosstalk and timing considerations are critical. Although the prototype breadboard indicated that the design would work, it was carefully checked using the actual boards. Again the dual function generator with independent outputs was used.

The coincidence matrix worked even better than the prototype, in that the signals were sharper and exhibited less ringing than previously. This

is due to the lack of wires laying over each other. The nearest non-pulsed P I input line to the receiver board has a 2V negative pulse capacitively coupled to it. The effect of this pulse may be completely eliminated by setting the reference voltage always below 3V. It is nominally set to 2.5 volts. The minimum overlap and passive delay times are the same as measured for the breadboard model and may be easily handled by the driver units. The total propagation time through the entire coincidence matrix is approximately 60 nsec, well within the desired goals set by the experimenter.

The design of the coincidence matrix has been completed and validated by check out of the matrix and receiver boards. This project involved a specific use of multiwire proportional chambers, but the approach taken to determine coincidence of wires from different chambers may be used universally wherever MWPCs are in use. As inter-event times become smaller and the use of MWPCs to determine spatial position more widespread, the need for coincidence matrices such as this will become more acute.

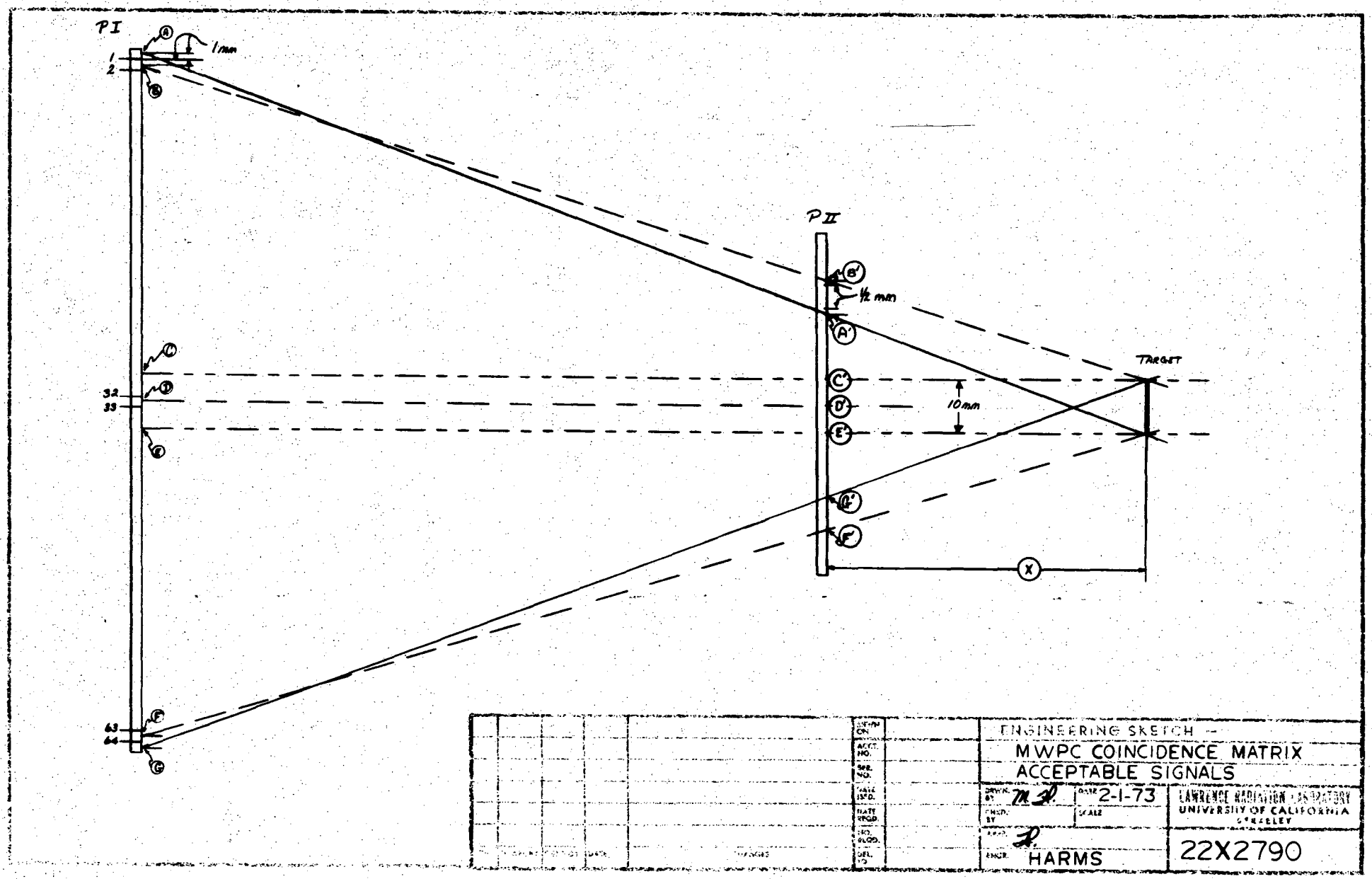


Figure 1

XBL 737-1001

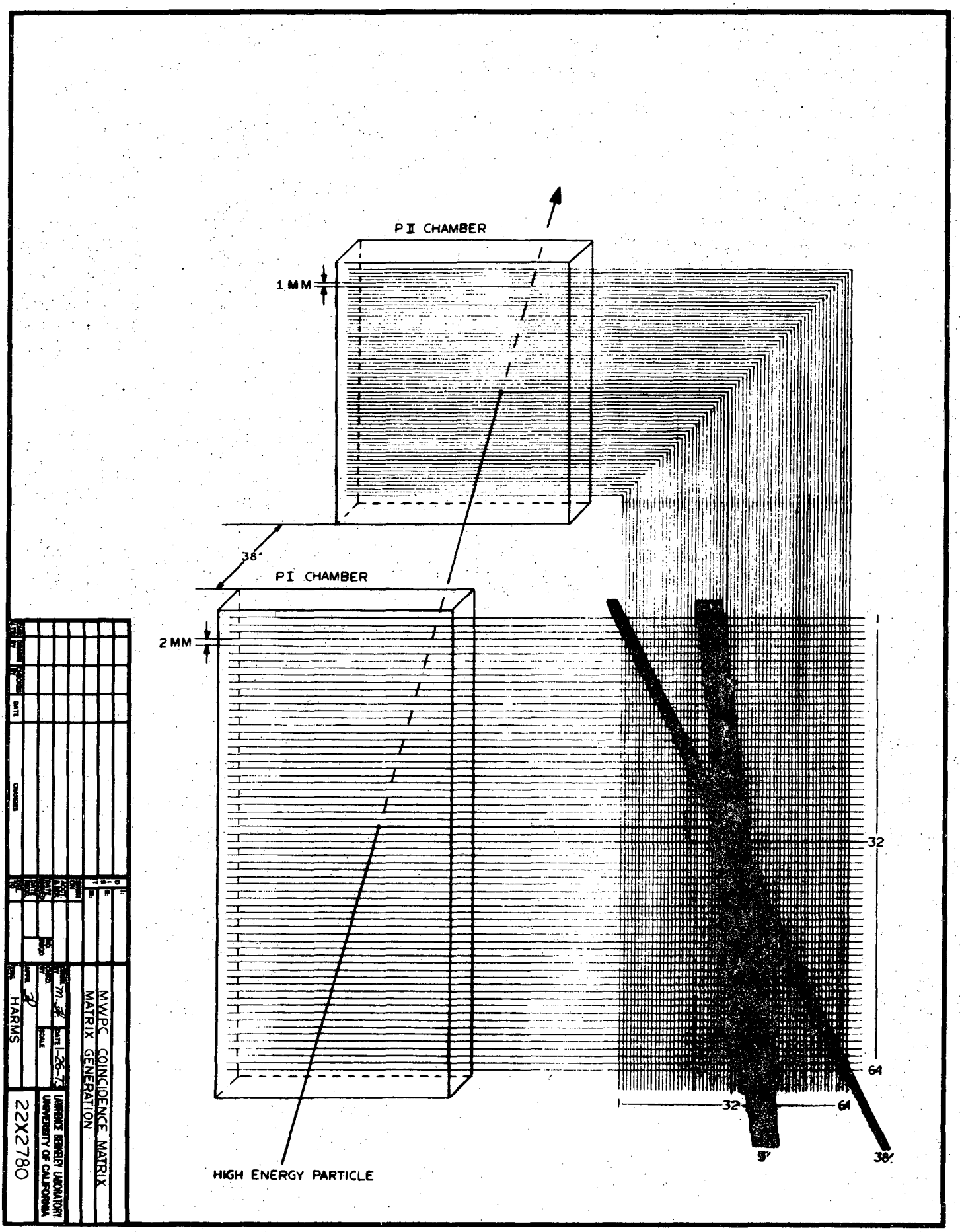


Figure 2

XBL 737-997

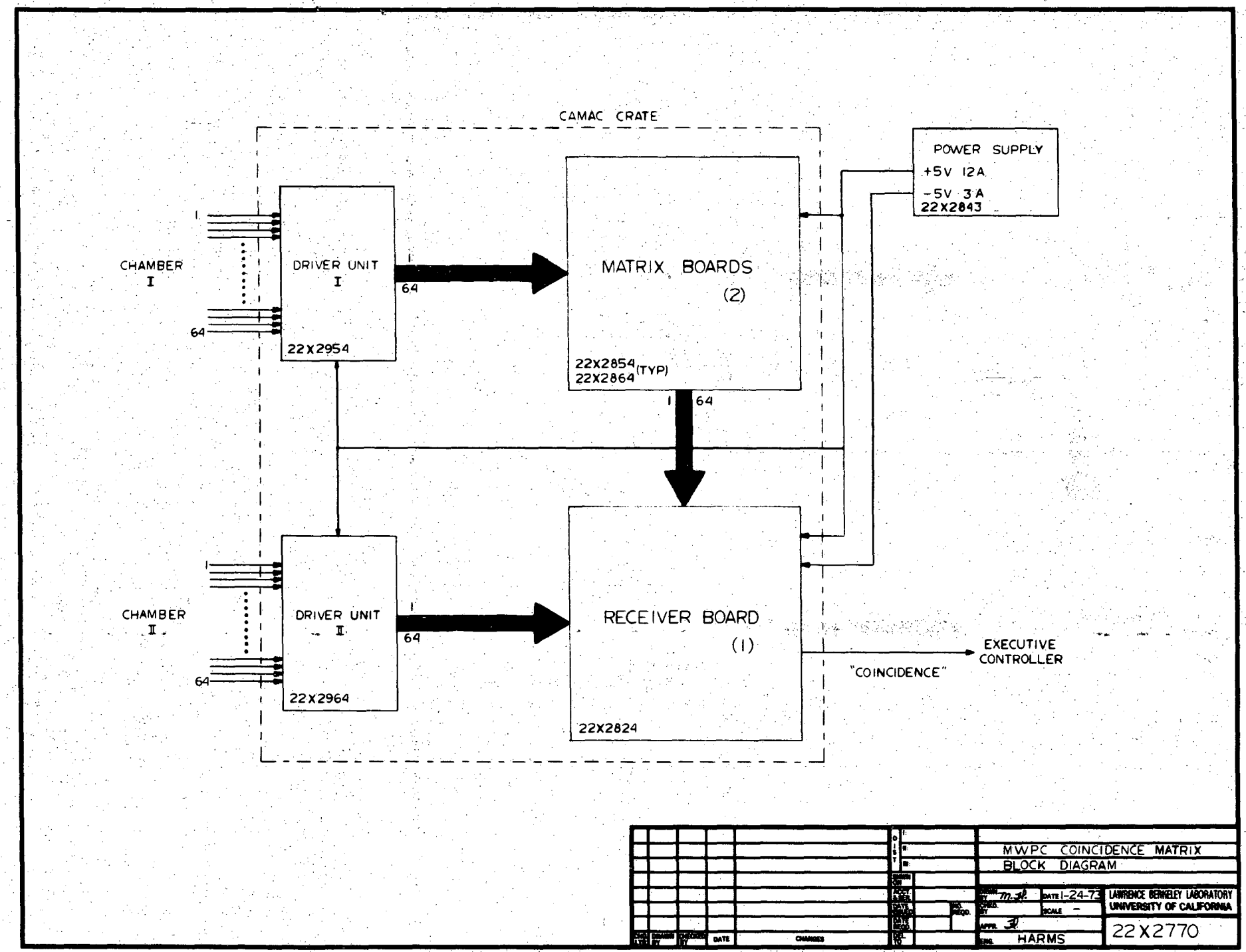


Fig. 3

XBL 737-995

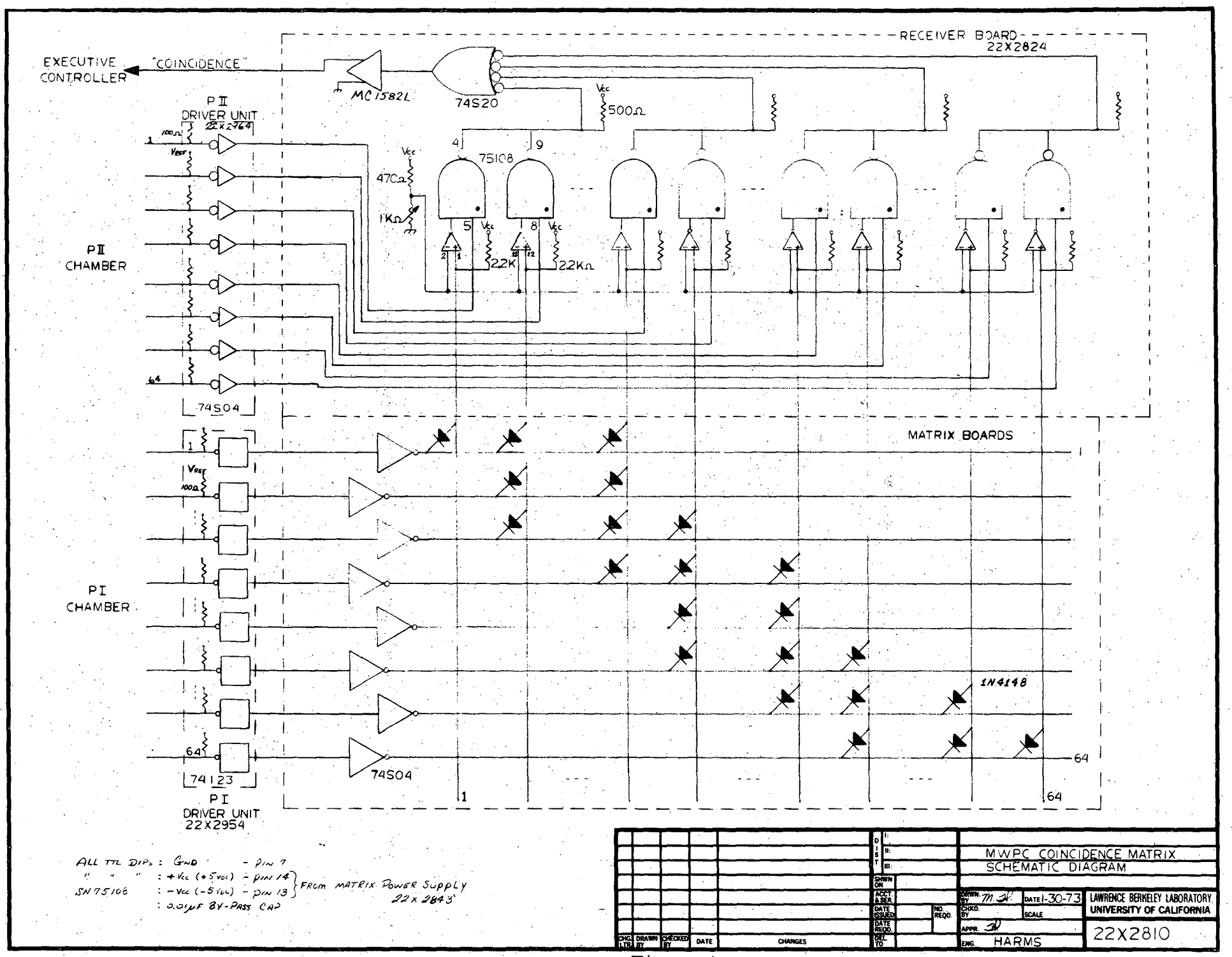
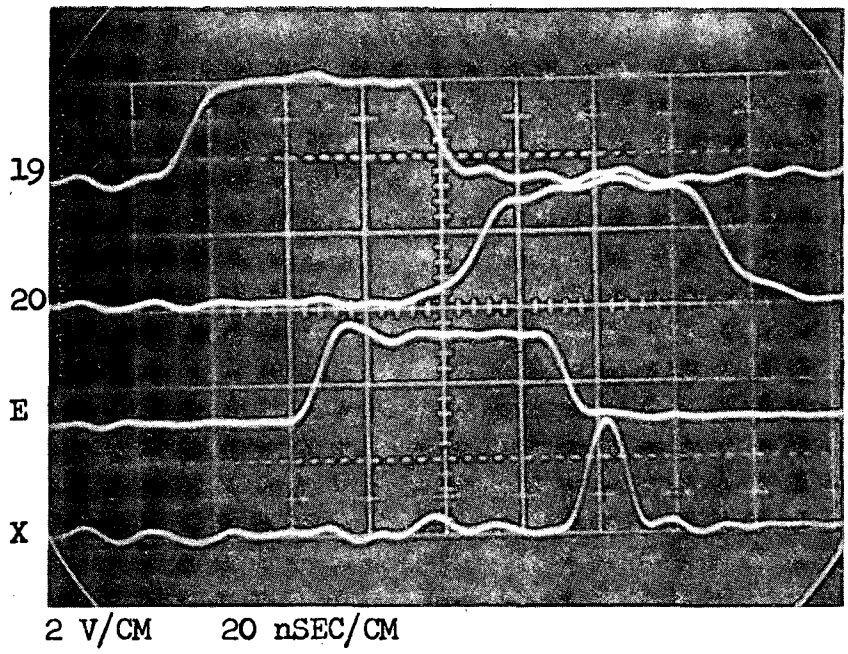


Figure 4

XBL 737-994

PROTOTYPE PHOTOGRAPHS



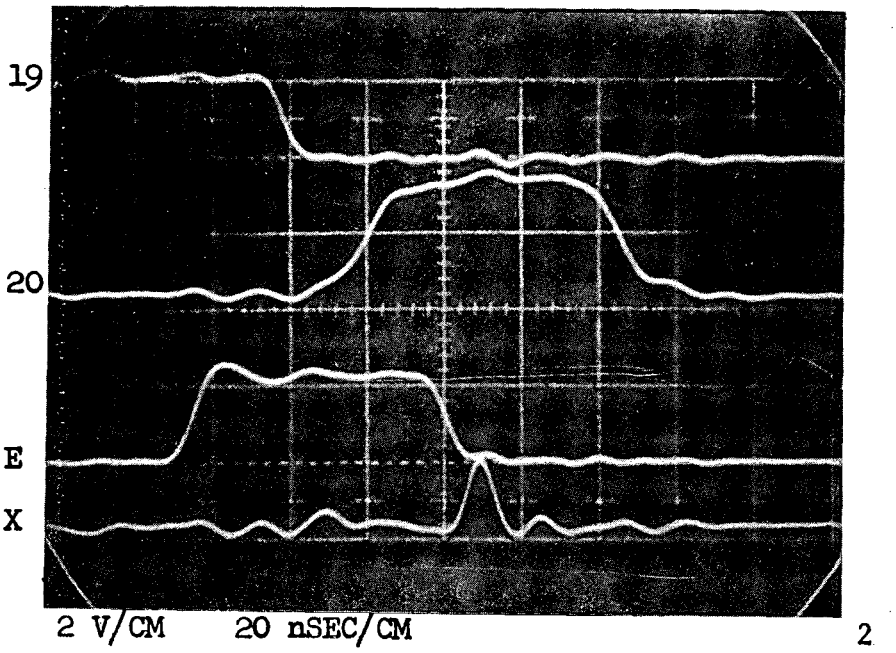
1

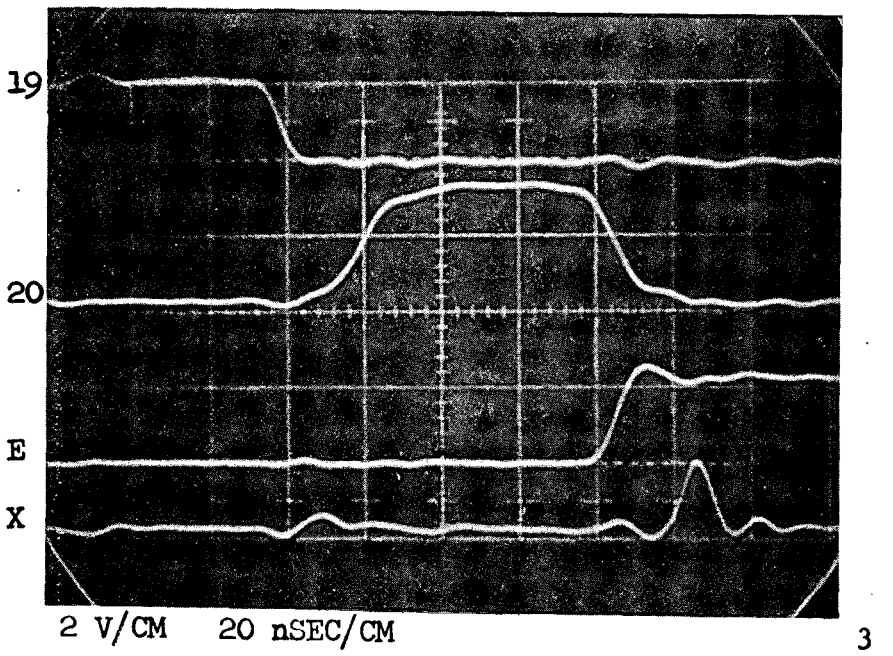
XBB 736-3546

TRACES:	18	P I signal at the function generator
	19	P I signal entering 38 feet of cable
	20	P I signal entering the matrix board
	E	P II signal entering the receiver board
	X	Final output from receiver board

Figure 5

PROTOTYPE PHOTOGRAPHS

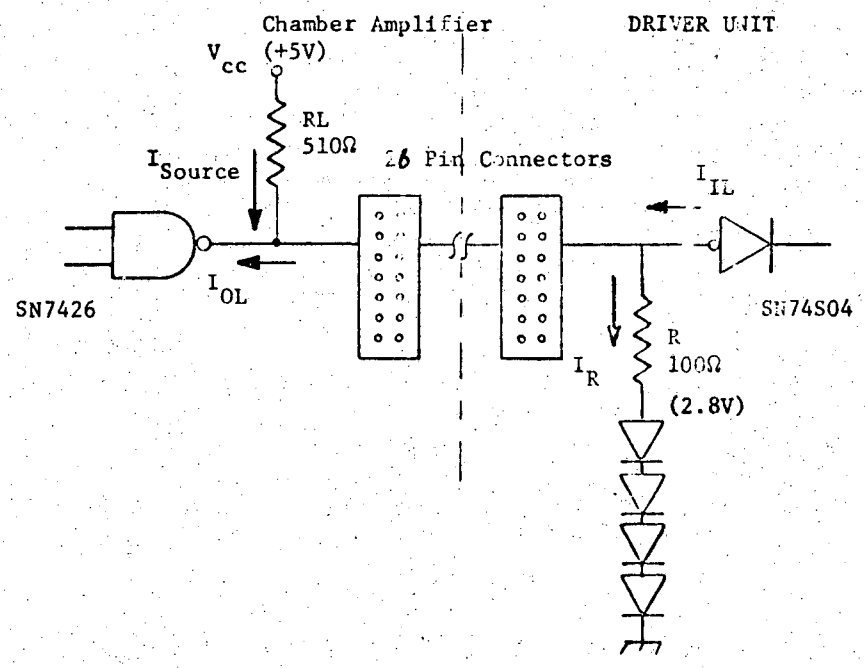




XBB 736-3545

Figure 6

LAWRENCE BERKELEY LABORATORY - UNIVERSITY OF CALIFORNIA SPECIAL PROJECTS	MWPC	FILE NO.	PAGE
SUBJECT Driver Unit Power Dissipation		NAME M. Harms DATE June 1973	



I_{IL} = 1.6 ma $\qquad V_{OL}$ = 0.4V

$$I_{Source} = \frac{V_{cc} - V_{OL}}{R_L} = \frac{5V - 0.4V}{510\Omega} = 9 \text{ ma}$$

$$I_{OL} = I_{Sink} = I_{Source} + I_{IL} = 9\text{ma} + 1.6 \text{ ma} = 11 \text{ ma}$$

(MAX I_{OL} is 16 ma)

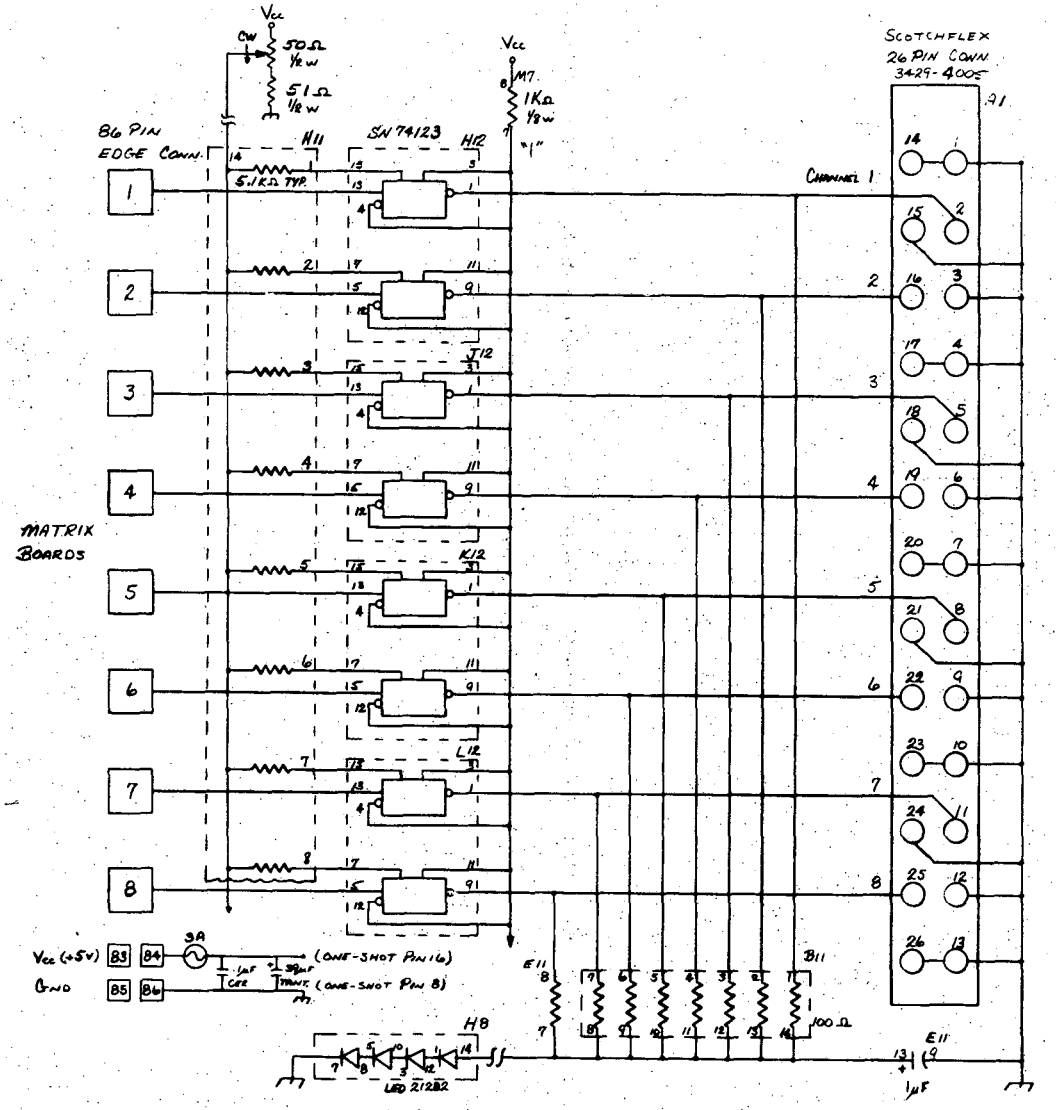
$$I_R = \frac{V_{cc} - V_{Diode}}{R} = \frac{5V - 2.8V}{100} = 22 \text{ ma}$$

$$\text{Power Dissipated} = \frac{(E_R)^2}{R} = \frac{(2.2V)^2}{(100\Omega)} = 48.5 \text{ mw per terminating resistor}$$

Power Dissipated for seven line terminating resistors = (7)(48.5 mw) = 0.338 w

(Seven terminating resistors are contained in each DIP module. Each resistor may dissipate 150 mw and the module may dissipate 1.5w of power).

Figure 6A



MWPC WIRES	INPUT CONNECTOR	TERM. RESISTOR 100Ω	ONE-SHOT INPUT 74123	CAP "1"	TIMING ONE-SHOT 74123	TIMING RESISTOR 5.1KΩ	ONE-SHOT OUTPUT 74123	86 PIN CONN.
57	12 - 2	B11 - 1	H12 - 1		H12-15	H11-1	H12-13	1
58	- 16	- 2	- 9		- 7	-2	- 5	2
59	- 6	- 3	J12 - 1	E11	J12-15	-3	J12-13	3
60	- 19	- 4	- 9	-13	- 7	-4	- 5	4
61	- 8	- 5	K12 - 1		K12-15	-5	K12-13	5
62	- 22	- 6	- 9		- 7	-6	- 5	6
63	- 11	- 7	L12 - 1	M7	L12-15	-7	L12-13	7
64	- 25	E11 - 8	- 9	-7	- 7	-8	- 5	8
49	10 - 2	D11 - 1	H10 - 1		H10-15	H11-9	H10-13	9
50	- 16	- 2	- 9		- 7	-10	- 5	10
51	- 5	- 3	J10 - 1	E11	J10-15	-11	J10-13	11
52	- 19	- 4	- 9	-6	- 7	-12	- 5	12
53	- 8	- 5	K10 - 1		K10-15	-13	K10-13	13
54	- 22	- 6	- 9		- 7	J8-1	- 5	14
55	- 11	- 7	L10 - 1	M7	L10-15	-2	L10-13	15
56	- 25	E11 - 1	- 9	-7	- 7	-3	- 5	16
41	9 - 2	B8 - 1	H9 - 1		H9-15	J8-4	H9-13	17
42	- 16	- 2	- 9		- 7	-5	- 5	18
43	- 5	- 3	J9 - 1	E8	J9-15	-9	J9-13	19
44	- 19	- 4	- 9	-13	- 7	-8	- 5	20
45	- 8	- 5	K9 - 1		K9-15	-9	K9-13	21
46	- 22	- 6	- 9		- 7	-10	- 5	22
47	- 11	- 7	L9 - 1	M7	L9-15	-11	L9-13	23
48	- 25	B9 - 8	- 9	-5	- 7		- 5	24
33	7 - 2	D8 - 1	H7 - 1		H7-15	J8-12	H7-13	25
34	- 16	- 2	- 9		- 7	-13	- 5	26
35	- 5	- 3	J7 - 1	E8	J7-15	H5-1	J7-13	27
36	- 19	- 4	- 9	-6	- 7	-2	- 5	28
37	- 8	- 5	K7 - 1		K7-15	-3	K7-13	29
38	- 22	- 6	- 9		- 7	-4	- 5	30
39	- 11	- 7	L7 - 1	M7	L7-15	-13	L7-13	31
40	- 25	B8 - 1	- 9	-5	- 7	-6	- 5	32
25	6 - 2	B5 - 1	H6 - 1		H6-15	H5-7	H6-13	33
26	- 16	- 2	- 9		- 7	-8	- 5	34
27	- 5	- 3	J6 - 1	E5	J6-15	-9	J6-13	35
28	- 19	- 4	- 9	-13	- 7	-10	- 5	36
29	- 8	- 5	K6 - 1		K6-15	-11	K6-13	37
30	- 22	- 6	- 9		- 7	-12	- 5	38
31	- 11	- 7	L6 - 1	M7	L6-15	-13	L6-13	39
32	- 25	B5 - 8	- 9	-3	- 7	J5-1	- 5	40
17	4 - 2	D5 - 1	H4 - 1		H4-15	J5-2	H4-13	41
18	- 16	- 2	- 9		- 7	-3	- 5	42
19	- 5	- 3	J4 - 1	E5	J4-15	-4	J4-13	43
20	- 19	- 4	- 9	-13	- 7	-5	- 5	44
21	- 8	- 5	K4 - 1		K4-15	-6	K4-13	45
22	- 22	- 6	- 9		- 7	-7	- 5	46
23	- 11	- 7	L4 - 1	M7	L4-15	-8	L4-13	47
24	- 25	B5 - 1	- 9	-3	- 7	-9	- 5	48
9	3 - 2	B2 - 1	H3 - 1		H3-15	J5-10	H3-13	49
10	- 16	- 2	- 9		- 7	-11	- 5	50
11	- 5	- 3	J3 - 1	E2	J3-15	-12	J3-13	51
12	- 19	- 4	- 9	-13	- 7	-13	- 5	52
13	- 8	- 5	K3 - 1		K3-15	H2-1	K3-13	53
14	- 22	- 6	- 9		- 7	-2	- 5	54
15	- 11	- 7	L3 - 1	M7	L3-15	-3	L3-13	55
16	- 25	B2 - 8	- 9	-1	- 7	-4	- 5	56
1	1 - 2	D2 - 1	H1 - 1		H1-15	H2-5	H1-13	57
2	- 16	- 2	- 9		- 7	-6	- 5	58
3	- 5	- 3	J1 - 1	E2	J1-15	-7	J1-13	59
4	- 19	- 4	- 9	-13	- 7	-8	- 5	60
5	- 8	- 5	K1 - 1		K1-15	-9	K1-13	61
6	- 22	- 6	- 9		- 7	-10	- 5	62
7	- 11	- 7	L1 - 1	M7	L1-15	-11	L1-13	63
8	- 25	B2 - 1	- 9	-1	- 7	-12	- 5	64

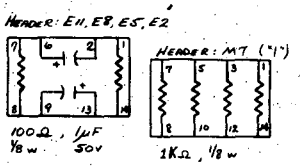
BOARD CONTAINS 8 SECTIONS IDENTICAL TO THE ONE ABOVE.

INPUT IS TO FLAT CABLE CONNECTOR.

OUTPUT IS FROM 86 PIN EDGE CONNECTOR.

ONE-SHOTS ARE BY-PASSED WITH A 0.01μF CAP.

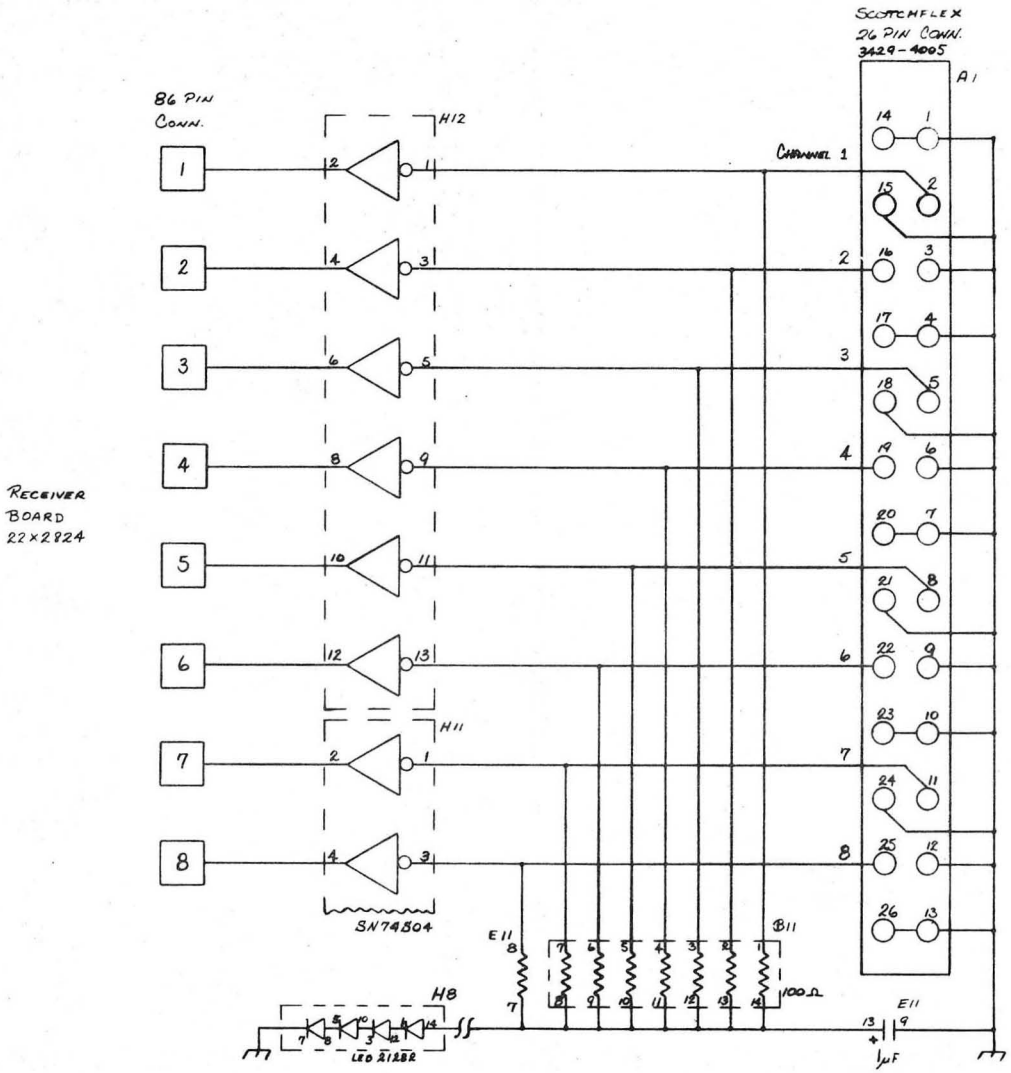
DIODES AND TIMING POT RESISTOR ARRANGEMENT ARE COMMON TO ALL 8 SECTIONS.



						MWPC COINCIDENCE MATRIX DRIVER UNIT PI	
					DRAWN BY	DATE 5-14-73	LAWRENCE BERKELEY LABORATORY UNIVERSITY OF CALIFORNIA
					CHKD. BY	SCALE	
					APPR.		22X2954
CHKD. LTR.	DRAWN BY	CHECKED BY	DATE	CHANGES	ENG. HARMS		

Figure 6b

XBL 737-999



MWPC WIRES	INPUT CONNECTOR	TERMINATING RESISTOR 100Ω	INVERTER INPUT 74804	INVERTER OUTPUT 74804	OUTPUT CONNECTOR	CAP μF
57	12 - 2	B11 - 1	H12 - 1	H12 - 2	1	
58	- 16	- 2	- 3	- 4	2	
59	- 5	- 3	- 5	- 6	3	E11
60	- 19	- 4	- 9	- 8	4	-13
61	- 8	- 5	- 11	- 10	5	
62	- 22	- 6	- 13	- 12	6	
63	- 11	- 7	H11 - 1	H11 - 2	7	
64	- 25	E11 - 8	- 3	- 4	8	
49	10 - 2	D11 - 1	H10 - 1	H10 - 2	9	
50	- 16	- 2	- 3	- 4	10	
51	- 5	- 3	- 5	- 6	11	E11
52	- 19	- 4	- 9	- 8	12	-6
53	- 8	- 5	- 11	- 10	13	
54	- 22	- 6	- 13	- 12	14	
55	- 11	- 7	H11 - 5	H11 - 6	15	
56	- 25	E11 - 1	- 9	- 8	16	
41	9 - 2	B8 - 1	H9 - 1	H9 - 2	17	
42	- 16	- 2	- 3	- 4	18	
43	- 5	- 3	- 5	- 6	19	E8
44	- 19	- 4	- 9	- 8	20	-13
45	- 8	- 5	- 11	- 10	21	
46	- 22	- 6	- 13	- 12	22	
47	- 11	- 7	H11 - 11	H11 - 10	23	
48	- 25	E8 - 8	- 13	- 12	24	
33	7 - 2	D8 - 1	H7 - 1	H7 - 2	25	
34	- 16	- 2	- 3	- 4	26	
35	- 5	- 3	- 5	- 6	27	E8
36	- 19	- 4	- 9	- 8	28	-6
37	- 8	- 5	- 11	- 10	29	
38	- 22	- 6	- 13	- 12	30	
39	- 11	- 7	H5 - 1	H5 - 2	31	
40	- 25	E8 - 1	- 3	- 4	32	
25	6 - 2	B5 - 1	H6 - 1	H6 - 2	33	
26	- 16	- 2	- 3	- 4	34	
27	- 5	- 3	- 5	- 6	35	E5
28	- 19	- 4	- 9	- 8	36	-13
29	- 8	- 5	- 11	- 10	37	
30	- 22	- 6	- 13	- 12	38	
31	- 11	- 7	H5 - 5	H5 - 6	39	
32	- 25	E5 - 8	- 9	- 8	40	
17	4 - 2	D5 - 1	H4 - 1	H4 - 2	41	
18	- 16	- 2	- 3	- 4	42	
19	- 5	- 3	- 5	- 6	43	E5
20	- 19	- 4	- 9	- 8	44	-6
21	- 8	- 5	- 11	- 10	45	
22	- 22	- 6	- 13	- 12	46	
23	- 11	- 7	H5 - 11	H5 - 10	47	
24	- 25	E5 - 1	- 13	- 12	48	
9	3 - 2	B2 - 1	H3 - 1	H3 - 2	49	
10	- 16	- 2	- 3	- 4	50	
11	- 5	- 3	- 5	- 6	51	E2
12	- 19	- 4	- 9	- 8	52	-13
13	- 8	- 5	- 11	- 10	53	
14	- 22	- 6	- 13	- 12	54	
15	- 11	- 7	H2 - 1	H2 - 2	55	
16	- 25	E2 - 8	- 3	- 4	56	
1	1 - 2	D2 - 1	H1 - 1	H1 - 2	57	
2	- 16	- 2	- 3	- 4	58	
3	- 5	- 3	- 5	- 6	59	E2
4	- 19	- 4	- 9	- 8	60	-6
5	- 8	- 5	- 11	- 10	61	
6	- 22	- 6	- 13	- 12	62	
7	- 11	- 7	H2 - 5	H2 - 6	63	
8	- 25	E2 - 1	- 9	- 8	64	

BOARD CONTAINS 8 SECTIONS IDENTICAL TO THE ONE ABOVE.

INPUT IS TO FLAT CABLE CONNECTOR

OUTPUT IS FROM 86 PIN EDGE CONNECTOR.

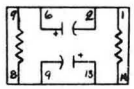
DIODES ARE COMMON TO ALL 8 SECTIONS.

ALL INVERTERS ARE BY-PASSED WITH A 0.01μF CAP.

V_{cc} (+5V) 85 84 2A .1μF CER. 39μF TANT. to INVERTER pin 14

GND 85 86 to INVERTER pin 7

HEADER: E11, E8, E5, E2



100 Ω, 1/8 W

1μF, 50V

CHG. ULTR.	DRAWN BY	CHECKED BY	DATE	CHANGES

DIST I: II: III:

SHWN ON | ACCT. & BER. | DATE REQUIRED | DATE RECEIVED | REL TO | NO. REQD.

MWPC COINCIDENCE MATRIX
DRIVER UNIT PII

DRAWN BY | CHKD. BY | APPR. | ENG. HARMS | DATE 4-25-73 | SCALE

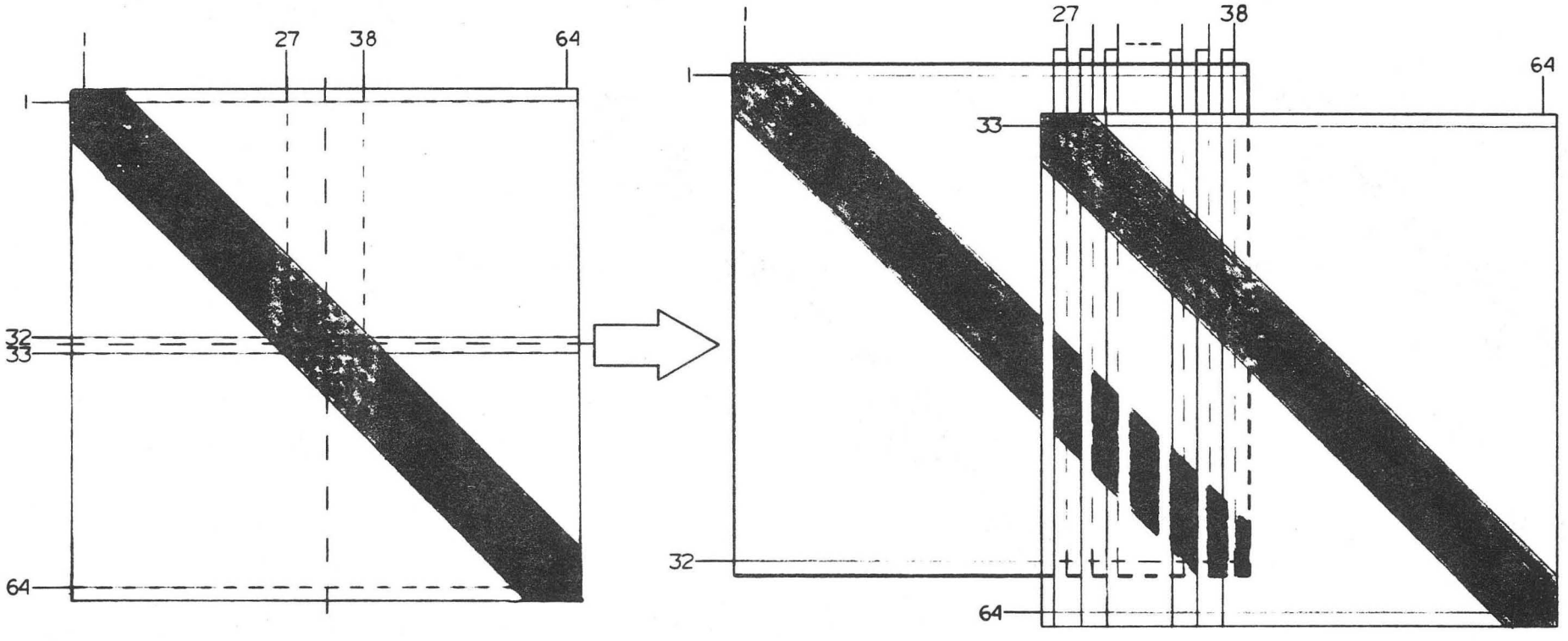
LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA

22X2964

BL-2009-3(REV.12-71)

Figure 6c

XBL 737-996



ENGINEERING SKETCH —
MWPC COINCIDENCE MATRIX
DUAL MATRIX BOARDS
DRAWN BY M.L. DATE 1-31-73
LAWRENCE RADIATION LABORATORY
UNIVERSITY OF CALIFORNIA
BERKELEY
CHKD. BY SCALE
APPR. L.
ENGR. HARMS
22X2800

Figure 7

XBL 737-998

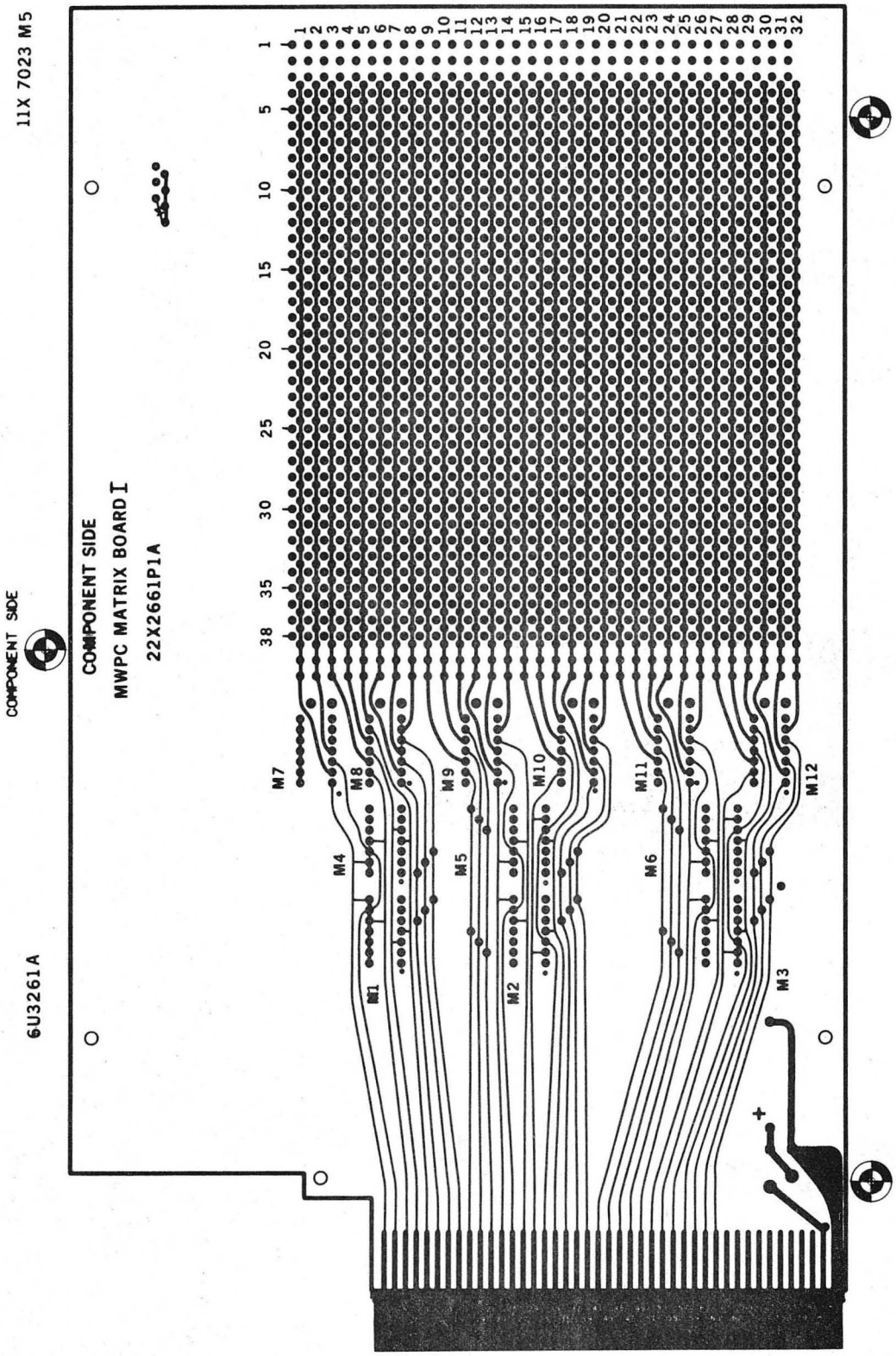

11X 7023 M5
COMPONENT SIDE
6U3261A
COMPONENT SIDE
MWPC MATRIX BOARD I
22X2661P1A
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
+

Figure 8A

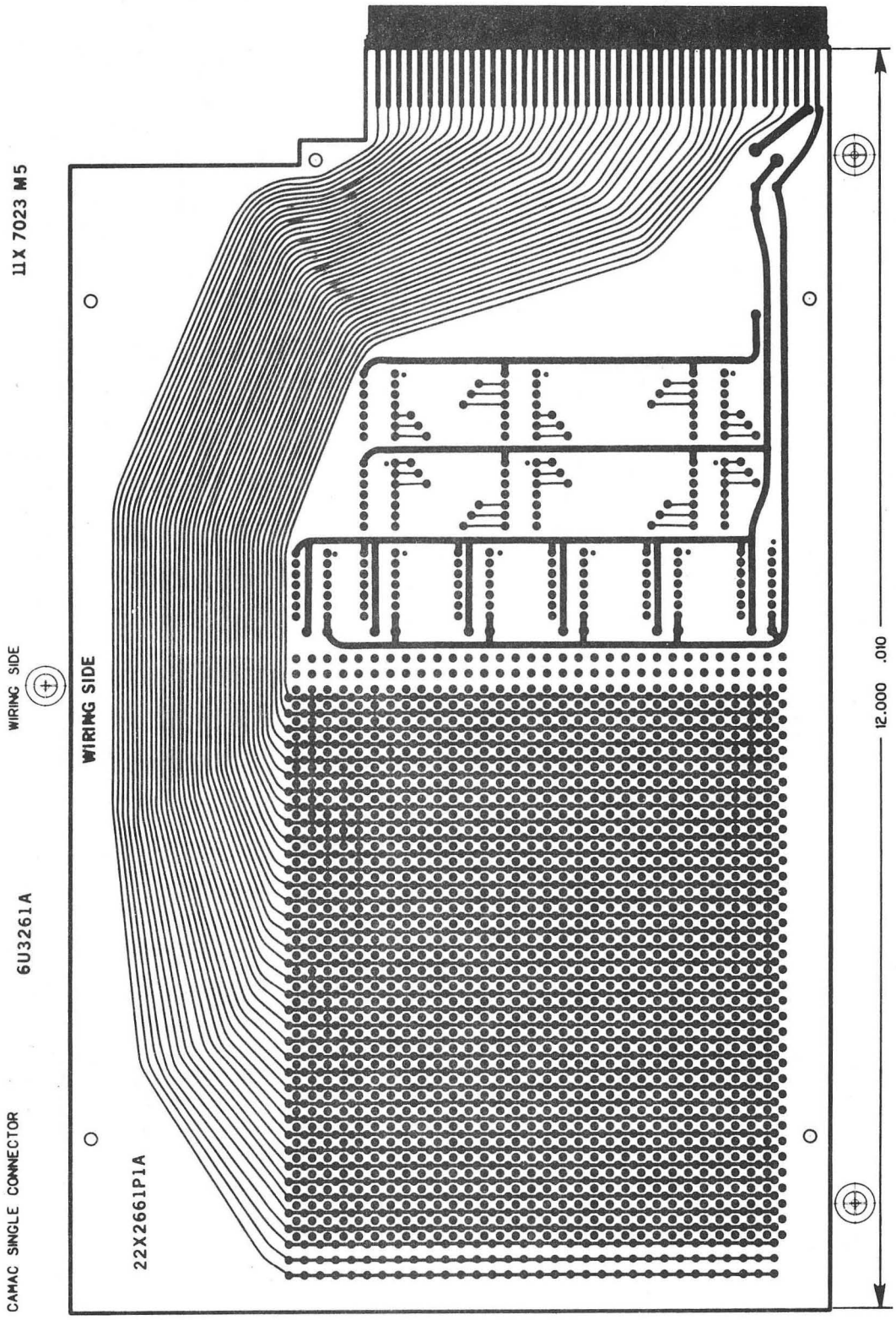

CAMAC SINGLE CONNECTOR
6U3261A
WIRING SIDE
11X 7023 M5
22X2661P1A
WIRING SIDE
12.000 .010

Figure 8 B

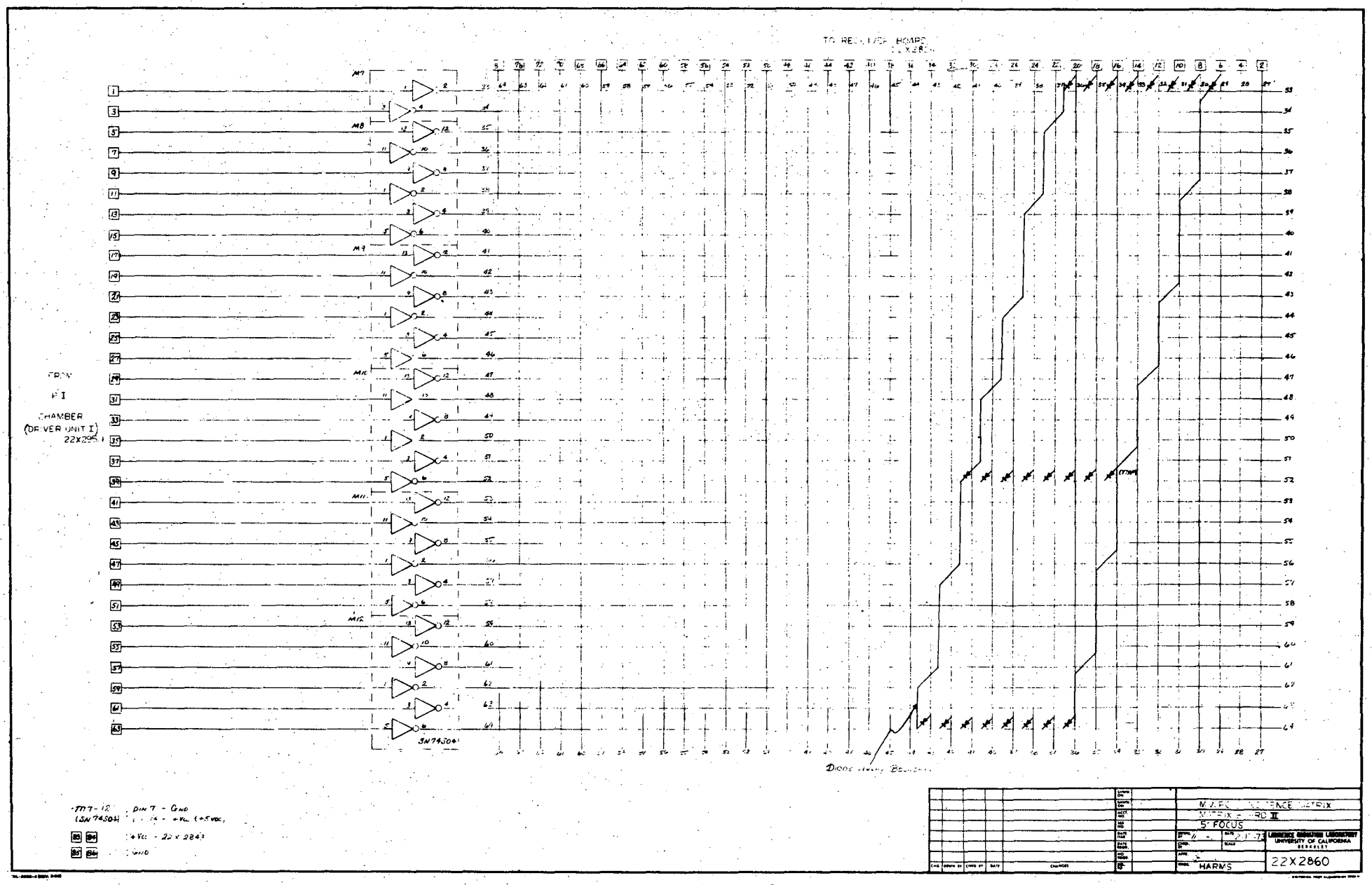


Figure 9a

XBL 737-1003

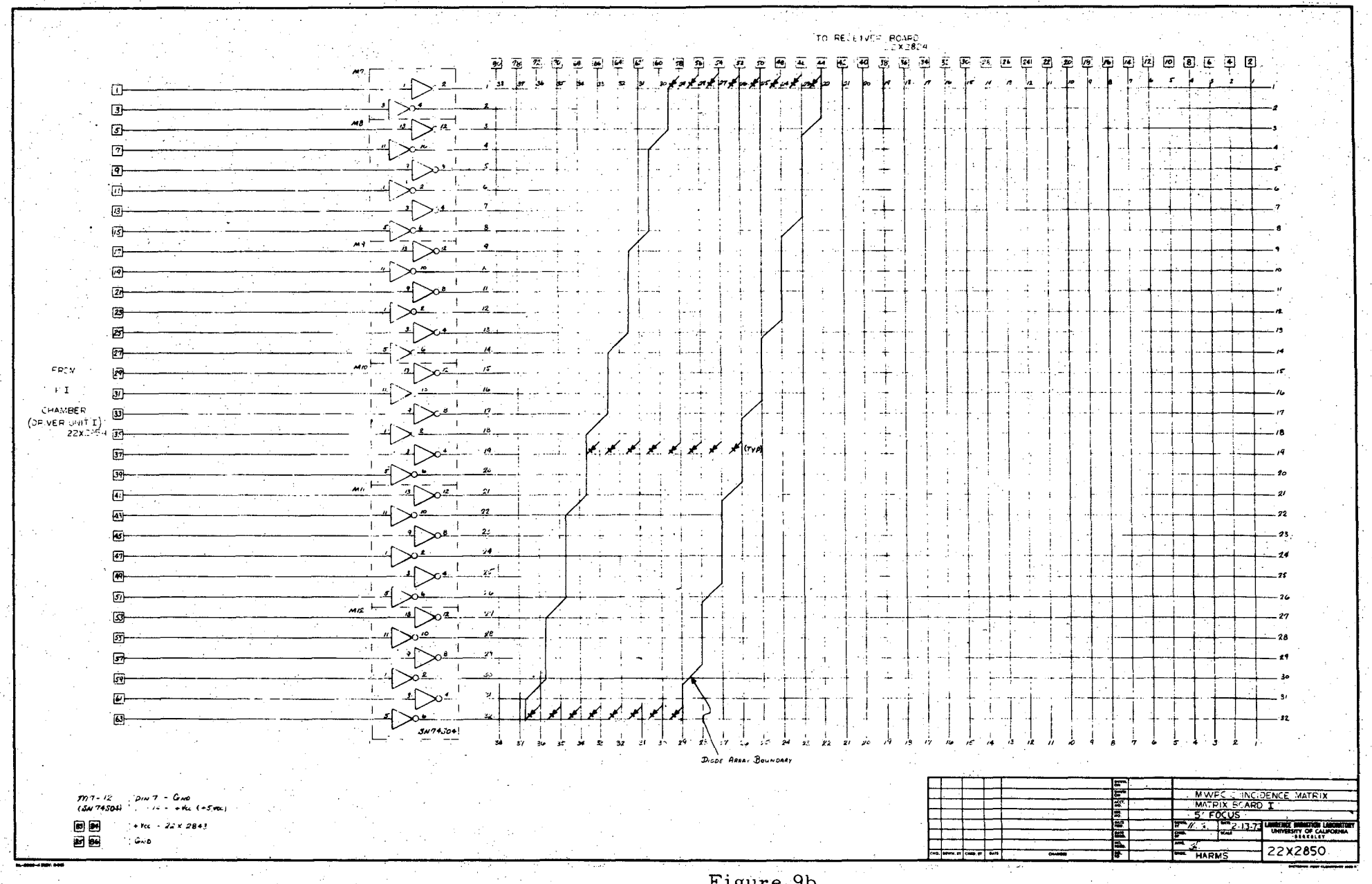


Figure 9b

XBL 737-1004

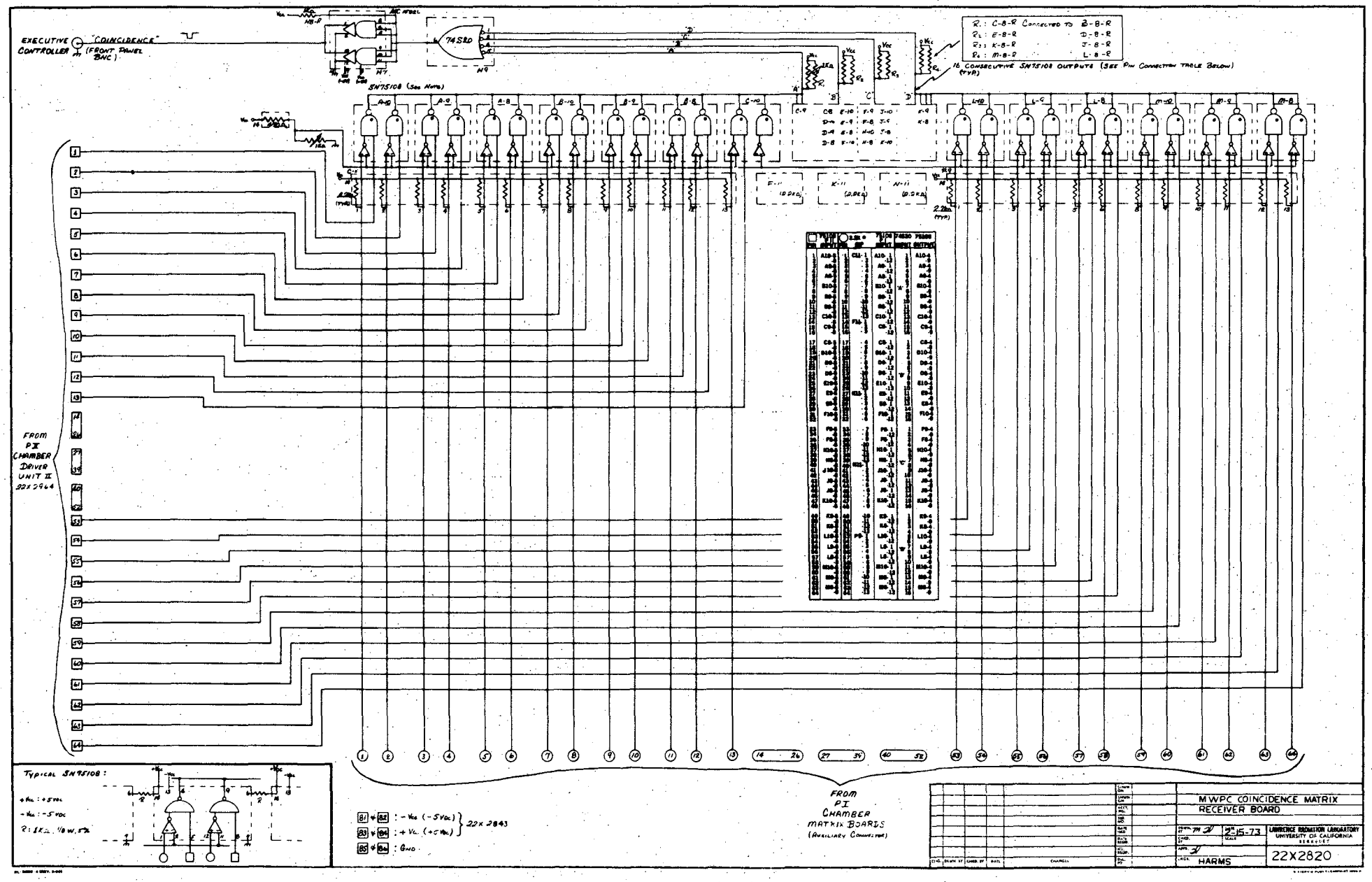
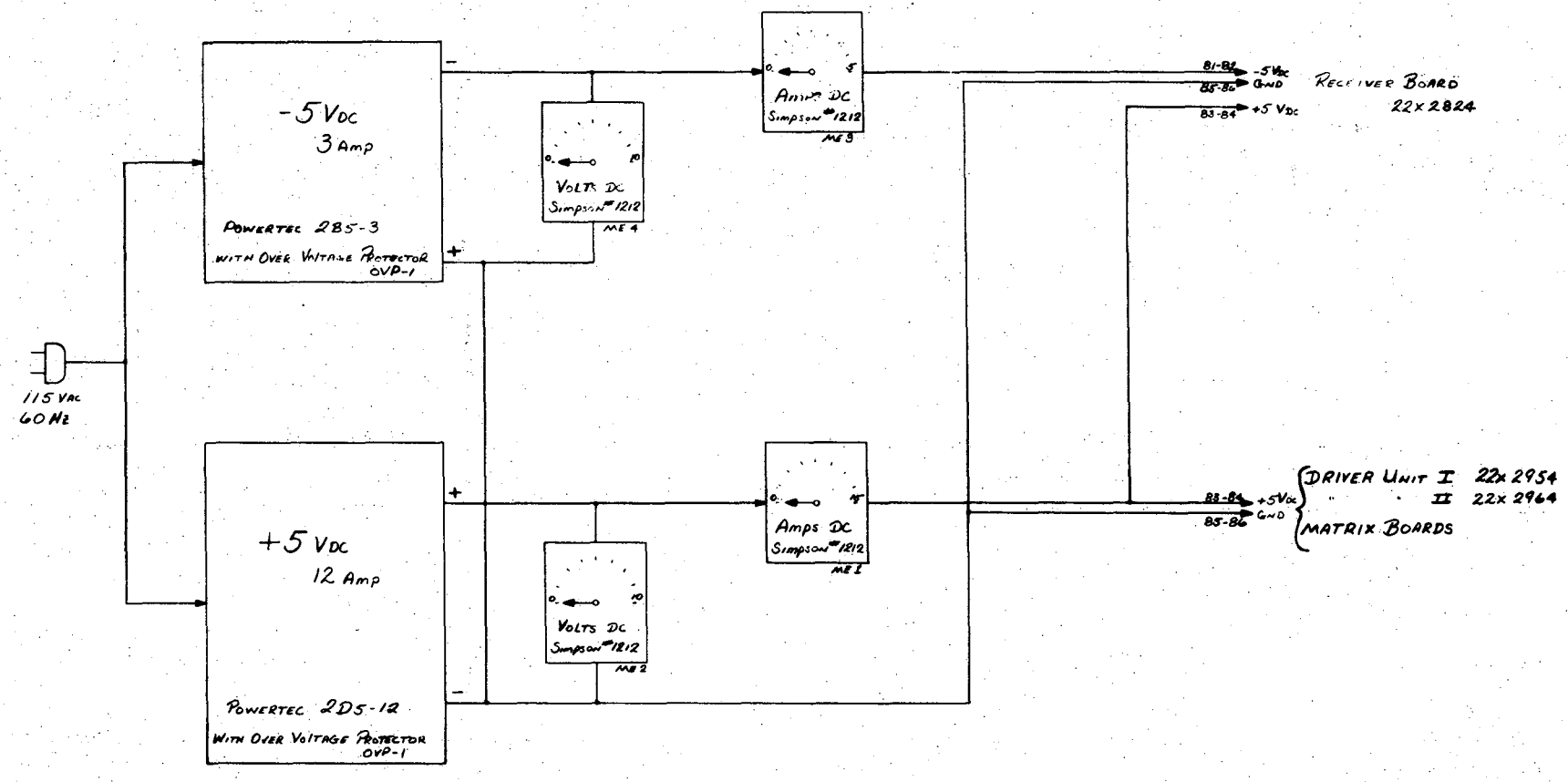


Figure 10

XBL 737-1002



							MWPC COINCIDENCE MATRIX
							MATRIX POWER SUPPLY
						DRAWN BY	DATE 3-9-73
						CHKD. BY	SCALE
						APPR.	
CHKD. DATE	DRAWN BY	CHECKED BY	DATE	CHANGES		ENG. HARMS	

LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA

22X2840

Figure 11

XBL 737-1000

TABLE 1

LAWRENCE RADIATION LABORATORY - UNIVERSITY OF CALIFORNIA
COST ESTIMATE

FILE NO.

PAGE 1 of 1

PROJECT: MWPC Coincidence Matrix

NAME: M. Harms

DATE: 10 May 1973

SUBJECT: Hardware Cost Estimate	ENG. & DESIGN $	DETAIL & DRAFT $	TECH. $	SHOP & FAB. $	INSTALL $	MAT'L. $
DRIVER UNIT BOARDS (4)						
Insert, solder sockets 16 hrs @ $12 ea			192			
Wire-wrap (1600 wires) 32 hrs @ $12 ea				384		
Inverters 22 @ $1.65 ea						36
One-shots 64 @ $3.80 ea						242
Resistors 32 @ $1.50 ea						48
DIP sockets 150 @ .65 ea						98
Cable connectors 32 @ $2.00 ea						64
CAMAC boards 4 @ $20.00 ea						80
CAMAC hardware 4 @ $10.00 ea						40
TOTAL FOR DRIVER UNIT = $1,184						
MATRIX BOARDS (20)						
Artwork design 30 hrs @ $12 ea	360					
Diode insertion (done by experimenter)						
Artwork fabrication (20 bds)(1 hr/bd) @ $12 ea				240		
Wave soldering 10 hrs @ $12 ea				120		
Diodes 3600 @ .03 ea						108
Inverters (6/bd)(20 bds) @ $1.65 ea						198
CAMAC boards 20 @ $5.00 ea						100
CAMAC hardward 20 @ $10.00 ea						200
TOTAL FOR MATRIX BOARDS = $1,326						
RECEIVER BOARDS (2)						
Insert, solder sockets 24 hrs @ $12 ea			288			
Wire-wrap (680 wires) 12 hrs @ $12 ea				144		
NANDs 2 @ $1.50 ea						3
Receivers 64 @ $3.00 ea						192
Capacitors 68 @ .29 ea						20
Resistors 10 @ $1.50 ea						15
Line drivers 2 @ $2.00 ea						4
DIP sockets 78 @ .65 ea						51
CAMAC boards 2 @ $20.00 ea						40
CAMAC hardware 2 @ $10.00 ea						20
TOTAL FOR RECEIVER BOARDS = $777						
OTHER HARDWARE						
CAMAC crate						210
Power supplies						100
Contingency 15% total						540
TOTAL HARDWARE COST = $4,137						

RL-3396

LEGAL NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Atomic Energy Commission, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

TECHNICAL INFORMATION DIVISION
LAWRENCE BERKELEY LABORATORY
UNIVERSITY OF CALIFORNIA
BERKELEY, CALIFORNIA 94720