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# Schottky barrier degradation of the W/GaAs system after high temperature annealing

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## Abstract

W/GaAs diodes annealed at temperatures ranging from 100°C to 900°C were investigated with current voltage (I-V) and capacitance voltage (C-V) techniques, Rutherford backscattering spectrometry (RBS), scanning electron microscopy (SEM), and transmission electron microscopy (TEM). Improvements in the diode characteristics were observed after annealing at temperatures below 600°C. Noticeable degradation in the rectifying behavior of the diodes occurred after annealing at temperatures > 600°C. Correlations between the electrical degradation and the interdiffusion of W and GaAs at the interface were found. Our results strongly suggest that the in-diffusion of W leads to the formation of a diffused, highly resistive region near the W/GaAs interface. The high resistance of this region is believed to be caused by the compensation of the substrate dopants by tungsten acceptors. Annealing the diodes at temperatures > 850°C resulted in reactions between W and GaAs. The W-GaAs reaction leads to islands of $W_2As_3$ at the W/GaAs interface resulting in physical breakdown of the W/GaAs diode.

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## I. INTRODUCTION

Recently, the fabrication of a high-speed metal GaAs field effect transistor (MESFET) using the self-aligned gate (SAG) technique has been proposed [1]. In the SAG process, the gate is used as an implantation mask for the formation of the source and drain regions. Implantation is followed by a high-temperature annealing step (> 850°C). This requires thermally stable (up to 850°C) and reproducible GaAs Schottky contacts.

Refractory metals, especially W have been shown to form thermally stable Schottky contacts to n-GaAs up to annealing temperatures of 600°C [2-4]. Deviations from ideal Schottky behavior were observed for the W/GaAs diode after annealing at temperatures > 650°C. Extremely high thermal stabilty (up to 950°C) for the W/GaAs diode was also reported by Matsumoto et al [5]. After annealing at 950°C in an As overpressure, Matsumoto et al observed significant interdiffusion of W and GaAs at the interface. However, the electrical behavior of the diode did not deviate from ideal diode characteristics ($\phi_b \sim$ 0.7 eV and $n \sim 1.2$).

Successful SAG GaAs MESFETs have been fabricated with Ti/W [1], Ti/W silicide [6] and Ta silicide [7] as gate materials. WN/GaAs also showed good thermal stability for annealing at 800°C [9]. The thermal stability of TiN [10] and $MoSi_2$ [11] contacts to GaAs has also been investigated, but they were found to be unstable contacts for annealing temperatures higher than 700°C and 500°C, respectively. The degradation of these contacts at high temperatures was believed to be connected to the interdiffusion of GaAs and the contact materials at the interface [8,11]. This explanation, however, does not seem to be applicable to the W/GaAs contact studied by Matsumoto et al. The excellent electrical behavior of the W/GaAs diode after annealing at 950°C observed by Matsumoto et al might be the result of the formation of a uniform layer of

a W-GaAs intermetallic compound at the W/GaAs interface. The formation of such a layer at the interface is possibly due to the As overpressure which is much more effective than the oxide capping technique commonly used to prevent As loss during high temperature annealing.

In order to select better gate materials for GaAs for the SAG process in the future, the high temperature degradation mechanisms for metal-GaAs Schottky diodes must be clearly understood. In this paper, the electrical and structural properties of the W/GaAs diode after annealing with oxide capping at temperatures ranging from 100°C to 900°C are investigated. The emphasis of this study is on the high temperature (> 700°C) degradation mechanisms of the diode. Electrical measurements were performed with current voltage (I-V) and capacitance voltage (C-V) techniques. Analytical techniques including Rutherford backscattering spectrometry (RBS), scanning electron microscopy (SEM), and transmission electron microscopy (TEM) were used to characterize the structural properties of the diodes. A possible model derived from the experimental results for the degradation of the diode after high temperature annealing will be discussed.

## II. EXPERIMENTAL

Undoped semi-insulating ($\rho > 10^7$ Ω-cm) and Te-doped ($n \sim 10^{17}/cm^3$; $\rho \sim 10^{-2}$ Ω-cm) <100> GaAs wafers were degreased and etched with a solution of $H_2SO_4$:$H_2O_2$:$H_2O$ (5:1:1) for 1 min. The n-type GaAs wafer was patterned with a standard lithographic technique. Dots of sizes ranging from 0.2 mm to 1 mm in diameter were exposed for metallization. Prior to W deposition, the patterned n-type GaAs wafer was cleaned with a solution of $NH_4OH$:$H_2O_2$:$H_2O$ (1:1:100) for 1 min followed by a 1 min etch in 50% HCl solution for native oxide removal. The undoped wafer was etched in 50% HCl solution before W deposition.

W was sputtered onto the GaAs substrate in a Perkin-Elmer Randex sputtering system* at an Ar pressure of ~ 15 mtorr. W dots of thickness ~ 1800 Å were defined on the n-GaAs substrate using the standard lift-off technique for electrical measurements. A thin layer (~ 180 Å) of W was deposited on the undoped GaAs substrate for RBS and TEM measurements. The metallized wafers were then cut into small pieces and capped on both sides with ~ 2000 Å of $SiO_2$ by sputtering. Annealing was carried out in the temperature range of 100 - 900°C for various time durations in a flowing $N_2$ ambient. Au-Ge alloy ohmic contacts were formed on the back side of the diodes by e-gun evaporation of Ge-doped Au followed by brief annealing at 425°C after the removal of the $SiO_2$ cap.

Current-voltage measurements were performed with a HP 4140B* current meter with a built-in DC voltage source. Ideal I-V characteristics are represented by the following equation:

$$J = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \cdot \left[\exp\left(\frac{qV_a}{nkT}\right) - 1\right]$$

where J is the current density, A* is the Richardson constant (taken to be ~ 8.6 $A/cm^2/K^2$ [12] in this work), T is the temperature in K, k is the Boltzmann constant, $V_a$ is the applied voltage, $q\phi_b$ is the Schottky Barrier height of the diode, and n is the ideality factor which is ≈ 1 if the thermionic emission process dominates. The capacitance-voltage measurments (C-V) were carried out with a HP 4192A impedance analyzer*. Dopant concentration profiles of the GaAs substrates and the Schottky barrier heights of the diodes can be obtained by plotting the $1/C^2$ versus reverse bias voltage $V_R$. The dopant concentration $N_d$ at the edge of the depletion region $x_d$ under an applied dc voltage $V_R$, can be expressed as

$$N_d(x_d) = \frac{-2}{q\epsilon\epsilon_o A^2 [d(1/C^2)/dV_R]}$$

where A is the diode area and $\varepsilon$ is the relative dielectric constant of the substrate material.

Rutherford backscattering spectrometry (RBS) measurements were performed with a 2.0 MeV $^4He^+$ beam generated by a 2.5 MeV Van de Graaff accelerator. The beam was focused down to 0.75 mm in diameter on target. Energy resolution of ~ 18 keV (FWHM) was obtained with a Si surface barrier detector located at a backscattering angle of 170°. The samples were mounted on a goniometer and were tilted at 65° with respect to the normal axis of the sample surface so that depth resolution of ~ 20 Å for W could be achieved. Transmission electron microscopy and scanning electron microscopy were carried out with a Siemens 102 TEM* and Hitachi S310 SEM*, respectively.

## III. RESULTS

### 1. Rutherford Backscattering Spectrometry (RBS) Measurements

RBS spectra for samples of W/GaAs as-deposited and annealed at 650°C, 750°C, 800°C, 900°C are shown in Fig. 1. Below 650°C no change can be detected in the RBS spectra. At annealing temperatures between 650°C and 800°C, interdiffusion of W and GaAs was observed. The W diffusion profiles in GaAs at various temperatures, as measured by RBS, are shown in Fig. 2. Note that after annealing at 800°C for 20 min, there was ~ 0.2 at .% ($8 \times 10^{19}$ $cm^{-3}$) of W present at 600 Å below the W/GaAs interface. The distribution profiles of W in GaAs shown in Fig. 2 are of the form $C(x) = C_0 \exp(-x/\delta)$. For such a plot a characteristic distance $\delta$ can be defined and is determined from the inverse slope of the plot. A plot of $\delta$ vs $\sqrt{\text{time}}$ for samples annealed at 700°C is shown in Fig. 3. The linear relationship in Fig. 3 confirmed that it was a diffusion process with $\delta = 2(Dt)^{1/2}$ where D is the diffusion constant of the diffusing

species. From values of D obtained in this way, an Arrhenius plot of ln (D) vs 1/T was obtained and is shown in Fig. 4. From the slope and intercept of the curve in Fig. 4 and following the equation for diffusion $D = D_0 \exp[-\Delta E/kT]$, the activation energy of W diffusion in GaAs is found to be $\Delta E = 1.87 \pm 0.65$ eV with the prefactor $D_0 = 7.3 \times 10^{-7} cm^2/sec$. GaAs outdiffusion was also noted from the spectra at annealing temperatures between 650°C and 800°C. It is obvious that As diffuses into the W overlayer. However, corresponding Ga outdiffusion cannot be identified by the RBS measurements due to overlapping of the Ga and As backscattering signals in the RBS spectra. Possible reactions between W and GaAs were observed for diodes annealed at temperatures > 850°C. Atomic compositions of the reaction products cannot be determined by RBS because of the non-abrupt nature of the backscattering spectra.

RBS spectra from the thick W layer (1800 Å) on GaAs as-deposited and annealed at 900°C are shown in Fig. 5. No change was observed for the outer 1500 Å of W. Reactions between W and GaAs were confined to the ~ 300 Å of W at the interface.

2. Electron Microscopy Measurements

Figure 6 shows a series of scanning electron micrographs for samples as-deposited and annealed at 300°C, 700°C and 900°C. A morphologically smooth W film on the GaAs substrate is observed in the sample annealed at 300°C. After 700°C annealing, the edge between the W film and the GaAs substrate starts to form voids indicating that the W/GaAs interface is becoming "rough". Annealing at 900°C results in more voids at the interface and a non-uniform W film with holes appearing at the W surface.

Transmission electron diffraction patterns for thin (~ 180 Å) W layers on GaAs as-deposited and annealed at 750°C and 900°C with their corresponding

bright field images are shown in Fig. 7. The as-deposited film shows fine grain size ~ 70 Å. From the diffraction pattern, this fine-grained layer was identified as the β-W phase with A-15 crystal structure [13]. However, the 100 and 110 diffraction rings which are kinematically forbidden in a perfect A-15 structure were faintly visible in the diffraction pattern. This suggests that the sputtered W film may contain defects (vacancies, interstitials or impurities) at high concentrations. After annealing at 750°C for 20 min, the film transformed into b.c.c. α-W with large grain size (~ 900 Å). The electron diffraction pattern of this sample indicates that a small amount of $W_2As_3$ was present. Small voids also appeared at the grain boundaries covering ~ 1% of the total surface.

Micrographs for samples annealed at 900°C for 20 min show that the W film balled up and formed spherical grains of ~ 1000 Å in diameter on the GaAs substrate. About 60% of the GaAs surface was exposed. Diffraction patterns of the individual grain indicated that these islands formed were single grains of $W_2As_3$ with a monoclinic structure. Since a diffraction data file for other W-Ga or W-Ga-As phases is not available for comparison, the presence of these phases as reaction products cannot be ruled out. The electron diffraction data for the samples as-deposited and annealed at 750°C and 900°C are shown in Table I. X-ray diffraction data for the α-W, β-W and $W_2As_3$ phases taken from the JCPDS powder diffraction file are also shown in the table.

3. Electrical Measurements

Figure 8 shows the forward and the reverse I-V characteristics of the W/GaAs diodes after annealing at various temperatures up to 900°C. The Schottky barrier heights $\phi_b$ were obtained by extrapolating the linear portion of a curve to intercept the current axis. The ideality factor n is obtained from

the slope of the linear portion of a curve. Figure 9 shows the $\phi_b$ and n calculated from Fig. 8 for diodes annealed at various temperatures. After annealing at temperatures between 300 and 500°C, the reverse leakage currents of the diode decrease by an order of magnitude. Figure 10 shows a plot of the leakage currents at a reverse bias of 0.4 V versus the annealing temperature. The forward current also shows very good linearity with n ~ 1.05 (n ~ 1.1 for as-deposited diodes) in this temperature range. These values of n and the low reverse leakage currents indicated that diodes annealed at temperatures between 300°C and 500°C have close to ideal characteristics.

Degradation of the diodes is noticeable from the I-V curves after annealing at 600°C and higher temperatures. The ideality factor increased to 1.14 and the reverse leakage current increases by an order of magnitude compared to the 300°C annealed diode. After 700°C annealing, n becomes much larger than 1 (~ 1.34) indicating that the diode deviates substantially from the ideal thermionic model. Higher temperature annealing at 800 and 900°C resulted in ohmic-like behavior with comparable forward and reverse currents and n > 2. The thermionic emission model can no longer be applied to the I-V characteristics of these structures. This is not surprising in view of our microscopy and RBS results reported in the preceding sections.

Figure 11(a) shows $1/C^2$ versus reverse bias voltage $V_R$ for the W/GaAs diodes for different annealing conditions. The dopant concentration profiles of the diodes calculated from these curves are shown in Fig. 11 (b). Relatively uniform dopant concentrations are observed for diodes annealed below 700°C ($N \sim 3 \times 10^{17}$ $cm^{-3}$).

## IV. DISCUSSIONS

### 1. Electrical Behavior of the W/GaAs Diodes Under Low Temperature Annealing ($T < 600^\circ C$)

Significant improvements on the diode characteristics in terms of n, $\phi_b$ and the leakage current were noted for diodes annealed between 300°C and 500°C. Diodes annealed in this temperature range closely followed the thermionic emission model and showed ideal rectifying characteristics. This is in close agreement with the result of Waldrop [3] who found that diodes with W evaporated on clean GaAs surface as well as GaAs surface covered with ~ 10 Å native oxides have nearly ideal behavior in the temperature range of 350 - 450°C. This can be explained by the annealing out of defects due to native oxide and surface states at the interface resulting in a sharp W/GaAs interface. The SEM images suggest that the W films are more adherent to GaAs after annealing at low temperature (< 600°C). Previous X-ray diffraction experiments on W films [14] further showed that the transformation from β-W to α-W occurred at a temperature of ~ 300°C. However, the contribution of this phase transformation to the electrical properties of the diode is unclear.

### 2. The Effects of W and GaAs Interdiffusion on the Electrical Degradation of the Diode

According to the RBS results, W diffused into the GaAs substrate at annealing temperatures greater than 650°C. Corresponding outdiffusion of As and probably Ga atoms into the W film was also observed at this annealing temperature. After annealing at 700°C for 20 minutes, the W concentration was ~ 0.3 at .% at a depth of 500 - 600 Å below the W/GaAs interface. Since the W is known to be an acceptor in GaAs [15,16], it is expected that the W atoms which diffuse into the GaAs substrate will change the electronic properties of the

n-type GaAs at the interface. Therefore, W diffusion will affect the electrical properties of the diode in two ways. First, the W levels present a high concentration of recombination centers near the junction. As a result, the recombination current of the diode increases. According to the Shockley-Read-Hall model [17,18], the recombination current $J_r$ can be expressed as

$$J_r = J_{ro} \exp(\frac{qV}{2kT}),$$

where $J_{ro}$ is the prefactor which depends on the geometry of the diode and the electronic properties of the substrate material. Therefore, the ideality factor for the forward I-V characteristics of the diode will approach 2 when the recombination current is large. The reverse leakage of the diode will also increase when the recombination current increases. These effects were observed in the I-V characteristics of the W/GaAs diodes annealed at 600°C and 700°C shown in Fig. 8. The sample annealed at 600°C had n = 1.13 which was slightly higher than diodes annealed at lower temperatures ($n < 1.1$). The leakage current for this diode was an order of magnitude higher than that for diodes annealed at lower temperatures. Further increase in the recombination current was noted for diodes annealed at 700°C. The ideality factor n for these diodes increased to 1.5 and their leakage increased by a factor of five (as compared to the 600°C annealed diode). Thus it was suspected that significant W diffusion actually started at ~ 600°C but this diffusion was, however, below the detectable limit of RBS ($< 10^{18}$ atoms/cm$^3$) and could not be observed in the spectra.

Second, when the concentration of W acceptors in GaAs is high enough, the shallow donors will be significantly compensated by these acceptors resulting in a non-abrupt layer of higher resistivity GaAs at the interface. In our

case, this highly resistive layer was between 600 Å and 1000 Å thick and did not have sharp interface with the n-GaAs. The existence of this layer for the 600°C and 700°C annealed diodes was indirectly confirmed by the inversion behavior at reverse bias in the low frequency C-V measurements on these diodes shown in Fig. 12. Furthermore, a calculation of the series resistance of the diode using the I-V data based on the Norde's function [19,20] indicated an order of magnitude increase in the series resistance of the 700°C annealed diode as compared to the 500°C annealed diode. Such an increase in the series resistance strongly suggested the presence of a highly resistive layer near the W/GaAs interface. Table II shows the results of the series resistance calculations derived from the Norde's approach. In other words, the W/n-GaAs diode became a W/GaAs:Te+W/n-GaAs structure after annealing at temperatures > 600°C. Therefore, the electrical behavior deviated significantly from the ideal rectifying behavior after high temperature treatment. Schematics of the possible band structure of the diode before and after 700°C annealing are shown in Fig. 13.

Similar electrical degradation was observed by Waldrop [3] for W/GaAs diodes annealed at temperatures > 550°C. However, no structural information on the interdiffusion of W and GaAs in this temperature range has been reported in the literature.

### 3. Effects of W-GaAs Reactions on the Electrical Degradations of the Diode

The TEM and RBS measurements showed that above 850°C annealing, the W overlayer started to react with the GaAs substrate and the reaction product, $W_2As_3$, tended to ball up forming islands on the GaAs surface. The Ga produced from the dissociation of the GaAs during reaction possibly diffused

through the voids along the W grain boundaries and into the $SiO_2$ cap. At this stage, the diode was physically degraded with a very rough interface as can be observed from the SEM micrographs in Fig. 10. A schematic diagram for the structure of the diode as it proceeded through ever higher annealing temperatures is shown in Fig. 14. Parameters such as ideality factor, Schottky barrier height, depletion width, etc., obtained from electrical measurements (I-V, C-V) become meaningless for these cases as indicated by our results.

## V. SUMMARY

The electrical behavior of W/n-GaAs diodes was studied for different annealing temperatures ranging from 100 - 900°C. Ideal diode characteristics were observed for diodes annealed at temperatures between 300°C and 500°C. Diode degradation in terms of ideality factors larger than 1.14 and unreasonable Schottky barrier heights were observed for diodes annealed at temperatures higher than 600°C. For diodes annealed between 600°C and 750°C, the degradation was found to be correlated with the diffusion of W into the GaAs substrate. The in-diffused W atoms create acceptor-type recombination centers and compensate the shallow donors (Te in this study) resulting in a non-abrupt transition layer of GaAs with high resistivity at the interface. Annealing the diodes at temperatures > 800°C results in the "physical breakdown" of diodes with islands of $W_2As_3$ formed at the interface.

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TABLE I. Electron diffraction data[a] of W/GaAs samples as-deposited and annealed at 750°C and 900°C for 20 min. X-ray powder diffraction data of α-W, β-W and $W_2As_3$ phases taken from the JCPDS diffraction file are also shown for comparison.

| Transmission Electron Diffraction Data | | | X-Ray Powder Diffraction Data [b] | | |
|---|---|---|---|---|---|
| as-deposited | 750°C 20 min | 900°C 20 min | β-W | α-W | $W_2As_3$ |
| | 0.79 | | | | 0.787(001) |
| | 0.58 | 0.59 | | | |
| | 0.56 | | | | 0.548(200) |
| 0.507(w) | | | 0.504(100)[c] | | |
| | 0.473 | 0.467 | | | 0.472(20$\bar{2}$) |
| | 0.424 | | | | |
| 0.359(w) | 0.366 | | 0.356(110)[c] | | 0.363(201) |
| | 0.330 | | | | 0.330(40$\bar{2}$) |
| 0.257(m) | 0.264 | 0.262 | 0.252(200) | | 0.263(31$\bar{1}$,003) |
| | | 0.233 | | | 0.232(20$\bar{4}$) |
| 0.229(s) | 0.225(s) | 0.226 | 0.225(210) | 0.224(110) | 0.227(31$\bar{3}$) |
| 0.206(m) | | | 0.206(211) | | 0.207(51$\bar{2}$) |
| | 0.175 | | | | 0.179(312) |
| | 0.158 | 0.157 | | 0.158(200) | 0.156-0.159(220, 60$\bar{6}$,601,40$\bar{6}$) |
| | 0.151 | 0.151 | | | 0.151(022,11$\bar{5}$) |
| 0.146(w) | | | 0.145(222) | | |
| | 0.142 | | | | 0.142(512,42$\bar{3}$) |
| 0.140(m) | | | 0.140(320) | | |
| 0.135(w) | | | 0.134(321) | | |
| | 0.130(s) | 0.129 | | 0.129(211) | |

[a]All plane spacings are in nm. X-ray data is indexed with hkl in parentheses. (w), (m) and (s) denote weak, medium and strong intensity diffraction rings, respectively.

[b]X-ray data for α-W, β-W and $W_2As_3$ are from cards 2-1138, 4-806 and 18-1415 of the JCPDS powder diffraction file.

[c]These reflections are kinematically forbidden for a perfect A15 structure.

Table II. Series resistances R for the W/GaAs diodes as-deposited and annealed at 500°C and 700°C for 20 min calculated by using the Norde's function.

| | as-deposited | 500°C 20 min | 700°C 20 min |
|---|---|---|---|
| n | 1.1 | 1.05 | 1.34 |
| R(Ω) | 25.4 | 11.5 | 117.5 |

FIGURE CAPTIONS

FIG. 1. (a) - (e) RBS spectra for W/GaAs diodes as-deposited and annealed for 20 min at 650°C, 750°C, 800°C and 900°C.

FIG. 2. W diffusion profiles in GaAs at various temperatures as measured by RBS.

FIG. 3. Characteristic diffusion depth $\delta$ versus $\sqrt{\text{time}}$ for diodes annealed at 700°C for various time durations.

FIG. 4. Plot of diffusion coefficient D calculated from Fig. 2 versus inverse temperature (1/T).

FIG. 5. RBS spectra of 1800 Å W on GaAs as-deposited and 900°C annealed for 20 min.

FIG. 6. SEM micrographs of 1800 Å W on GaAs as-deposited and annealed at 300°C, 700°C and 900°C (magnification ≈ 15 K).

FIG. 7. (a) - (c) Transmission electron diffraction patterns for W/GaAs diodes as-deposited and annealed at 750°C and 900°C with their corresponding TEM bright field images.

FIG. 8. (a) Forward I-V curves for as-deposited and annealed W/GaAs diodes.
(b) Reverse I-V curves for as-deposited and annealed W/GaAs diodes.

FIG. 9. Ideality factor n and Schottky barrier heights $\phi_b$ measured from I-V curves for diodes annealed at different temperatures.

FIG. 10. Leakage current density at 0.4 V reverse bias for diodes annealed at different temperatures.

FIG. 11. (a) Plots of $1/C^2$ versus reverse bias $V_R$ for W/GaAs diodes at different annealing temperatures.
(b) Plots of dopant concentration profiles for diodes annealed at different temperatures calculated from Fig. 4(a).

FIG. 12. Low frequency (80 Hz) C-V plots for as-deposited, 600°C and 700°C annealed W/GaAs diodes.

FIG. 13. Schematic energy band structures for W/GaAs diodes (a) as-deposited, and (b) annealed at 700°C for 20 min.

FIG. 14. Schematic diagrams for the structural evolution of the W/GaAs diode undergoing different annealing temperatures.

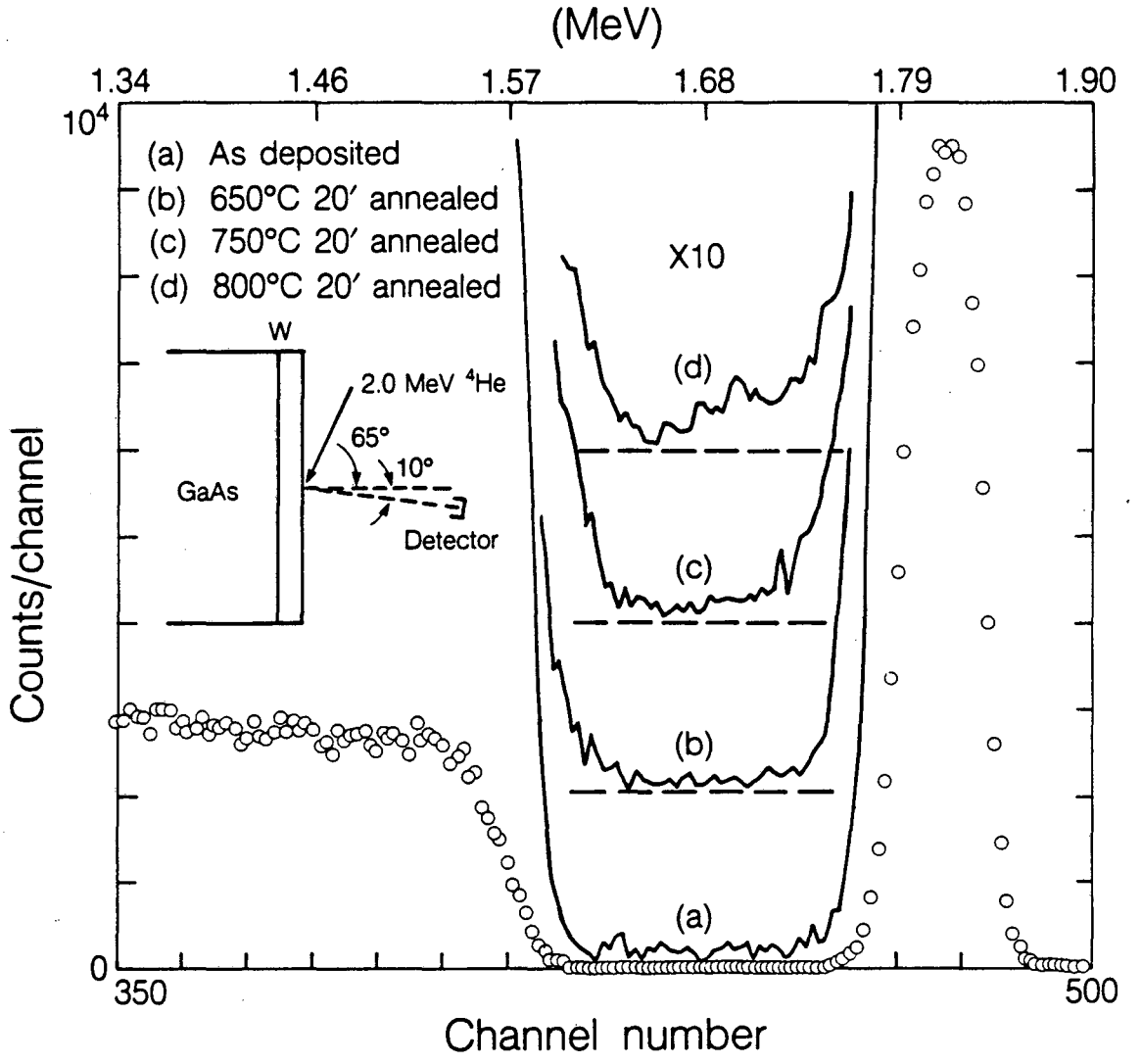


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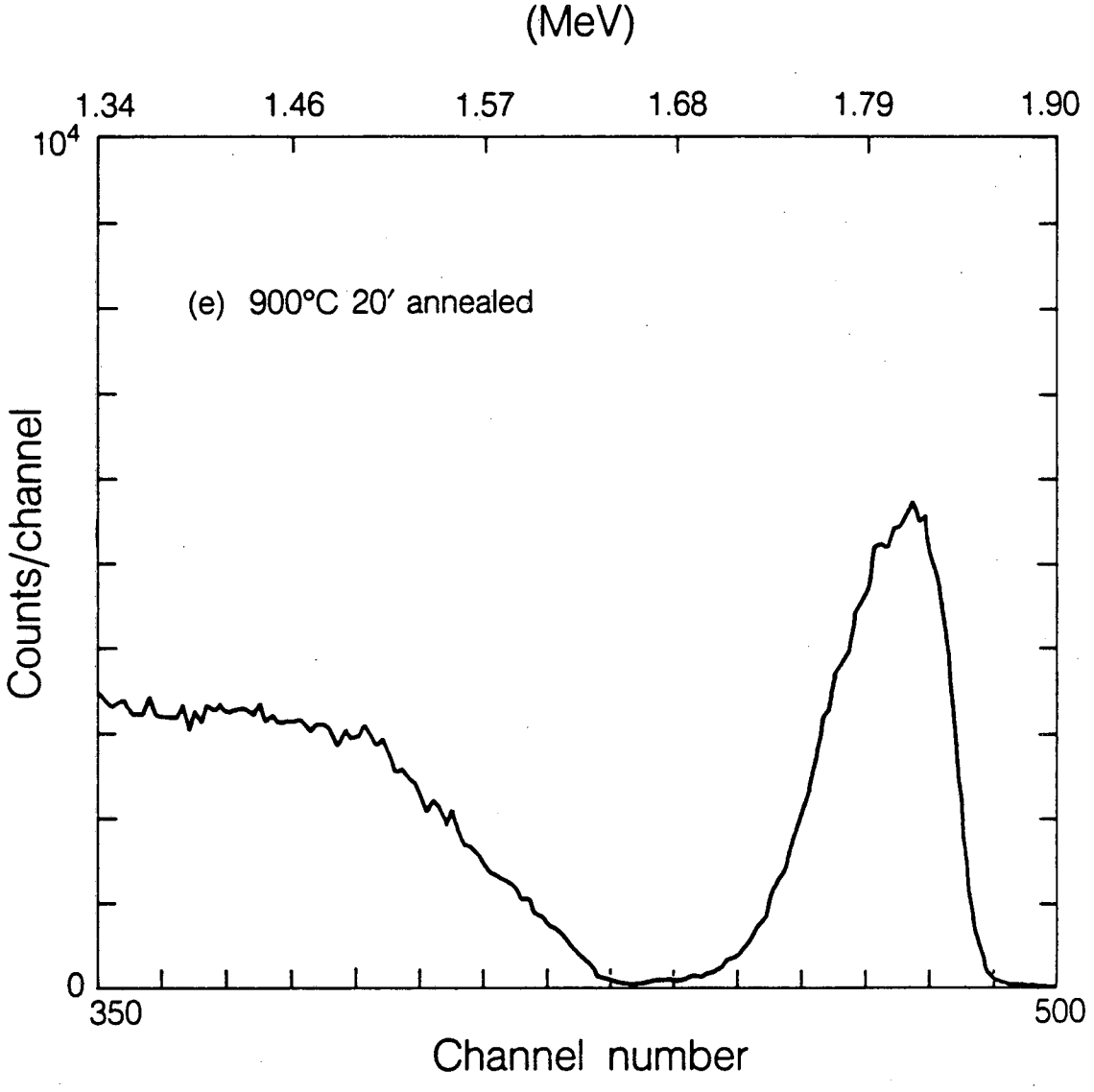
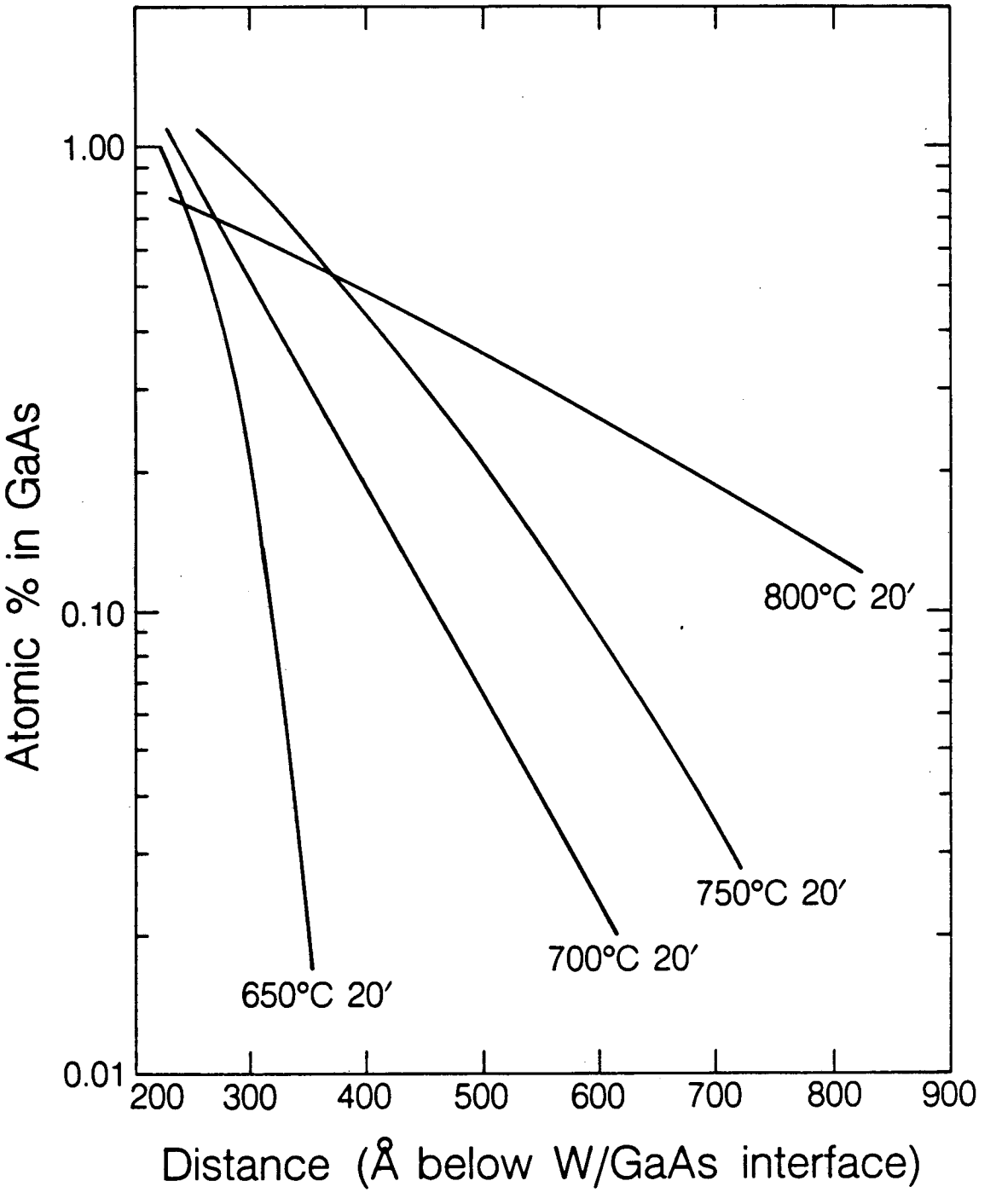
Figure 1



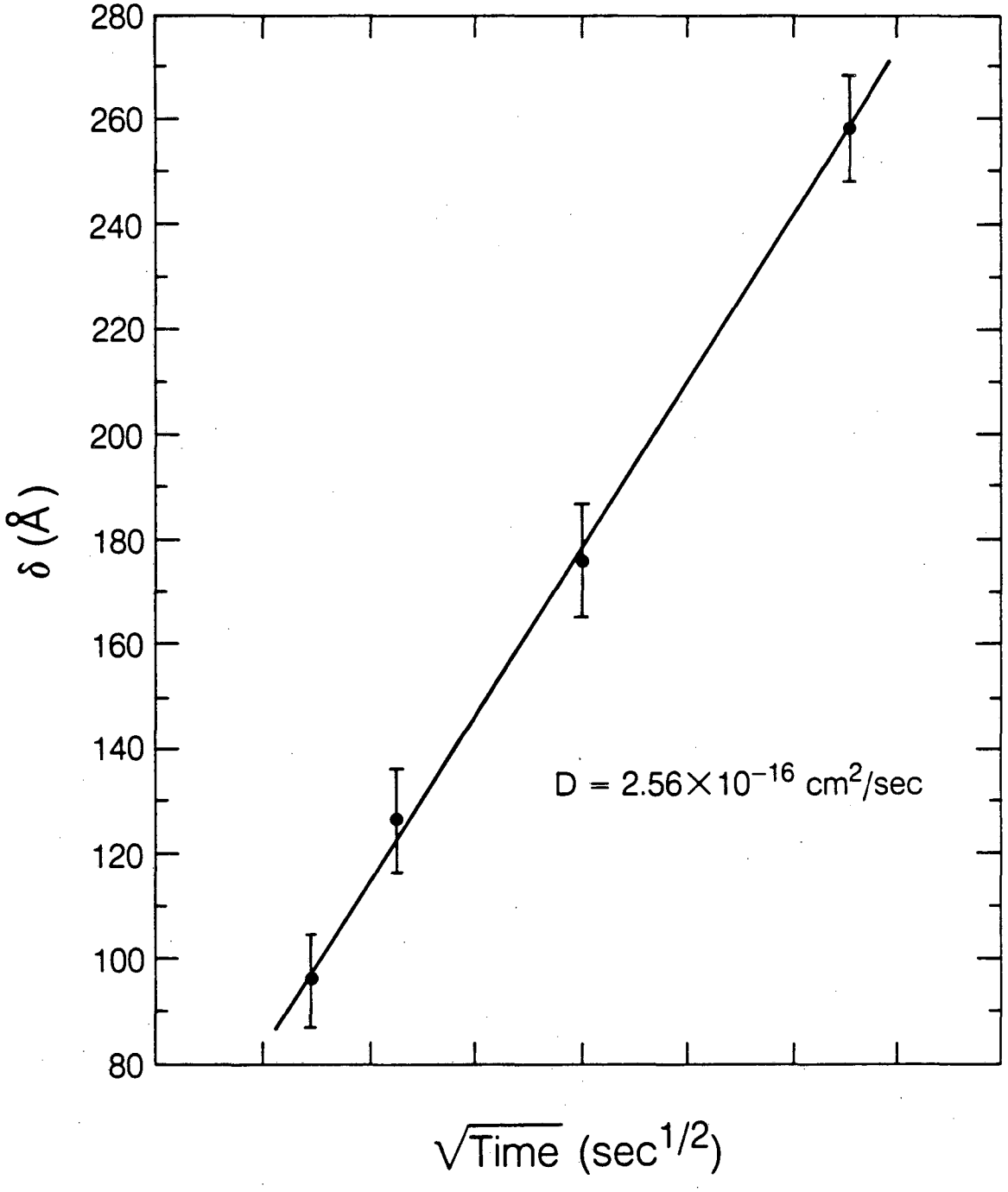

XBL 862-9126

Figure 1(e)



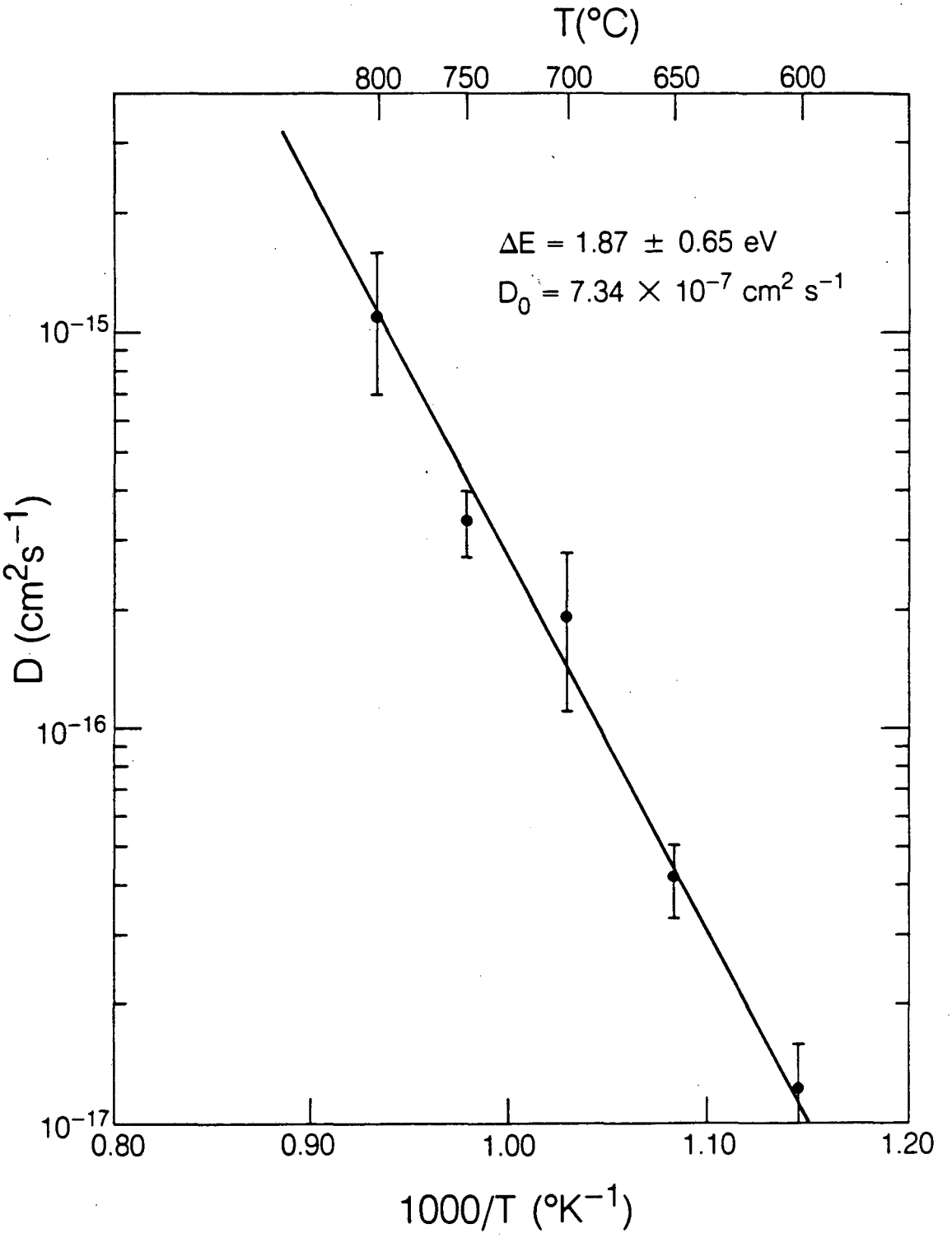

XBL 862-9133

Figure 2



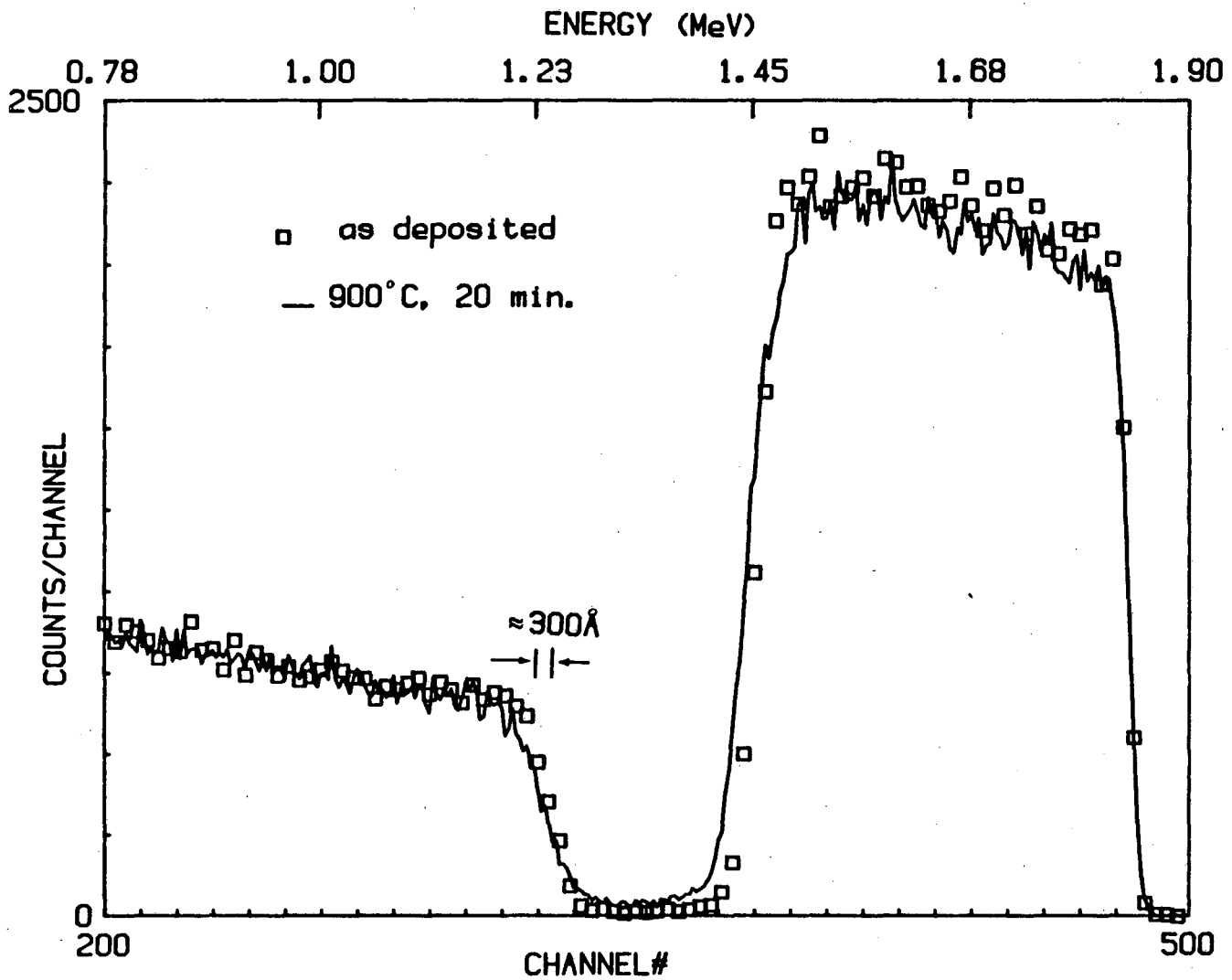

XBL 862-9134

Figure 3




XBL 862-9136

Figure 4

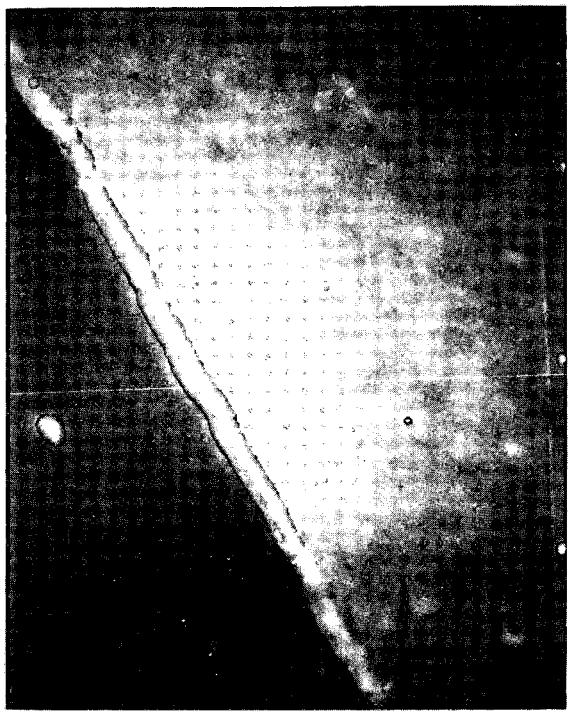



XBL 863-1068

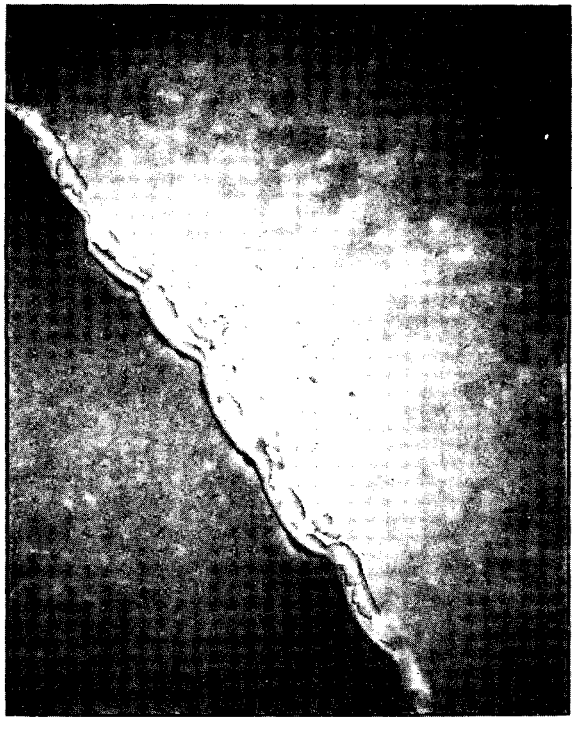
Figure 5

as deposited

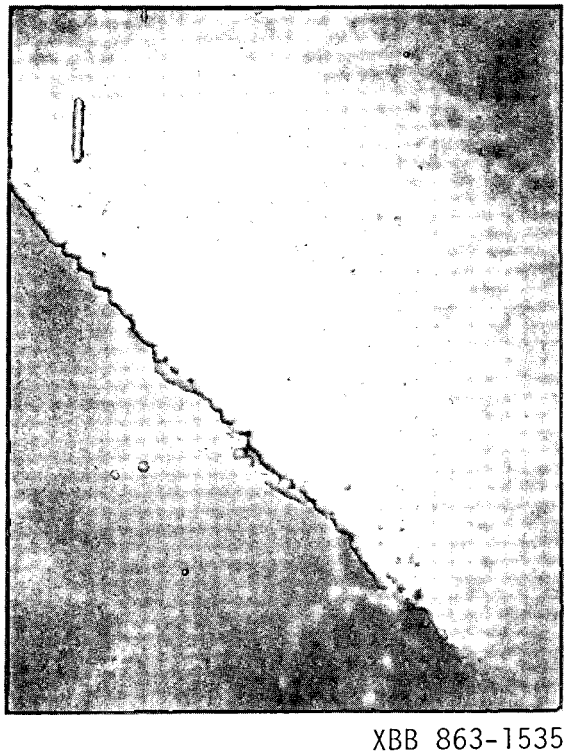
300C 20min.



700C 20min.

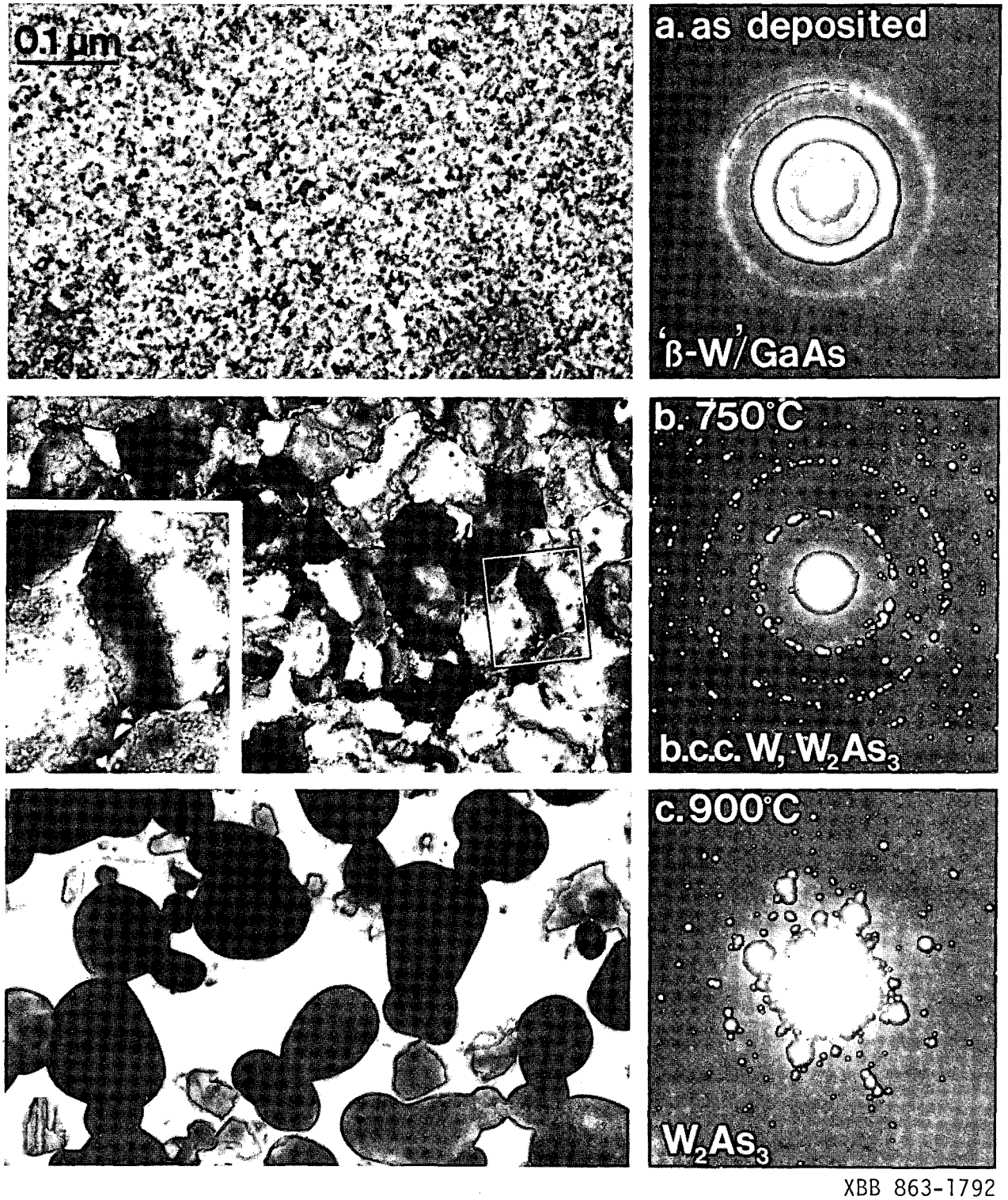


900C 20min.



XBB 863-1535

Figure 6




XBB 863-1792

Figure 7

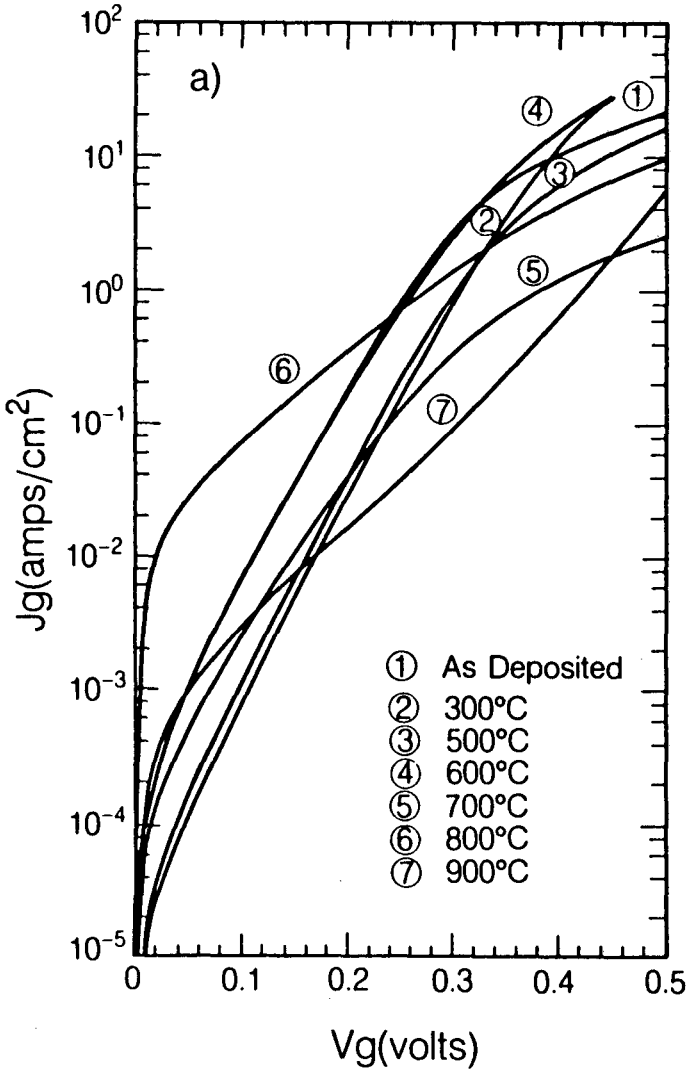
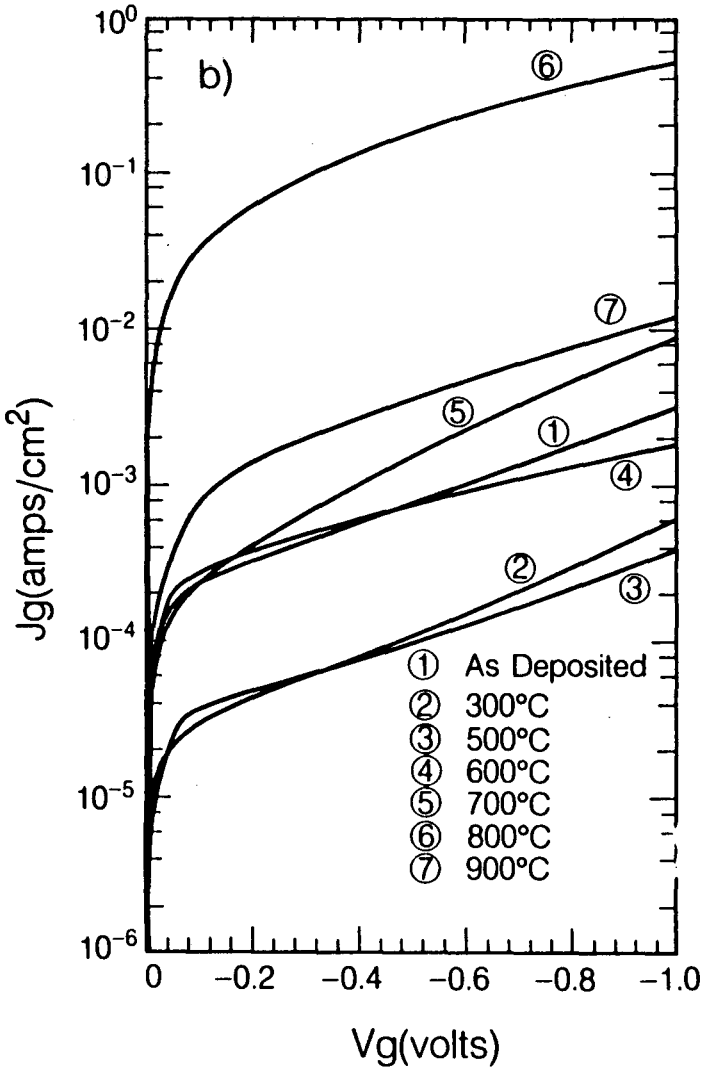
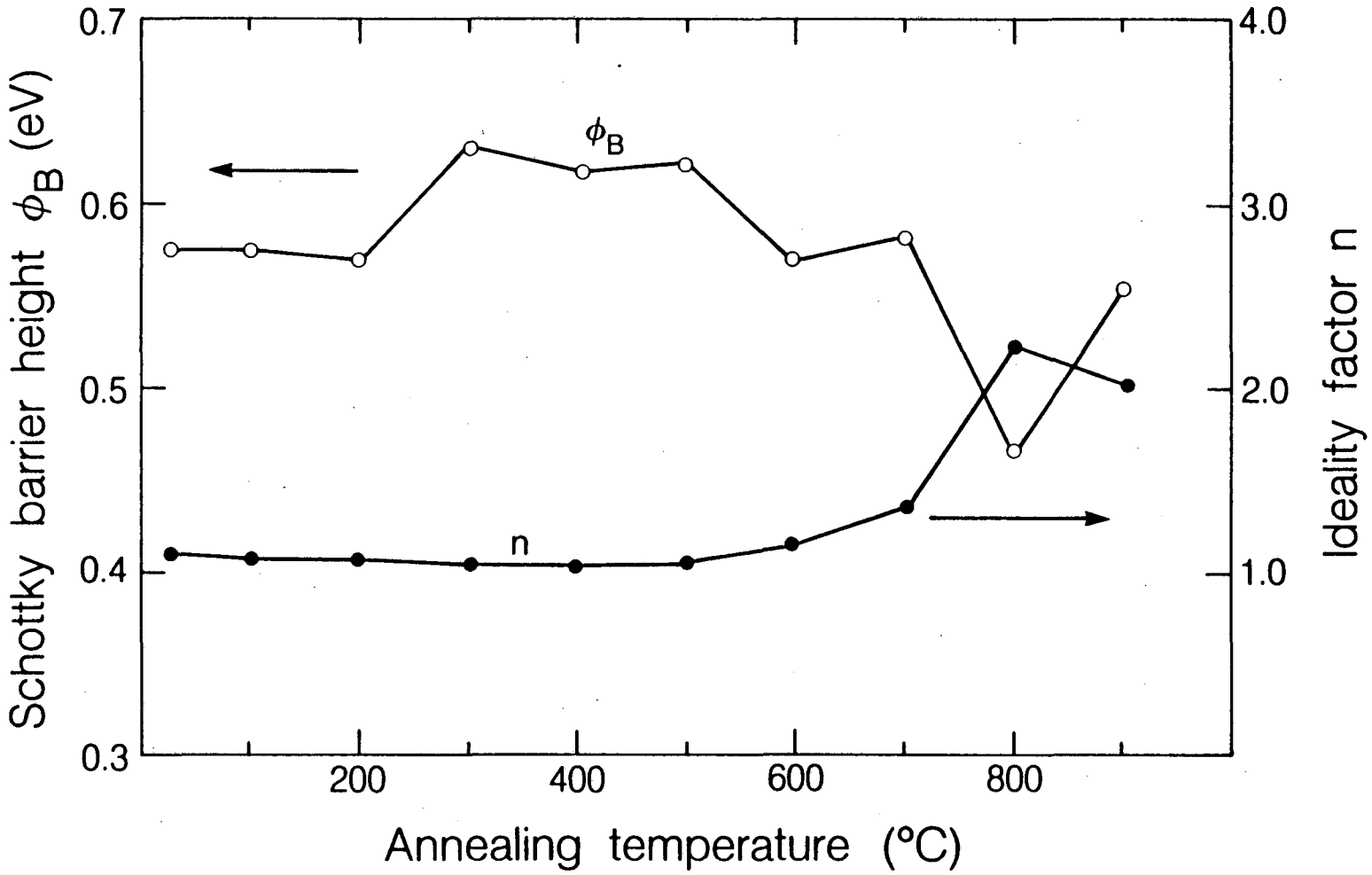



Figure 8
(a)



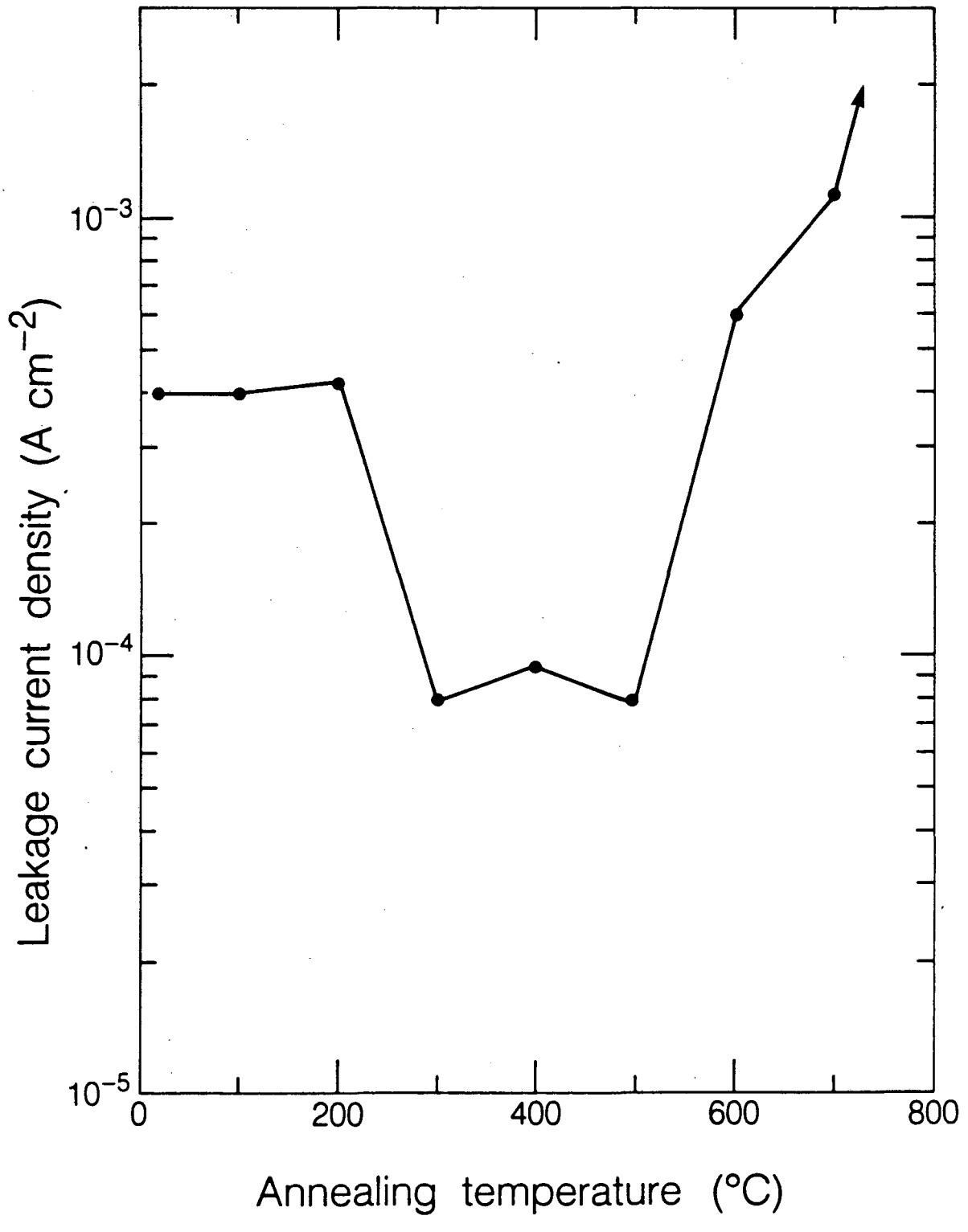

XBL 862-9123

Figure 8
(b)



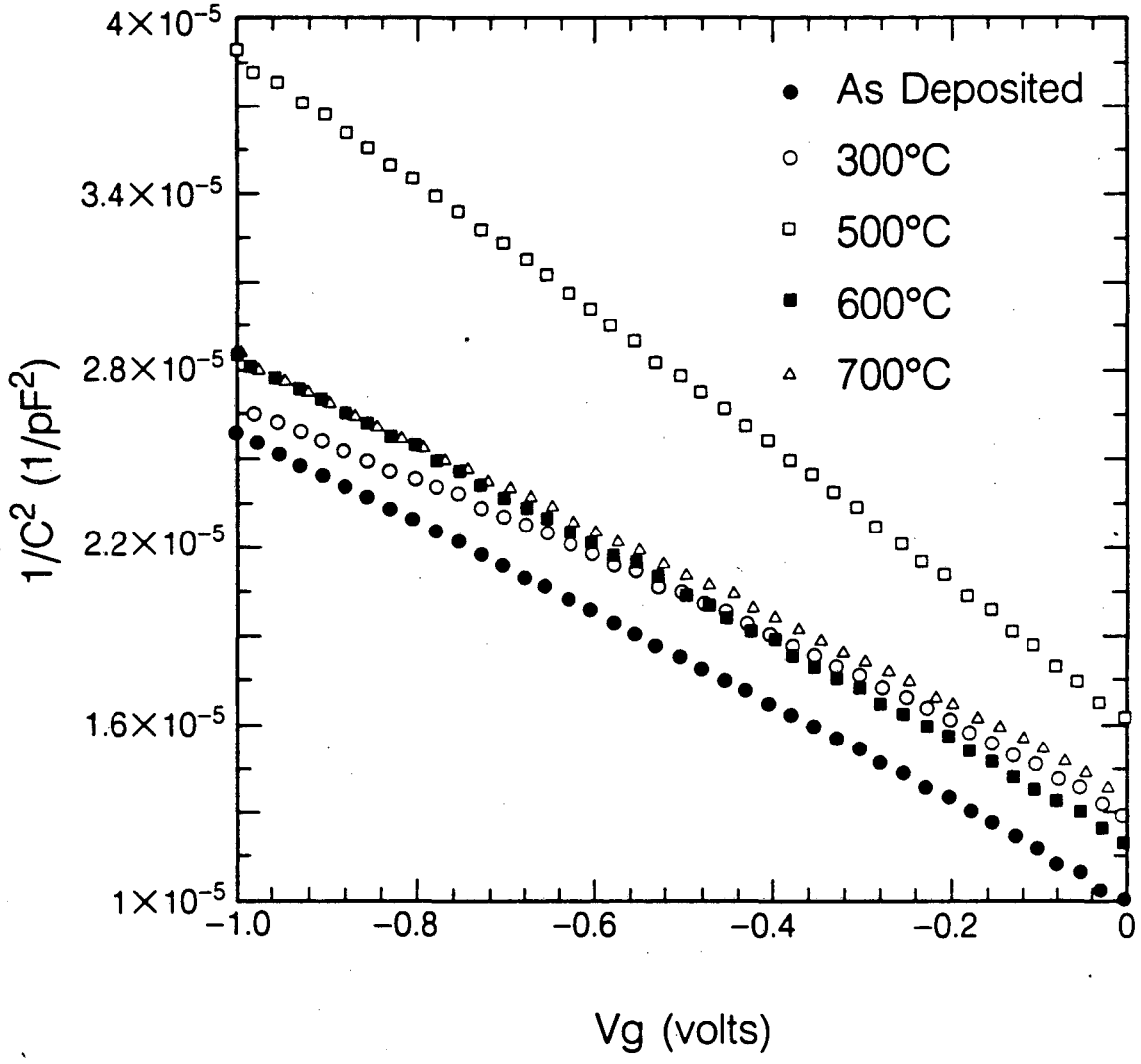

XBL 862-9132

Figure 9



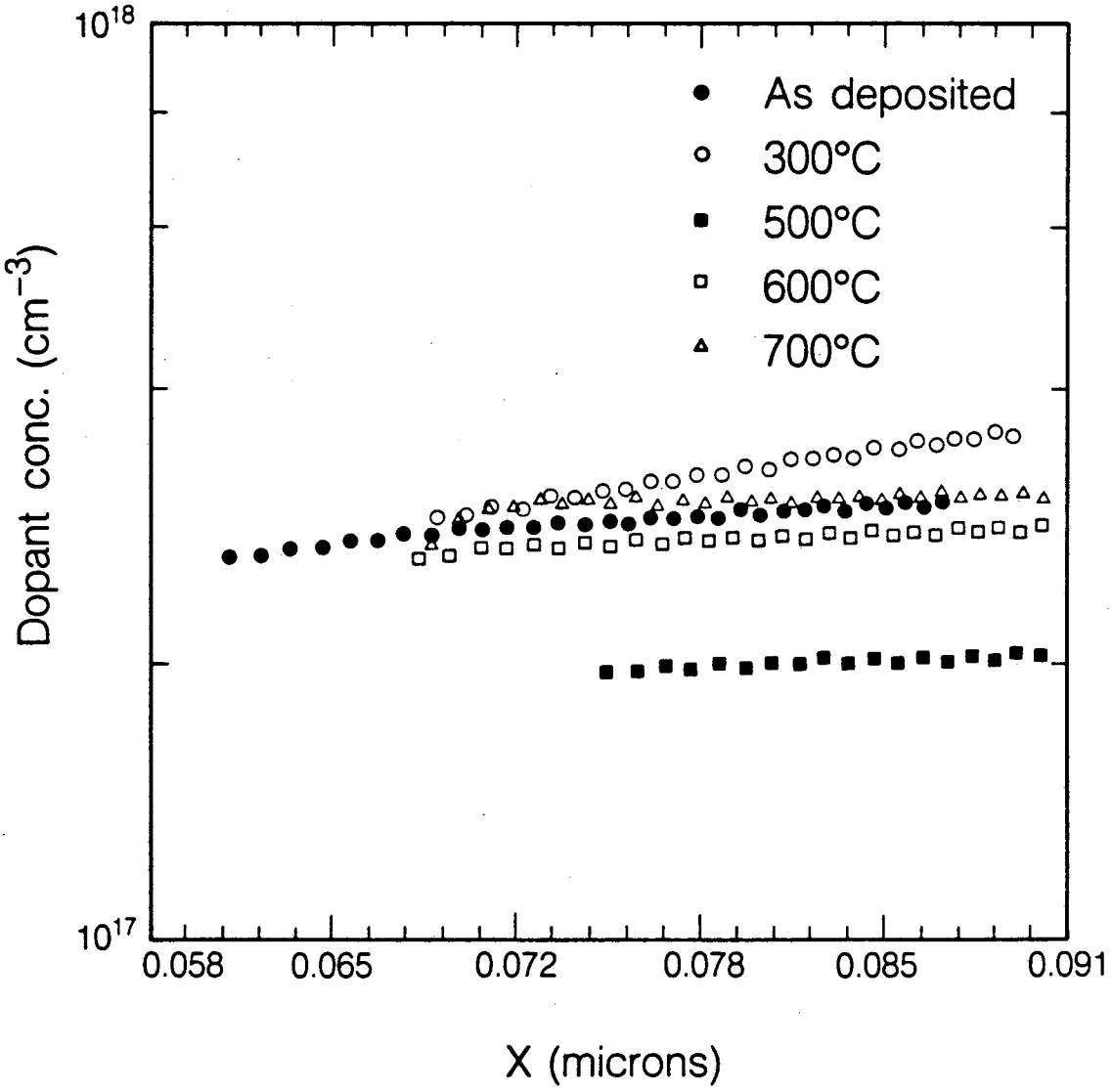

XBL 862-9131

Figure 10



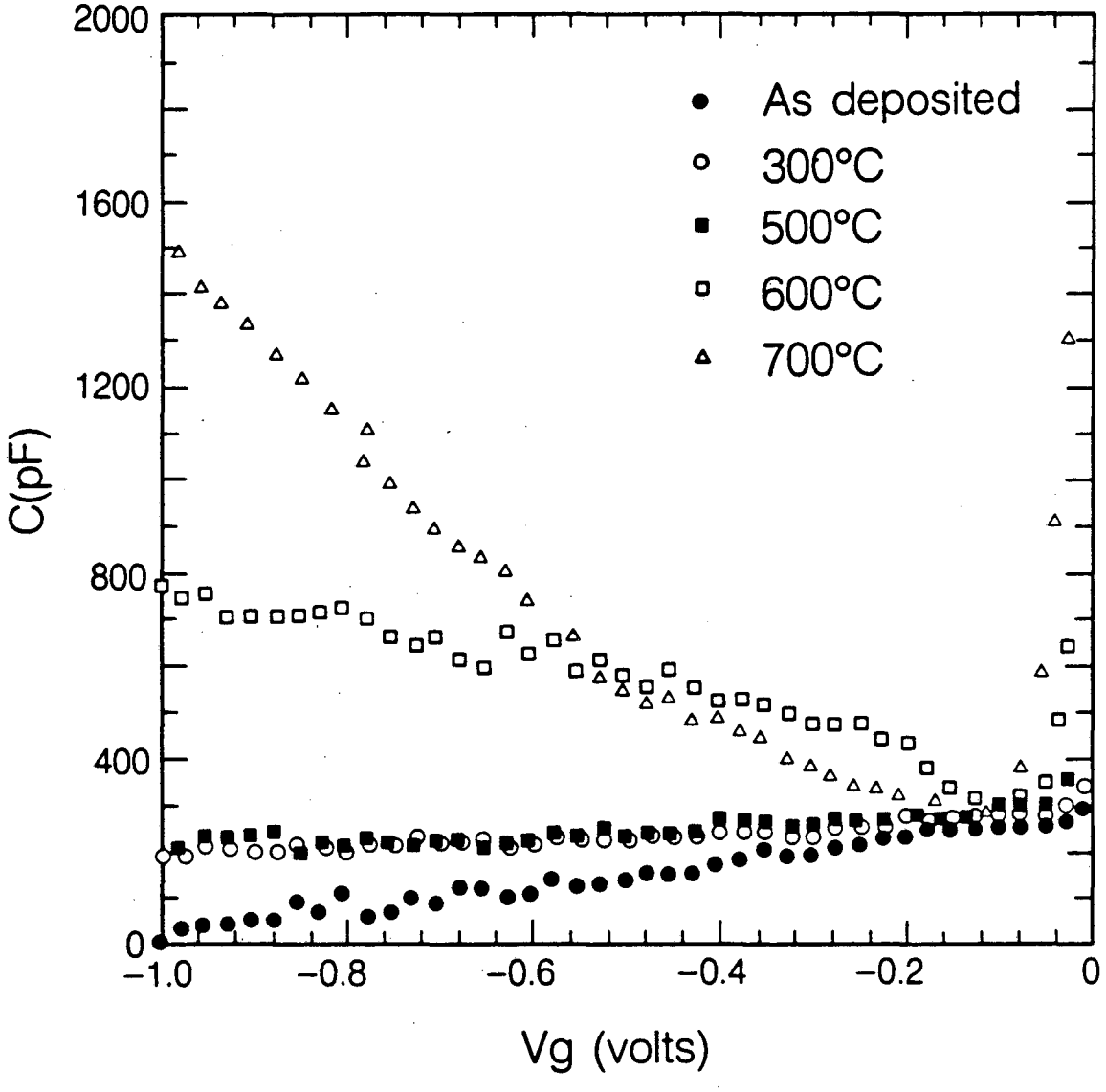

XBL 862-9125

Figure 11
(a)



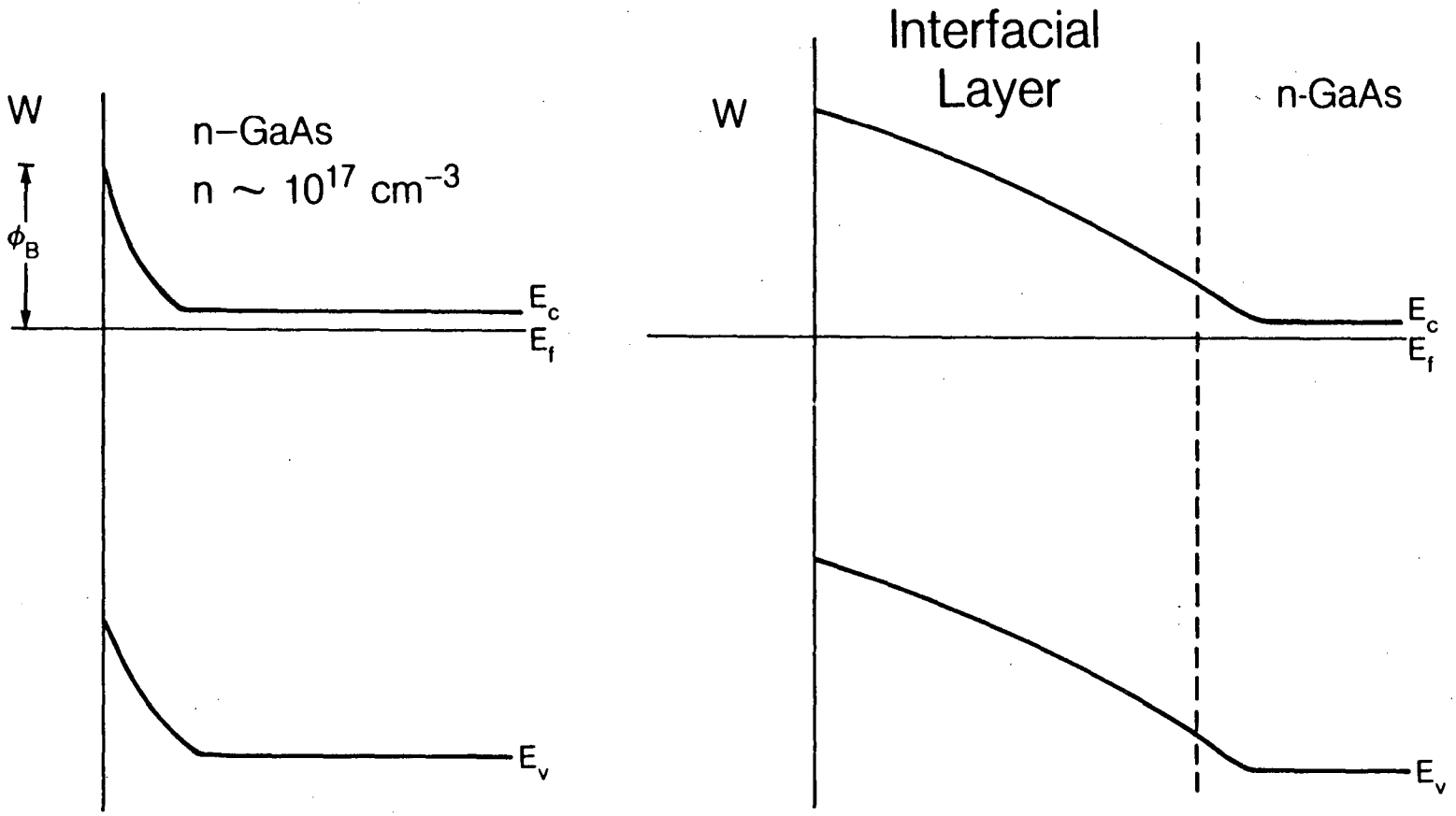

XBL 862-9127

Figure 11
(b)




XBL 862-9128

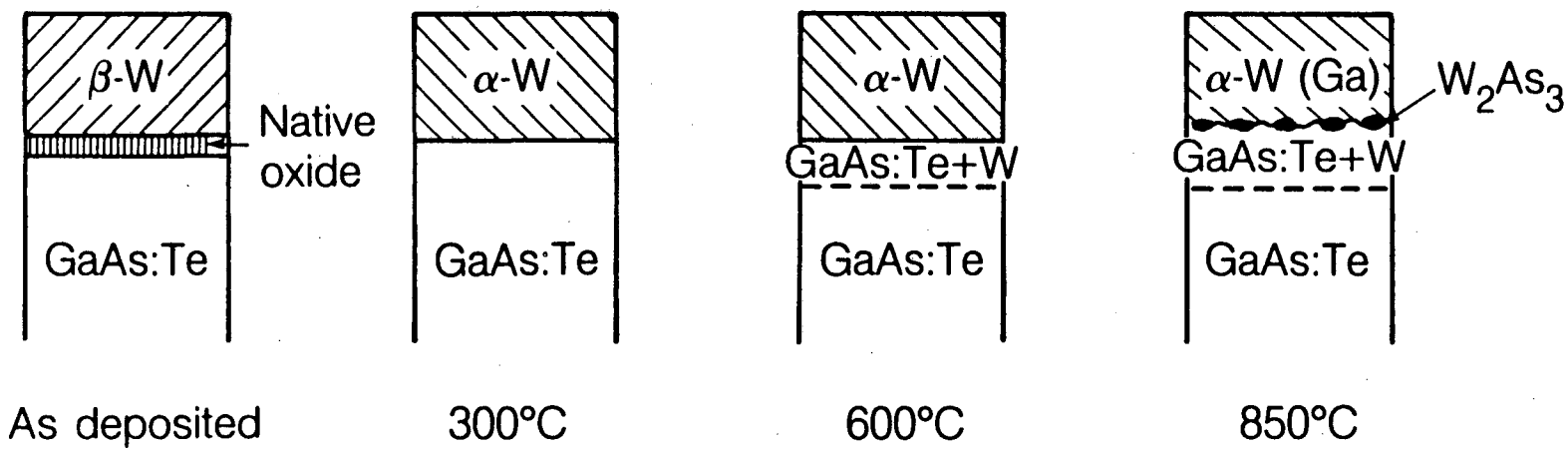
Figure 12




XBL 862-9130

Figure 13

Figure 14




XBL 862-9135

Figure 14

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