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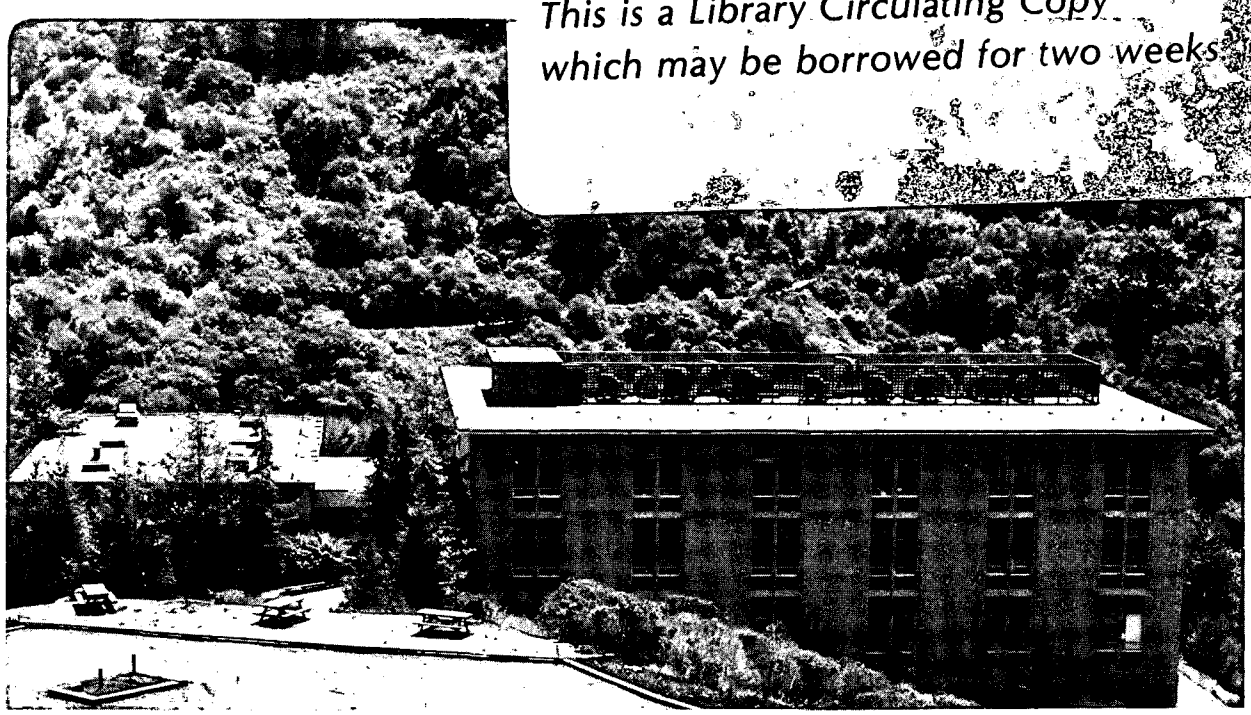

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THE EFFECTS OF INTERFACE REACTIONS ON ELECTRICAL CHARACTERISTICS OF METAL-GaAs CONTACTS

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Solid-state interface reactions between metal thin films and (100) GaAs substrates at elevated temperature are studied by conventional and heavy ion Rutherford backscattering spectrometry, x-ray diffraction and transmission electron microscopy. Metals investigated in this study include Pt, Pd, Ni, Co, Rh and W. Electrical properties of the metal/n-GaAs diodes undergoing annealing treatments at various temperatures were also measured with the current-voltage dependence. Optimum diodes with maximum barrier heights as well as minimum ideality factor and leakage currents are obtained for diodes annealed at temperatures at which a uniform thin layer of reacted phase is observable at the interface. The barrier heights of the optimum diodes show a linear dependence on the work functions of the various metals. The electrical properties of these diodes are discussed in terms of a recently proposed amphoteric native defect model.

According to the classical theory of Schottky [1], a metal coming in contact with a semiconductor creates a potential difference, the Schottky barrier height. This barrier is equal to the difference between the metal work function, ϕ_m and the semiconductor electronic affinity. Although Schottky's model was proposed to explain ideal metal-semiconductor contacts, most experimental results showed that it did not apply to real diodes. In 1947 Bardeen [2] suggested that interface states are important in the "pinning" the Schottky barrier resulting in the insensitivity of the barrier heights to the metal work functions.

Recently, many new models on the Schottky barrier formation mechanisms have been proposed [3,4] to explain experimental results obtained in ultra-high vacuum on atomically clean semiconductor surfaces [5]. One of these models, proposed by Spicer et al [6,7] assumes that the Fermi level position is determined by native defects formed at the interface. Although the simple defects (vacancies [6], antisites [8,9], etc.) were considered, none of them could be positively identified as the defect responsible for the Fermi level pinning. It has been shown recently [10] that a consistent model of Schottky barrier formation can be based on an amphoteric native defect system existing close to the interface. The model is capable of explaining a large variety of experimental results obtained on diodes prepared in ultra high vacuum on atomically clean GaAs surfaces.

However, since the practical Schottky diodes for device applications are prepared under less well controlled conditions, important questions arise:

1) Is the model formulated for the ideal situation still applicable in this case?

2) and How do the interface reactions at elevated temperatures affect the defect distribution at the interface?

To address these issues we have studied effects of thermal annealing on the structural and electrical properties of metal/GaAs contacts. The diodes are fabricated under conventional vacuum conditions ($\sim 10^{-6}$ torr) and only chemical etching is applied to the GaAs surface prior to metal deposition so that ~20Å of native oxide is present at the interface. The diodes are annealed at elevated temperatures in the range of 100-900°C.

Undoped and Te doped (100) GaAs wafers with $\rho > 10^{7}$ Ω-cm and $\rho \sim 10^{-2}$ Ω-cm respectively (Wacker Chemitronic [11]) were degreased in boiling trichloroethylene (TCE) for 5 min. followed by a brief etch in 50% HCl solution to reduce the thickness of the native oxide on the GaAs surface. Metal films (Co, Ni, Rh, Pd, Pt and W) of thicknesses between 100 and 1000 Å were deposited on the wafers by electron gun evaporation (Co, Ni, Rh, Pd and Pt) and RF sputtering (W) with base pressures below 2×10^{-6} torr in the deposition chambers. Circular diodes (diameter ~ 1mm) were patterned on the Te doped wafers by placing a metal shadow mask on the wafers during deposition. The samples were capped on both sides with ~1000Å of SiO_2 before annealing in flowing N_2 ambient at temperatures ranging from 100 to 900°C for 20 min. Ohmic contacts of the diodes were fabricated on the back side of diodes on Te doped wafers by depositing ~1000 Å of a Au-Ge eutectic alloy followed by a brief annealing treatment at 425°C after removal of the oxide caps. Ohmic contacts were formed before metal deposition for diodes annealed at temperatures below 450°C.

Rutherford backscattering spectrometry measurements were carried out with a 2.0MeV $^{4}He^{+}$ (RBS) beam and a 20MeV $^{16}O^{++}$ (heavy ion RBS) beam at a scattering angle of 170°. Improved depth resolution (<40Å) for very thin films (~100Å) was achieved by tilting the specimen at 50-65° with respect to the beam. Plan-view and cross-sectional Transmission Electron Microscopy

(TEM) were performed on some of the samples with a Siemens 102 TEM at 100keV and a JEOL JEM 200CX at 200keV, respectively [10]. Schottky barrier heights (ϕ_{bn}) of the diodes were obtained by considering the ideal thermionic emission equation:

$$J = A^* T^2 \exp\left(\frac{-q\phi_{bn}}{kT}\right) \cdot \left[\exp\left(\frac{qV_a}{nkT}\right) - 1\right]$$

where J is the current density, A* is the effective Richardson constant (taken to be $\approx 8.16\ A/cm^2/K^2$ in this work), k is the Boltzmann constant, V_a is the applied voltage, $q\phi_{bn}$ is the Schottky barrier height of the diode and n is the ideality factor which is ≈ 1 if the thermionic emission process dominates.

Table I shows the summary of the RBS, HIRBS, XRD and TEM results for the six different metal-GaAs systems after annealing at temperatures in the range of 100-900°C. Except for W, which is a refractory metal, all of the metals react with the GaAs substrate at a temperature below 350°C. Note that Co, Ni and Pd form ternary phases (M_xGaAs) with $2<x<4$ at low temperatures (<300°C). These ternary phases are intermediate phases and transform to binary phases at higher temperatures. For Rh and Pt, only binary phases (M-Ga and M-As) are observed at all annealing temperatures higher than 300°C. After annealing at temperatures higher than 600°C only binary phases are detected in all cases. Vertical phase separation with M-As at the interface and M-Ga on top is detected for systems which form binary intermediate phases (Pt and Rh). For systems which form ternary intermediate phases (Co, Ni and Pd) both the M-As and M-Ga phases are in intimate contact with the GaAs substrate at high temperatures. The W-GaAs system is a special case in this study since no interface reaction is observed up to 700°C. Only a W_2As_3 phase in the

form of islands is identified after annealing at temperatures higher than 750°C.

A summary of the electrical measurements of the six types of diodes is given in table II. The values of ϕ_{bn}, n and leakage current densities at -0.4V bias shown in table II are those of the best diode (lowest n and leakage and highest ϕ_{bn}) for each system. The annealing temperatures at which these diodes are obtained, T_o, are also given in table II. Correction to the image force lowering effect on the barrier heights (~ 0.04eV) [12] is included in the values of ϕ_{bn} shown in table II. Comparing tables I and II, we notice that the values of T_o are the same as those at which initial reactions at the interface are observed. For the W/GaAs diode, although no metallurgical reaction is observed up to 700°C, the diode exhibits ideal behavior after annealing at 300°C and remains so up to 600°C. This can be attributed to the balling up of the native oxide at high temperatures resulting in an intimate contact between the W and the GaAs [13]. In addition, W, being the most electropositive of the metals studied, may react with the GaAs native oxide [14]. Note that the ideality factors for these diodes deviate significantly from unity (n~1.2). This is mainly due to the high doping concentration of the substrates ($n \approx 2\text{-}3 \times 10^{17} cm^{-3}$). An exception is the W diode (n≈1.05) which has a better interface as a result of sputter deposition. These values of n are in good agreement with the results of Zussman [15] who explored the effects of high substrate doping and different deposition techniques on the diode characteristics.

Degradation in the diode properties for Co, Ni, and Pd diodes is observed after annealing at temperatures higher than 350°C. This can be correlated to the formation of laterally irregular interface morphology of the diodes resulting from the disintegration of the intermediate ternary phases and

precipitation of binary phases at this temperature range. Degradation of the Pt diode starts at temperatures higher than 500°C due to the interdiffusion of Pt and Ga and As atoms at the interface region as observed by Yu et al [16] and Sands et al [17]. The Rh diode experiences a degradation at ~400°C and a recovery at ~450°C with final degradation at ~600°C. This is due to the fact that the metastable phase RhAs formed at 300°C at the interface becomes unstable at ~400°C and the stable $RhAs_2$ phase starts to nucleate. As a result the diode interface becomes laterally non-uniform. As the $RhAs_2$ grows and forms a uniform layer at the interface, good diode properties resume. The degradation of the Rh diode at >600°C is believed to be the effect of interdiffusion of the Rh and Ga and As atoms similar to the Pt diode [18]. Such interdiffusions are also observed for the W diode after annealing at temperatures >650°C and account for the degradation of the W diode at these temperatures [13].

Values of the barrier heights for the diodes annealed at optimum temperatures along with the barrier heights of as deposited diodes are shown in figure 1. Note a very distinct difference between the more reactive metals Co, Ni and Pd and the relatively nonreactive ones, W and Pt. The diodes with reactive metals show no substantial increase of the barrier height upon annealing. In this case the barrier properties are well established during room temperature metal deposition. Barrier heights for nonreactive metals increase upon annealing at elevated temperatures. This effect is especially visible for Pt diodes where an increase of the barrier height by more than 0.2 eV is oberved.

The presented experimental data can be understood in terms of he recently proposed amphoteric defect model [10]. In this model the barrier height is determined by the pinning of the Fermi energy in the energy range 0.5 to 0.7eV

above the valence band maximum. This leads to the barrier height limits ϕ_{bn}^{max} =0.92 eV and ϕ_{bn}^{min} =0.72 eV. The lower and upper limit of this range is given by an energy level of (As_{Ga}, V_{As}) donor complex and the V_{Ga} acceptor, respectively. The final pinning positions in this range depend on additional factors such as metal electronegativity (or work function) and concentration of the native defects. The latter factor may in turn be affected by the surface preparation conditions and/or solid phase reactions at the interface.

It is known that the surface preparation technique used in the present work leads to an oxidized surface [17,19-21] with Fermi level pinned at ~ 0.7 eV above the valence band [22]. Deposition of a nonreactive metal results in the formation of a barrier determined by this initial pinning. On the other hand, highly reactive metals disperse the interface oxide during the deposition ensuring intimate contact between metal and semiconductor. For nonreactive metals higher temperatures are required to induce such reactions. The fact that the optimum Schottky barrier heights are very close to the limits predicted by the defect model indicates that most of the defects responsible for pinning are located at some distance from the interface so that they are not affected by the initial chemical reactions at the interface.

The barrier height's dependence on metal electronegativity is in general agreement with the prediction of the defect model. The only exception is the highly electronegative Rh which forms barrier lower than 0.8 eV. To account for such exceptions, better understanding of the effects of interface reaction on the defect stability would be required. As seen in figure 1 the optimum barrier height also shows a linear dependence on the experimental metal work function [23]. This observed linear dependence is believed to be due to the existence of the thin interface reacted layer. For all the metal/GaAs systems

studied, these interface layers have [M]/[GaAs] ≥ 2. They are expected to have work functions close to those of their corresponding metals.

In summary we have found a correlation between initial solid phase reaction at the metal/GaAs interface and the optimum electrical properties of Schottky contacts. We have also shown that the barrier heights agree well with the predictions of the amphoteric native defect mechanism of Schottky barrier formation.

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FIGURE CAPTIONS

Figure 1 Plot of Schottky Barrier Heights ϕ_{bn} of Co, Ni, Rh, Pd, W and Pt-GaAs diodes as deposited (filled circles) and after annealing at T_o (open circles) versus the metal work functions ϕ_m.

TABLE I Initial and final reactions of metal-GaAs systems studied by RBS, HIRBS, TEM and XRD.

Metal-GaAs	Initial Reaction Temp.	Initial Reaction Products	Final Reaction Temp.	Final Reaction Products
Co-GaAs	<300°C	Co_2GaAs	>500°C	CoGa, CoAs
Ni-GaAs	200°C	Ni_3GaAs	>500°C	NiGa, NiAs
Rh-GaAs[a)]	300°C	RhGa, RhAs	500°C	RhGa, $RhAs_2$
Pd-GaAs	250°C	Pd_4GaAs	600°C	PdGa, $PdAs_2$
W-GaAs	—	—	800°C	W_2As_3 islands
Pt-GaAs[a)]	350°C	Pt_3Ga, $PtAs_2$	600°C	PtGa, $PtAs_2$

a) Binary phases are vertically separated in the structure: M-Ga/M-As/GaAs.

TABLE II Summary of electrical measurements on six types of diode after annealing at T_o.

Metal-GaAs	Annealing Temp. T_o	ϕ_{bn}(V)	n	leakage current at -0.4V(A/cm^2)
Co-GaAs	<300°C	0.787	1.29	$6X10^{-6}$
Ni-GaAs	220°C	0.833	1.21	$5X10^{-6}$
Rh-GaAs	300°C	0.781	1.29	$1.5X10^{-5}$
Pd-GaAs	250°C	0.820	1.20	$1.5X10^{-6}$
W-GaAs	300°C	0.679	1.05	$8X10^{-5}$
Pt-GaAs	350°C	0.870	1.30	$8X10^{-7}$

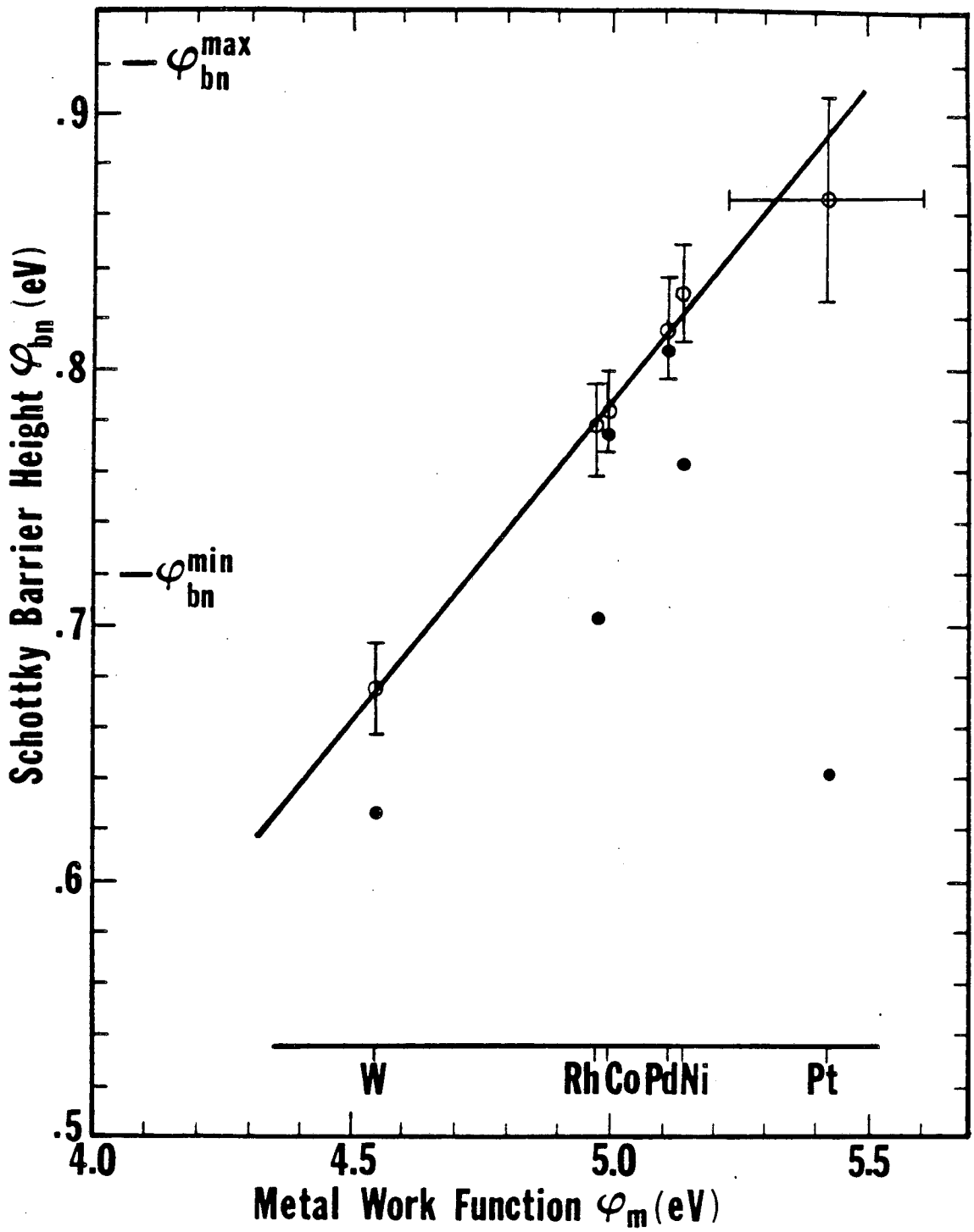

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Figure 1.

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