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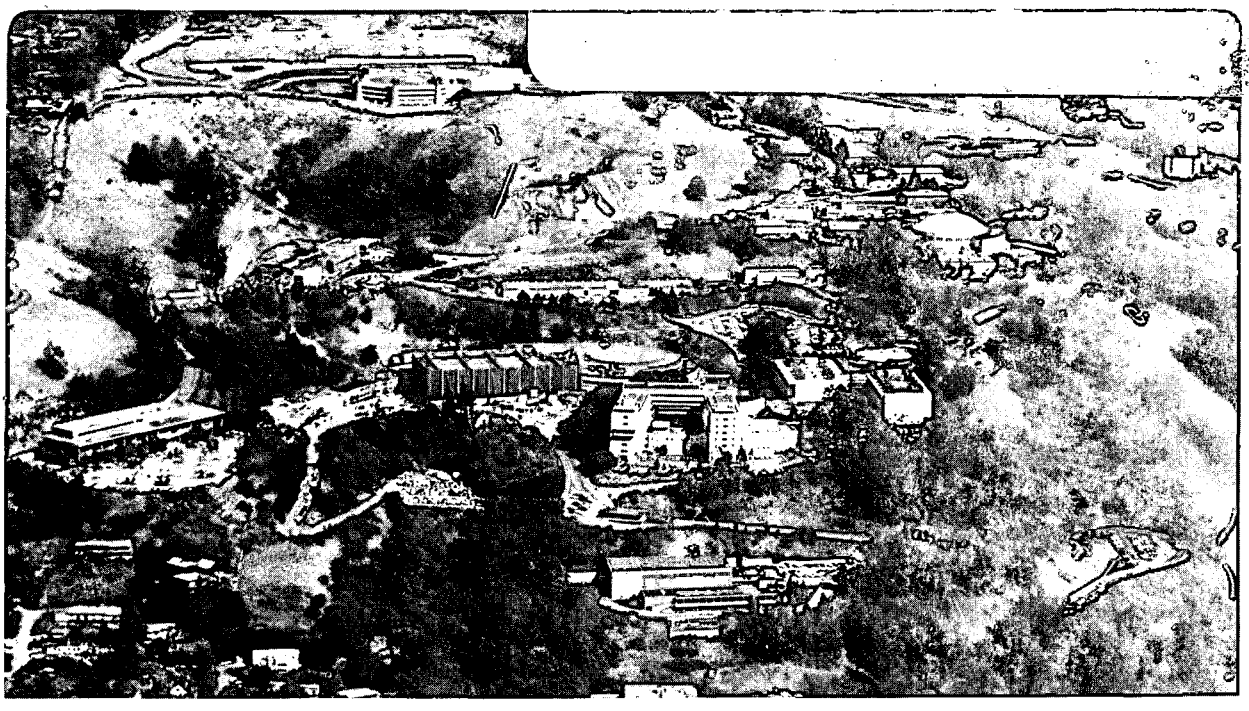

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TEST STANDS FOR THE CENTRAL DRIFT CHAMBER FRONT END HYBRID IN THE STANFORD LINEAR COLLIDER DETECTOR

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ABSTRACT

The Central Drift Chamber (CDC) of the SLAC Linear Collider Detector (SLD) uses 1280 front end electronic hybrid modules. Each of these modules contains over 450 components and performs numerous functions. This paper describes the four test stands for production and detailed circuit characterizations of these hybrids. Descriptions and performance of some of the important functions of the test systems will be presented here.

INTRODUCTION

The hybridized front end electronics of the Central Drift Chamber (CDC) in the Stanford Linear Collider Detector (SLD) contains two high density substrates with numerous functions[1]. All of these functions must be individually and collectively tested before the parts can be used for the detector system. The block diagram in Fig. 1 showing the CDC front end electronics system indicates the many functions to be tested by the test stands. The hybridized package has dimensions of 4.3 cm x 6.6 cm with an overall thickness of 0.8 cm and a total of 50 input/output pins.

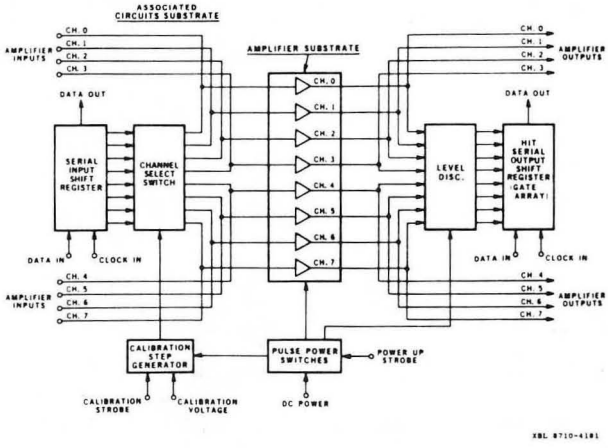

Fig. 1: System block diagram of the CDC front end hybrid.

Figure 2 is a photograph showing the top view of the CDC front end hybrid. The eight well-defined sections are the eight amplifiers on the upper substrate which will be referred to as the amplifier substrate. The 50 pads on the top and lower edges are the input and output connections which are located on the bottom substrate. This substrate will be referred to as the associated circuits substrate. The rest of the circuits are located on the bottom substrate underneath the upper substrate and hence are not visible in the photograph. Connections between the two substrates are made via wire bondings.

After the substrates have been made, the printed traces are tested for shorts and opens before components are mounted. After the amplifier and the associated circuit substrates have been loaded with components, they are individually tested before being connected together. The tests of the two substrates serve to identify non-operational units so they can be set aside. Identification of bad parts enables the defective substrates to be reworked and eventually used in a working hybrid. Tests on a completed hybrid ensure that only good working units are used in the final detector system.

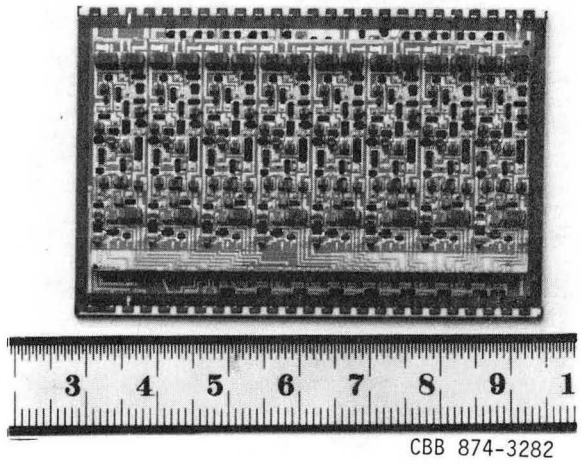

Fig. 2: Photograph of the CDC front end hybrid.

Descriptions of the four test stands are given below. The design and performance of some significant components will be discussed.

PRINTED SUBSTRATE TEST STAND

The main purpose of the first test stand is to find short or open printed traces on the substrates before components are mounted. This is an important screening which eliminates defective substrates before they are used. Figure 3 shows the system block diagram of the test stand which consists of the computer controller and a Substrate Continuity Check Module which contains 48 channels of drivers and receivers. A test voltage is sent out to various traces on the substrate through a certain number of drivers (up to 48) from the Substrate Continuity Check Module. More channels can be provided by additional Substrate Continuity Check Modules. The pattern obtained from the receivers is then compared to a predetermined pattern. If the two patterns do not match, the substrate under test is rejected. It is a simple but an important test in the manufacturing of a hybrid of this complexity.

AMPLIFIER SUBSTRATE TEST STAND

The eight amplifiers on the amplifier substrate have been partitioned into eight sections which are partially shielded from each other by their voltage

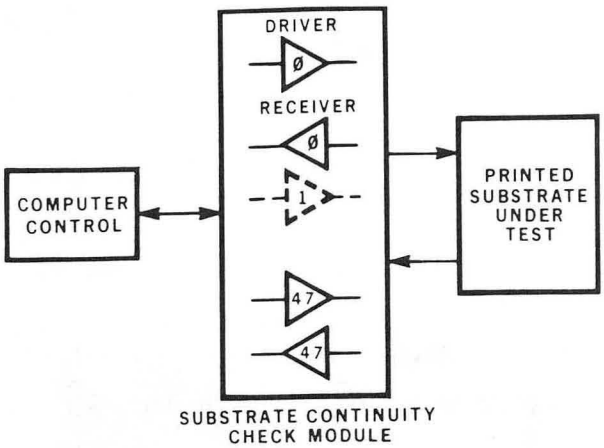

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Fig. 3: Block diagram of the printed susbstrate continuity check test stand.

buses to reduce crosstalk. Input and output grounds are carefully implemented to provide proper signal ground returns. Each amplifier has a calibration and a signal input; hence, there are 16 input lines, 8 input ground lines, 8 signal output lines, 4 output ground lines and 2 power supply lines on this substrate. The four output ground lines are shared by the eight amplifiers - one ground line for two neighboring amplifiers. This is necessary to make the number of input/output pins manageable.

Figure 4 shows the block diagram of the second test stand which is used for testing this substrate. A signal generator provides the signals for both the calibration and signal inputs for each amplifier. The amplifer outputs are sampled by eight comparators whose threshold levels are controlled by the computer. The channel selection input switches are necessary for isolating shorted input lines as well as performing other tests. By using a few input signal levels the amplifier performance through the intended operating dynamic range can be evaluated. Waveshape analysis can also be performed here to provide a more detailed evaluation of the amplifiers.

Figure 5 is a photograph showing a partial prototype test stand for this substrate. The amplifier substrate is situated at the center of the test station. Very fine pins are used to make connections with the 20 x 30 mil pads along the two edges of the substrate for signal inputs and outputs. These pads are used for wire bonding purposes.

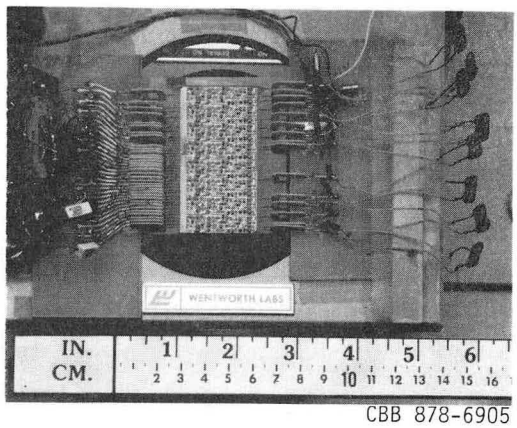

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Fig. 5: Photograph of a partial prototype test stand for the amplifier substrate.

TEST STAND FOR THE ASSOCIATED CIRCUITS SUBSTRATE

Descriptions of the five circuits residing on the bottom substrate are given below:

1. The calibration signal generator provides a voltage step which is used to provide a known charge to the inputs of the amplifiers. Design details of this generator are given in Ref. 2.

2. The input shift register provides selection of channels through eight sets of switches for calibration. Any combination of amplifers can be turned off or on by inputting the proper data to the input register.

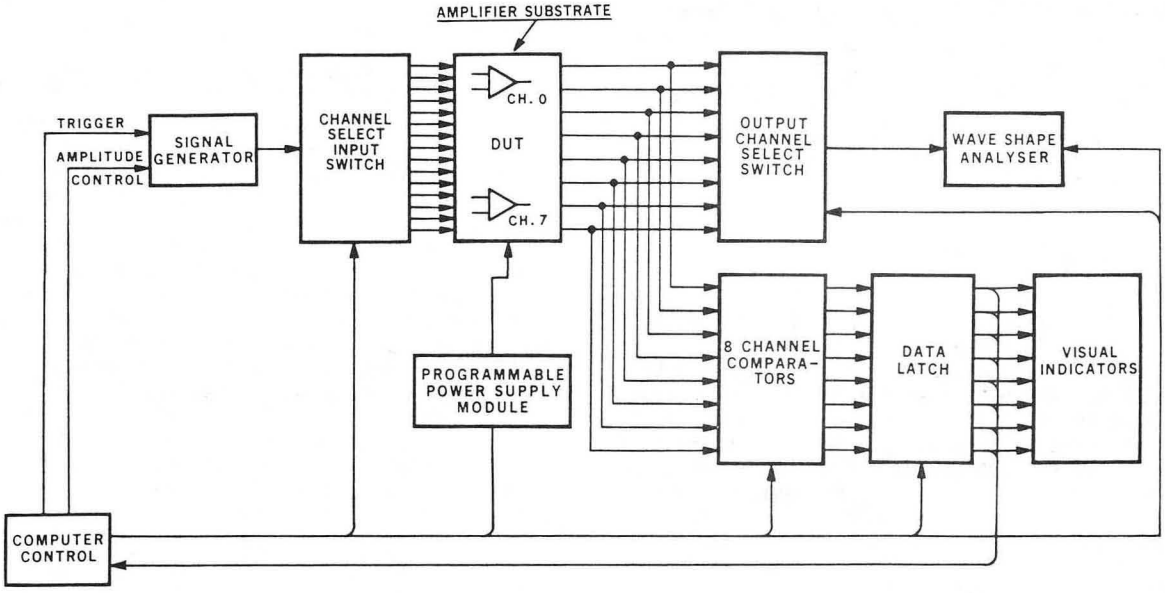

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Fig. 4: Block diagram of the amplifier substrate test stand.

3. The switched power supplies have three transistor switches for supplying +8V, +5V and -5V to the various circuits to reduce average power consumption. Output lines are provided for monitoring the voltages after the switches.

4. The eight discriminators have a common threshold setting. These discriminators provide hit information to an output register.

5. The output register contains CMOS gates and shift registers which have been implemented in the form of a gate array. The hit information is read out for decision making purposes.

The functions of these five circuits are individually tested with the third test stand whose block diagram is given in Fig. 6. Practically all functions on this substrate can be exercised directly from the computer-controlled interface with the exceptions of the triggering signal for the discriminators and the calibration generator output monitoring. Hence a fast comparator used for monitoring the calibration output and a trigger pulse generator whose amplitude and trigger are controlled by the computer are part of this system. The three test stands just described are used mainly for the purpose of screening substrates before they are used to make CDC hybrids.

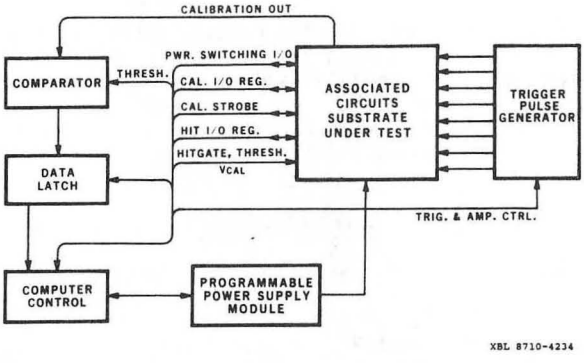

Fig. 6: Block diagram of the associated circuits test stand.

COMPLETE HYBRID TEST STAND

Figure 7 shows a block diagram of the fourth test stand for testing the complete front end hybrid. Performance evaluations such as crosstalk, linearity, I/O transfer function, calibration, input register operation, hit register operation, power-up settling characterization and many other tests must be carried out by this test stand. Many of the test routines from the last two previously described test stands will be included in this test system.

The level sensing comparator system is included in this test stand. A set of input signals at different levels can be used as described in the Amplifier Test Stand section to evaluate the operating dynamic range of the amplifiers. Linearity can also be measured by using the comparator trigger threshold to construct an input/output transfer function of the amplifier under test. The waveshape analyzer can be used to look at the entire output pulse which can then be compared to an acceptable pulse shape used as a standard. A 50-ohm output port is provided at the output of the output channel selection switch for monitoring purposes. Crosstalk can be measured by applying input signals to a number of channels while observing the output of the channel with no input signal. In this case the threshold setting of the comparator is used to measure the crosstalk level.

PROGRAMMABLE POWER SOURCE MODULE

The programmable power supplies are common to all test stands. Provisions have been made to allow the computer to read the load current and voltage of the device under test. This procedure performs a first order test on all substrates and is an important step in screening the substrates. A schematic diagram of such a power supply is given in Fig. 8 to illustrate this simple yet effective function of the test system. The D/A converter accepts a set of data from the computer and converts it to a voltage level. An operational amplifier with a power transistor inserted in the feedback loop serves as the power source which in this case can handle an output current of 1 ampere. The load current is sensed by the 1 ohm resistor. The voltage across this resistor is amplified by the instrumenta-

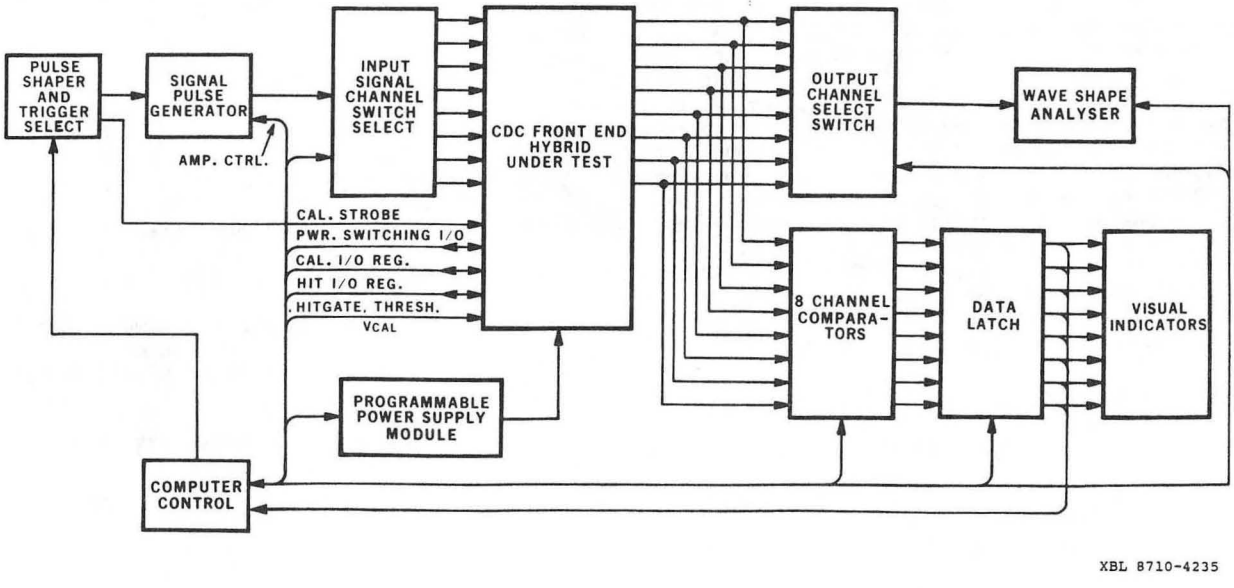

Fig. 7: Block diagram of the complete hybrid test stand.

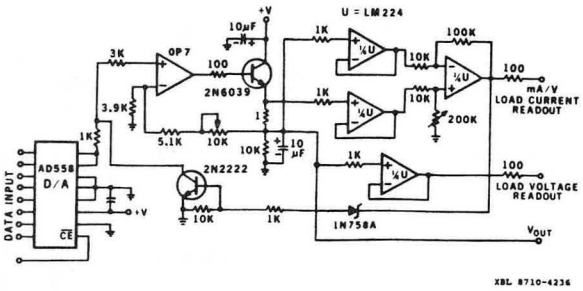

Fig. 8: Schematic diagram of a typical programmable power source.

tion amplifier and read out in mA/volt. The output voltage of the supply is read out directly as the device terminal voltage. Output current limiting is carried out by sensing the output level of the instrumentation amplifier and shutdown is done by shunting the output signal path of the D/A converter to ground. Adjustable current limiting level can be implemented by programmable switches or other similar means.

INPUT SIGNAL CHANNEL SELECTION SWITCHES

The input channel selection switches have been designed in such a way that the isolation between themselves are better than the crosstalk or feedthrough the test stand is used to measure. Sets of two CMOS switches are connected in a series - shunt fashion, and each set is isolated from its adjacent sets by being housed in individual shielded metallic chambers. This configuration provides isolation between switches on the order of less than one half of one percent. Discussion of the switch design is given in Ref. 2.

TEST FACILITIES - ANALOG INTERFACE MODULE

A block diagram showing the Computer, Computer Interface, Digital Bus, Analog Bus, Analog Interface Module (AIM), Dedicated Drivers, Programmable Power Source Module and a Substrate Continuity Check Module is given in Fig. 9. This presents an overall picture of the test facilities for the CDC front end hybrid. Since AIM is going to be used by other hybrid test stands as well, it has been designed to be flexible and able to accommodate a wide variety of testing functions. It consists of a dedicated Programmable Array Logic chip for interfacing, three 16 bit D/A converters, one 8 bit D/A converter, one sample and hold unit in conjunction with a 12 bit A/D converter, 32K of random access memory and one analog data acquisition unit. Self-diagnostic capability has been designed into the system. The combination of these components provides a flexible and powerful test system for a wide variety of needs.

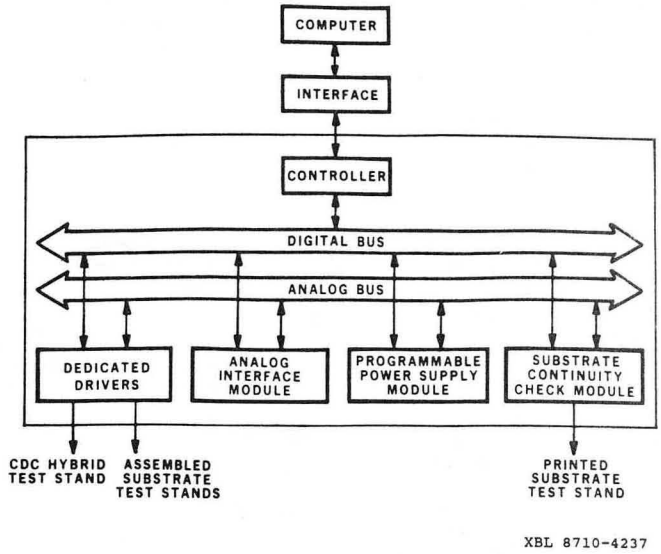

Fig. 9: System block diagram of the CDC front end hybrid test facilities.

CONCLUSION

Four test stands and their test facilities have been presented. Designs on important sections of the system have been completed and discussed. Partial prototype test stands have been used for testing the first version of Central Drift Chammber front end hybrid. Initial test results indicate that the concepts and designs are on course.

ACKNOWLEDGMENTS

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