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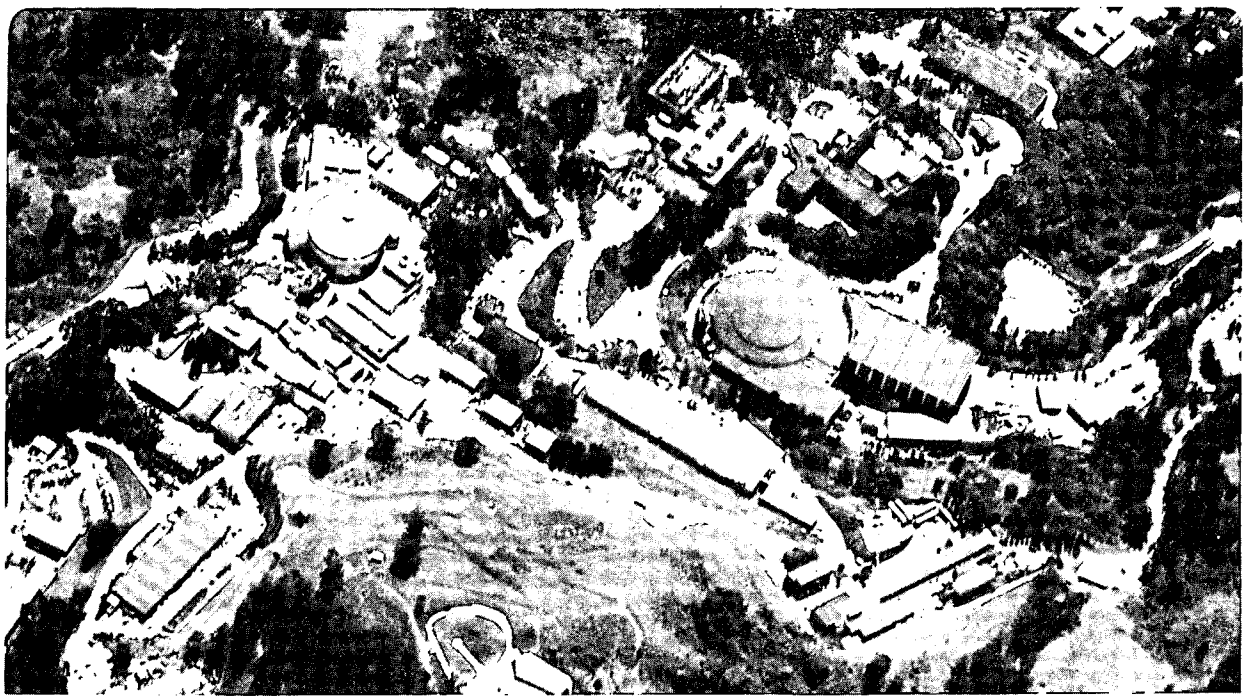

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Fabrication of Detectors and Transistors on High-Resistivity Silicon

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ABSTRACT

A new process for the fabrication of silicon p-i-n diode radiation detectors is described. The utilization of backside gettering in the fabrication process results in the actual physical removal of detrimental impurities from critical device regions. This reduces the sensitivity of detector properties to processing variables while yielding low diode reverse-leakage currents. In addition, gettering permits the use of processing temperatures compatible with integrated-circuit fabrication. P-channel MOSFETs and silicon p-i-n diodes have been fabricated simultaneously on 10 $k\Omega \cdot cm$ <100> silicon using conventional integrated-circuit processing techniques.

1. Introduction

The complexity and scale of many new applications for charged particle detectors, notably in high-energy physics, require well-controlled fabrication techniques. Local front-end and readout circuitry is essential for these systems, and monolithic integration of at least part of this circuitry would greatly simplify the readout system and increase performance and reliability [1]. Even on a smaller scale, devices such as the semiconductor drift chamber [2] would also benefit greatly from integrated front-ends by reducing the circuit capacitance in order to exploit the extremely low capacitance of these detectors. Hence, a modern detector process should offer minimum sensitivity to process-induced contaminants and ideally would be compatible with contemporary integrated-circuit (IC) fabrication techniques.

However, typical fabrication processes for radiation detectors do not fulfill either of these goals. While in one notable case outstanding results have been achieved [3], the process used is incompatible with conventional IC fabrication and is very sensitive to the temperature at which the implanted dopants are annealed [4]. This is due to the extreme sensitivity of detector leakage current to impurities that introduce energy levels near the center of the silicon bandgap [5].

In this work fairly conventional integrated-circuit processing techniques are used to realize low-leakage p-i-n diode detectors. The process developed for the detector fabrication relies on the formation of a gettering layer on the back side of the wafer. By utilizing gettering techniques that actively counteract the presence of harmful impurities in the active volume of the device, the sensitivity of the process to variations in the fabrication environment is greatly reduced. In addition, the use of relatively high processing temperatures is an integral part of the process; this removes a major obstacle to monolithic integration of front-end electronics with the detector. The process described here is fully compatible with conventional IC processing. Data are presented on radiation detectors that demonstrate the effects of gettering and also on p-channel MOSFETs that were fabricated on the same wafer as a first step towards monolithically integrated detector-readout systems.

2. Processing Considerations

A major goal in detector fabrication is the minimization of the diode reverse-leakage current, which contributes shot noise and can limit the dynamic range of the input amplifier. High quality float-zone refined silicon is required in order to achieve the high generation lifetime necessary for low reverse-leakage currents. The leakage current of a reverse-biased p-n junction is due to the generation of minority carriers in the device. These minority carriers can arise from the undepleted neutral region, the depletion region, and the surface [5]. In silicon diodes the leakage current is often dominated by generation in the depletion region. This component of leakage current is greatly enhanced by the presence of impurities that introduce energy levels near the center of the silicon bandgap. Such impurities are often referred to as lifetime killers since they also decrease the generation lifetime. Typical examples are the transition metals [6-7]. These are rather ubiquitous contaminants and great care is needed in the fabrication of devices in order

to achieve low leakage currents.

However, the total elimination of these contaminants has proven to be impractical due to the pervasiveness of such elements and the sensitivity of the leakage current to extremely small concentrations, typically part per billion or less [8-10]. This has led to the development of techniques, collectively known as gettering, which render any lifetime-killing impurities electrically inactive [11]. The basic concept of gettering relies on the fact that at typical integrated-circuit processing temperatures in silicon (approximately 900-1100C) most harmful impurities have relatively high diffusivities and hence are very mobile [12]. Therefore suitable impurity sinks can be incorporated in electrically inactive regions.

Two general classes of gettering are commonly employed. In "intrinsic" gettering, the bulk of the wafer forms the impurity sink with a relatively thin, defect-free region near the surface where the active devices reside. The technique is often applied to Czochralski-grown substrates and relies on the formation of oxygen precipitates in the bulk of the wafer [11]. While perfectly adequate for conventional IC processing, intrinsic gettering is not compatible with thick p-i-n diode detectors, where the depletion region often extends to the backside contact of the wafer. Thus the second class of gettering, "extrinsic" gettering, is utilized in this work. Extrinsic gettering relies on the formation of a gettering layer on the back side of the wafer, away from the active region of the device, e.g. the depletion region of detector diodes. Typical extrinsic gettering techniques include phosphorus doping [8], ion implantation [13], and deposition of thin films such as polysilicon [14] and silicon nitride [15]. Gettering techniques have been applied to detector fabrication, but no details of the actual method used were given [16-17].

3. Experimental procedures/results

Figure 1 shows the detector processing sequence used in this work. The technique shown has been applied to both 1 kΩ · cm <111> and 10 kΩ · cm <100> n-type starting substrates with similar results. Initially a layer of polysilicon, in-situ doped with phosphorus, is deposited at 650C by chemical vapor deposition on the back side of the wafer. This layer, which is approximately 1 μm thick, serves both as the gettering layer and as the backside contact. The gettering properties of this layer are due to the presence of both the polysilicon and the phosphorus. Polysilicon consists of small grains of single crystal material separated

by highly disordered regions called grain boundaries. These grain boundaries act as impurity sinks and hence polysilicon itself is an efficient gettering material [14,18]. In addition, phosphorus also getters impurities by an ion-pairing mechanism [19] and the combination of both methods has been shown to yield synergistic results [20].

After deposition the polysilicon layer is capped by a low-temperature oxide formed by chemical vapor deposition at 450C. This layer minimizes the oxidation of the polysilicon during subsequent processing. A passivating oxide is then thermally grown, followed by selective removal of the oxide in the areas where boron is desired. For this experiment, the boron was diffused at 900C from a B_2O_3 source in order to avoid any crystalline damage at the p-n junction associated with ion implantation. In order to unambiguously determine the effectiveness of the gettering layer, some of the wafers received the backside polysilicon gettering on one half of the wafer only, while the other half received implantation of arsenic to form the back contact. After implantation the wafers were annealed at 900C for fifteen minutes in oxygen followed by a two hour anneal at the same temperature in nitrogen. Conventional aluminum metallization followed by a 400C/450C (<100>/<111>) anneal in forming gas (80% nitrogen, 20% hydrogen) completes the processing.

The detector diodes used in this work were circular in area with a 1 mm radius. In addition, the diodes were surrounded by a circular guard ring consisting of a p^+ region contacted by metallization. The inner radius of the guard ring measured from the center of the diode was 1.1 mm, and the outer radius was 1.4 mm. For the diode current-voltage measurements, the bias voltage was applied to the substrate with the top contact and guard ring grounded.

Figure 2 compares the reverse-leakage currents of gettered and ungettered devices from the same wafer (<100>, 10kΩ · cm). The gettered sample exhibits a substantially reduced leakage current relative to the sample that did not receive the gettering. The current is reduced by a factor of nearly 400 at low voltages and even more at higher voltages where the ungettered sample exhibits a soft breakdown characteristic. The leakage current density at 100V, which corresponds to a fully depleted detector (≈ 250 μm depletion region thickness), is on the order of 1–2 nA/cm^2, which compares very favorably with the result of Kemmer [3]. However, the Kemmer process limits the processing temperatures to 600C after the initial

oxidation. This restriction is necessary in order to maintain low leakage currents for that process, and in fact an attempt to incorporate higher anneal temperatures into a similar process has been reported to increase the leakage current significantly, e.g. 420 nA/cm^2 per 100 μm depletion width after annealing at 900C [4]. In contrast, the devices shown in Figure 2 have undergone approximately 3 hours at 900C after the initial oxide was grown, while maintaining low leakage currents. Thus this process avoids the major drawbacks of the Kemmer process, namely the high sheet resistance of the implanted layers and resulting incompatibility with monolithic integration of active devices.

The current of the gettered device in Figure 2 is relatively insensitive to voltage, which implies that the current is limited by either diffusion of minority carriers from the undepleted regions of the diode, or from surface leakage currents, but not from generation in the depletion region. The bulk generation current is expected to increase with the volume of the depletion region, which is in turn bias-voltage dependent [5].

Similar results were observed for the <111> substrates. However, a significant surface component of leakage current is observed on the <111> substrates (on the order of 3–12 nA/cm^2) [21]. This current arises from electrically active states at the silicon-silicon dioxide interface. It can be suppressed by proper biasing of a metal-oxide-semiconductor (MOS) capacitor located between the diode and guard ring, similar to a gated-diode structure [5]. Once the surface leakage current is suppressed, the gettered devices achieve leakage currents on the order of 1 nA/cm^2 as shown in Figure 3. The higher surface current for the <111> substrates is consistent with the higher density of surface states on oxidized <111> substrates as compared to the <100> orientation [22].

A significant aspect of the gettering process is the fact that the diodes were fabricated at typical integrated-circuit processing temperatures. Thus monolithic integration of detectors and active devices can be investigated with the use of a process employing gettering, and MOS devices on high-resistivity silicon have been reported [23]. In order to pursue this further, polysilicon-gate p-channel MOS transistors were fabricated simultaneously with detector diodes on high-resistivity silicon. The only additional steps required for the transistor fabrication consisted of the growth of a 36.5nm gate oxide in steam at 800C followed by the chemical vapor deposition of polysilicon at 610C to form the gate of the transistor. The source/drain regions of the transistor are self-aligned to the gate to minimize the gate to drain overlap

capacitance [22].

In order to determine directly the effect of this additional processing on the detector properties, detector diodes were fabricated on the same substrates. This was accomplished by using a mask aligner which steps nine separate 1 cm^2 fields. Five of these fields were devoted to the transistor array and the other four contained the diodes described previously. The polysilicon and gate oxide were completely removed from the diode fields prior to boron doping, which simultaneously formed the source/drain regions of the transistors and the top contact of the diode.

Figure 4 shows typical output current-voltage characteristics of a p-channel MOSFET fabricated on 10 $k\Omega \cdot cm$ silicon. The channel width and length for this device are 26 μm and 5 μm, respectively. Due to the high-resistivity material the devices behave normally even with a large bias (100V in Figure 4b) applied to the substrate as has been reported earlier [23]. The change in device threshold voltage due to the substrate bias is proportional to the square root of substrate doping [22] and hence is very small in this case.

The I-V characteristic of a p-i-n diode fabricated on the same wafer is shown in Figure 5. The leakage current is on the order of 1–3 nA/cm^2, comparable to the results shown in Figures 2 and 3. Hence no significant degradation in the detector diode properties result from the additional processing necessary to fabricate p-channel transistors. The fact that the devices were processed at 900C for nearly 3 hours while maintaining low leakage current is significant and offers the prospect that CMOS or JFET circuits can be integrated directly with the detector on high-resistivity silicon.

Figure 6 shows the response of a detector fabricated on <100> silicon to an Americium 241 source [24]. The full width at half maximum for the 59.4 KeV gamma ray is approximately 1.7-1.8 KeV yielding an energy resolution of approximately 3%, which is limited by the noise of the signal-processing electronics.

4. Conclusion

A silicon detector process has been developed that is compatible with standard IC processing. Extrinsic gettering of lifetime-killing impurities yields leakage current densities in the range 1–3 nA/cm^2 at depletion region thicknesses of 250–300 μm. Gettering allows processing temperatures consistent with typical IC fabrication, and reduces the sensitivity of the process to detrimental impurities. The additional processing necessary to fabricate p-channel MOSFETs did not significantly degrade the detector leakage current. Hence, the effective use of gettering provides a path to integrating readout electronics on the same substrate with the detector diode with potentially high fabrication yields. It remains to be seen if variations of this technique can be applied to devices which require junction formation on both sides of the wafer such as the silicon drift chamber [2]. However, good gettering results have been reported using a patterned silicon nitride film [25] thus offering hope that drift chambers and other two-sided devices could also benefit from gettering.

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Figure captions

Fig 1 The fabrication process used in this work.

Fig 2 The detector diode reverse-leakage current for a device with backside gettering compared to one without. The devices were fabricated on 10 kΩ · cm<100> substrates, and both devices are from the same wafer.

Fig 3 The detector diode reverse-leakage current for a device with backside gettering compared to one without. The devices were fabricated on 1 kΩ · cm<111> substrates, and both devices are from the same wafer. For the gettered device the surface leakage current has been suppressed by biasing an MOS capacitor located between the diode and guard ring at -5V.

Fig 4 Current-voltage characteristics of a p-channel MOSFET fabricated on 10 kΩ · cm silicon. The transistor gate oxide thickness is 36.5nm, and the channel width to length ratio is 26 μm/5 μm.

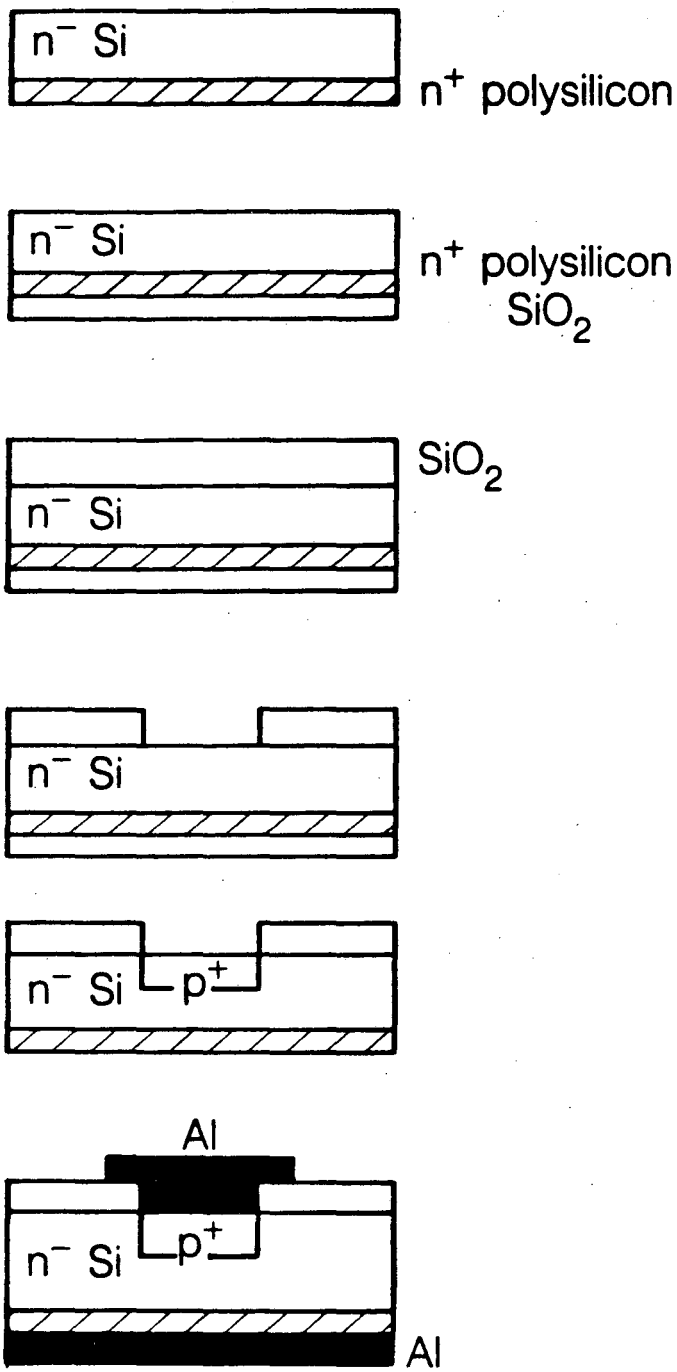
(a) Zero volts substrate bias.

(b) 100 volts substrate bias.

Fig 5 Detector diode reverse-leakage current of a device fabricated on the same substrate with p-channel MOSFETs.

Fig 6 The response of a detector fabricated on <100> silicon to an Americium 241 source. The peak at lower channel numbers is the detector response to the 59.4 KeV gamma ray whereas the peak at higher channel numbers corresponds to a voltage pulser applied directly to the input of the preamplifier. The full width at half maximum is approximately the same for both implying that the detector response is dominated by the noise in the signal processing electronics. The diode bias was 30V

and the integration time was 0.8 microseconds. The counting period was approximately eight hours and the measurements were performed at room temperature. The sensitivity is approximately 0.026 KeV per channel.



(1) Deposition of in situ-doped polysilicon on the backside

(2) Deposition of silicon dioxide on the backside

(3) Thermal oxidation

(4) Photolithography and etching of the silicon dioxide

(5) Boron doping and removal of backside oxide

(6) Aluminum metallization

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Fig. 1

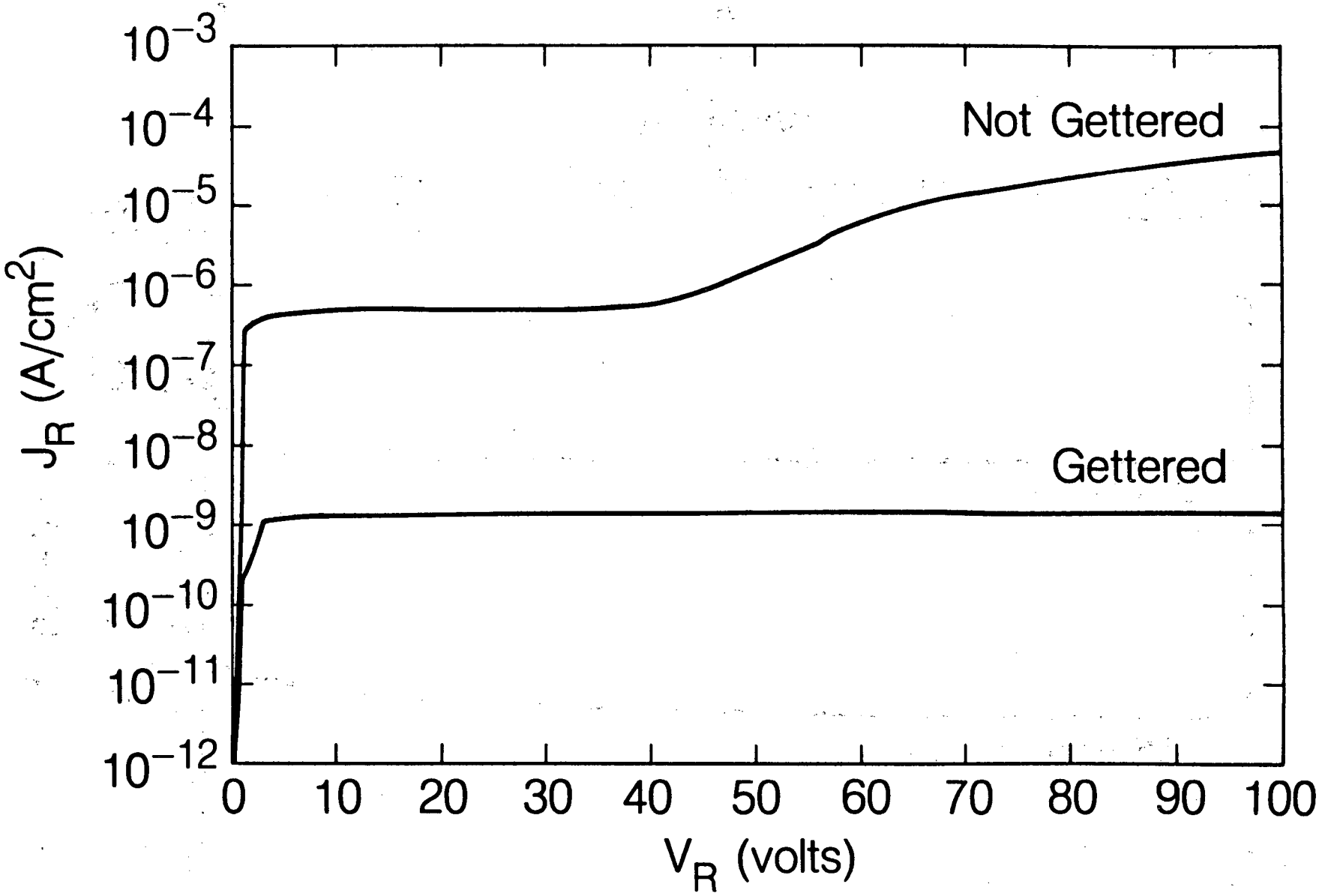

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Fig. 2

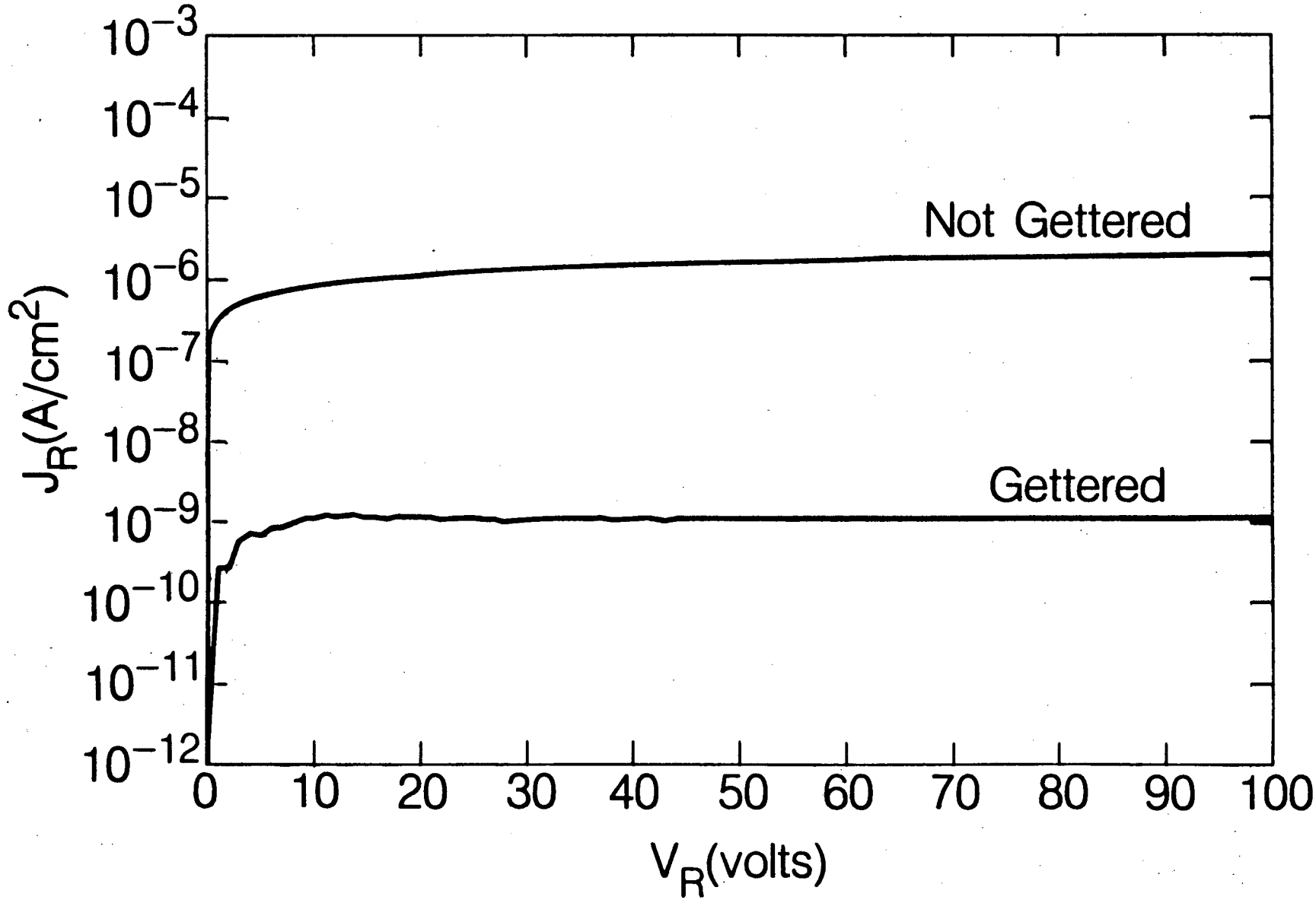

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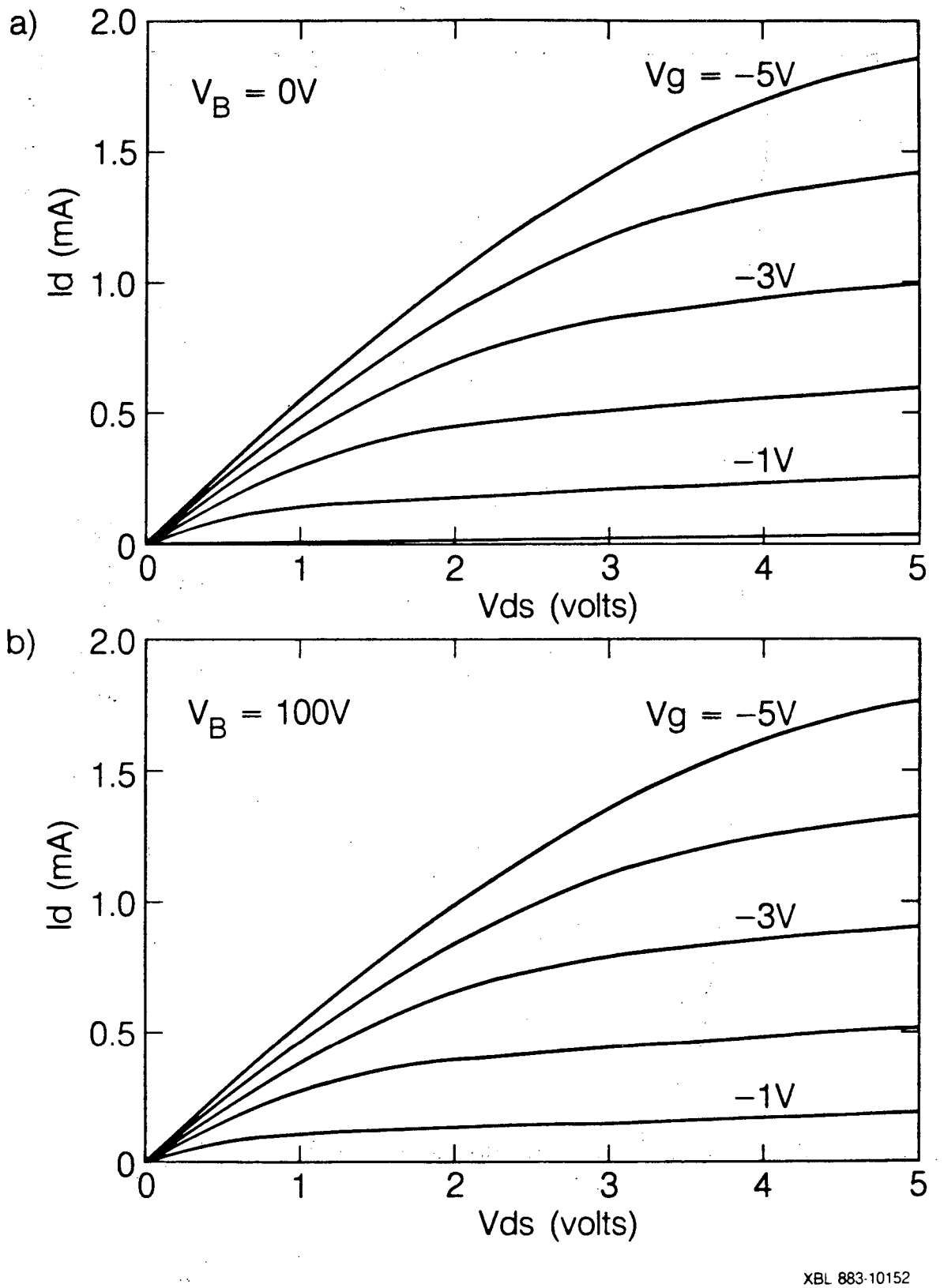
Fig. 3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Vg = −5V
−3V
−1V
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1.5
1.0
0.5
0
0
1
2
3
4
5
Vds (volts)
b)
V_B = 100V
Vg = −5V
−3V
−1V
Id (mA)
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1
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Vds (volts)
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Fig. 4

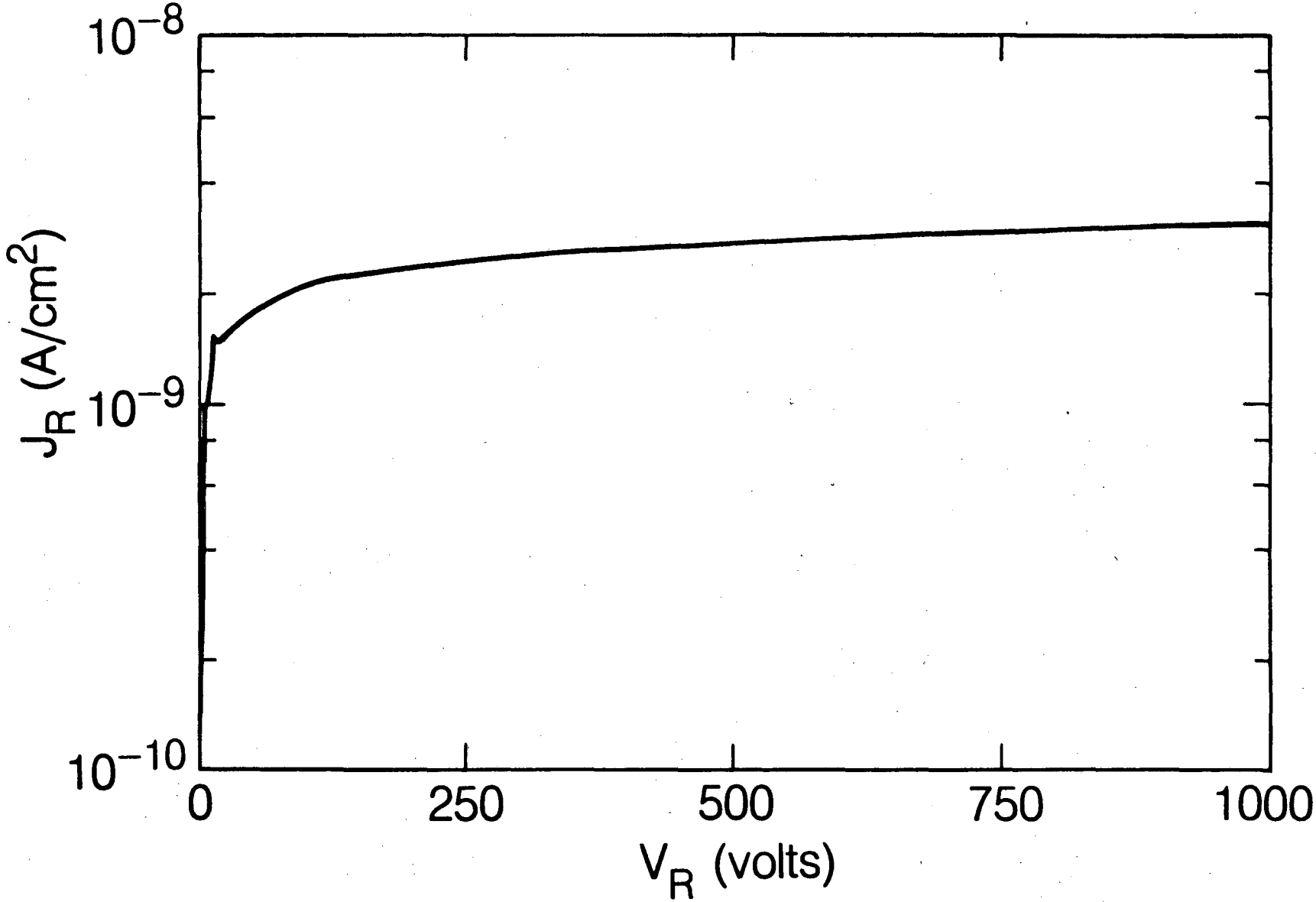

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Fig. 5

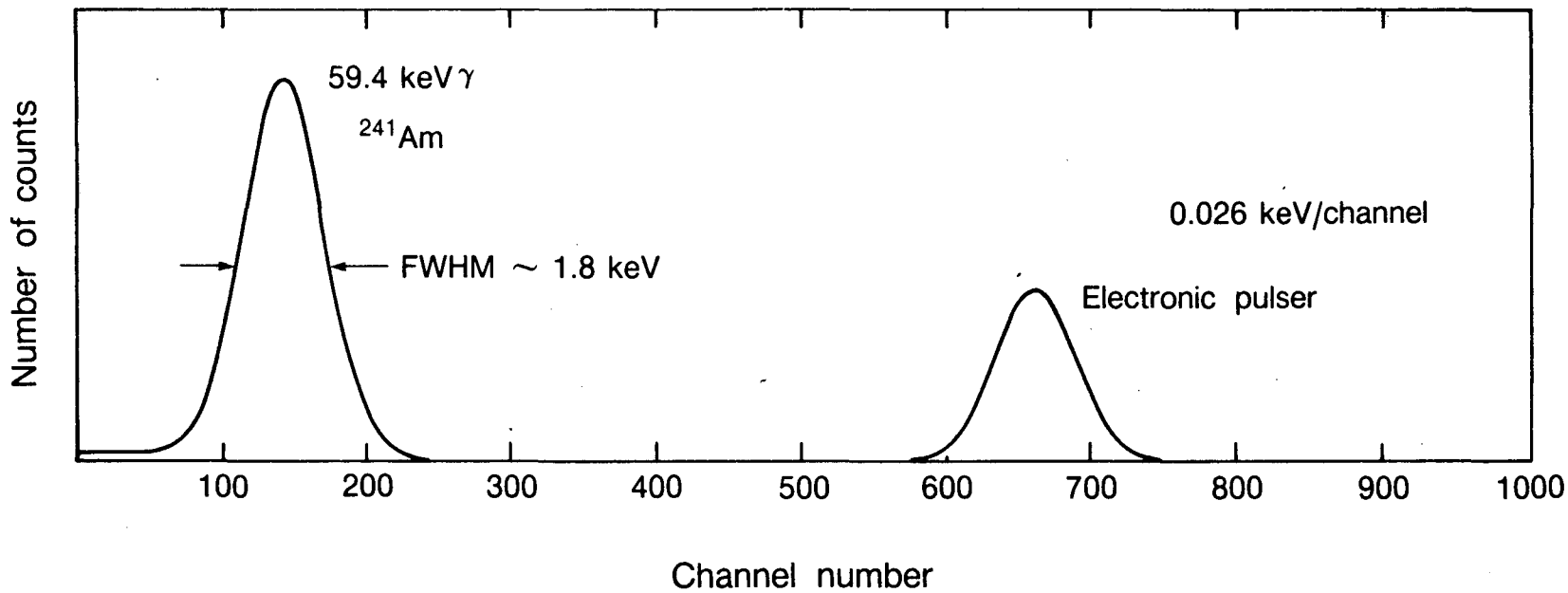

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Fig. 6

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