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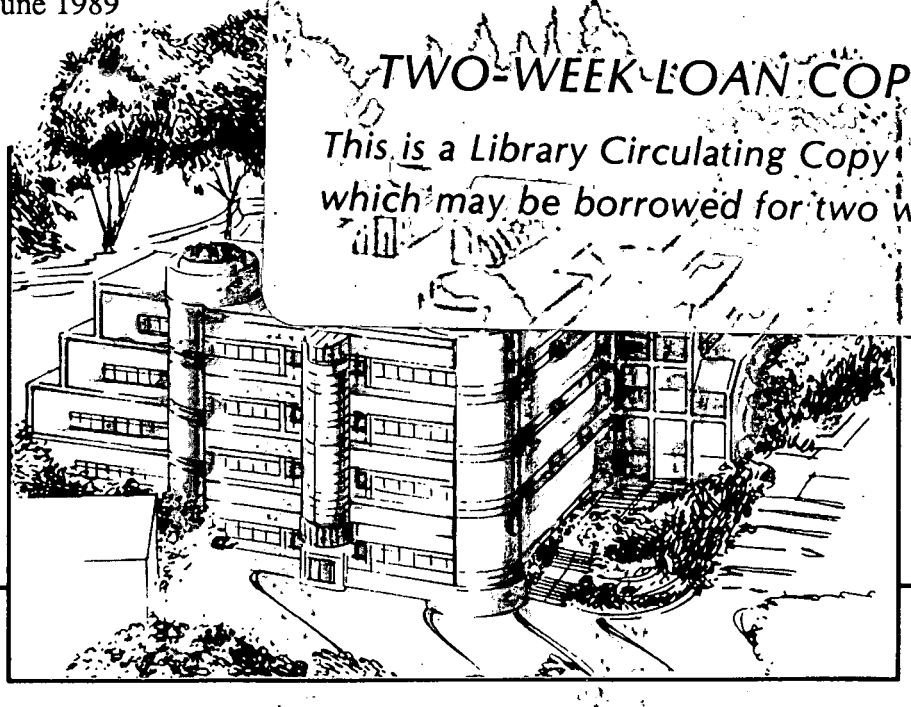

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CHARACTERIZATION OF GaAs/Si/GaAs HETEROINTERFACES

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ABSTRACT

Transmission electron microscopy of GaAs grown on Si for metal-semiconductor-metal photodetectors is presented in this paper. Two kinds of samples are compared: GaAs grown on a 15 Å Si epilayer grown on GaAs, and GaAs grown at low temperature (300°C) on Si substrates. It is shown that the GaAs epitaxial layer grown on thin Si layer has reverse polarity to the substrate (antiphase relation). Higher defect density is observed for GaAs grown on Si substrate. This higher defect density correlates with an increased device speed, but with reduced sensitivity.

INTRODUCTION

The motivation for this work was the desire to fabricate ultra-high-speed metal-semiconductor-metal (MSM) photodetectors. Optimum performance of such detectors requires a combination of high sensitivity with short minority carrier lifetime. In earlier work, neutron-damaged GaAs has been used in MSM devices [1,2], with sensitivity sacrificed for increased speed. Our approach was to use molecular beam epitaxy (MBE) to grow GaAs on Si substrates. The planar thin film geometry, in principle, allows good carrier mobility parallel to the GaAs/Si interface, while the expected high density of crystal defects at this interface should reduce carrier lifetime.

EXPERIMENTAL

Two different types of samples were grown in a Varian molecular beam epitaxy (MBE) system. In the first type of samples, a thin layer (15 Å) of Si was grown on a GaAs buffer layer grown on GaAs substrate, followed by a 1μm thick layer of GaAs. The thin Si epilayer was grown using a Si doping cell at a nominal temperature of 600°C, with a substrate temperature of 600°C. Growth of the final 1μm GaAs epilayer was initiated at 425°C at approximately 0.1μm/hr and slowly ramped up to 1μm/hr at 600°C. The second types of samples were prepared by growing low temperature (LT) GaAs epilayers on Si substrate at 300°C. All substrates were at nominal (001) orientation.

Cross-section samples of both types of material were studied using a JEOL 200CX electron microscope with a point-to-point resolution of 2.4 Å and the Atomic Resolution Microscope (ARM) at Berkeley with a resolution of 1.7 Å. In each case, cross-sections were examined with [110] and [100] parallel to the electron beam.

RESULTS

Transmission electron microscopy revealed many defects in the first type of samples, GaAs grown on Si (15 Å) deposited on epi-GaAs substrate (Figs. 1-3). Defect types and their density were similar to that in GaAs grown directly on Si substrates, e.g. misfit dislocations, stacking faults, microtwins and threading dislocations [3,4]. The number of stacking faults in the GaAs epilayer was much higher than in typical two-step growth GaAs layers grown on bulk Si, with typical spacings between stacking faults of 15nm.

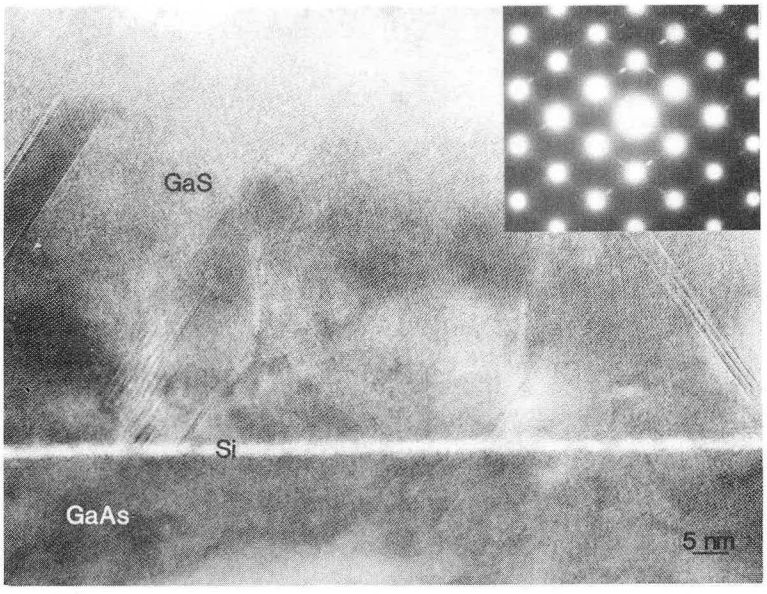

Fig. 1: High resolution image of the GaAs/Si/GaAs interface taken in <110> projection. Note high density of microtwins and stacking faults present in the GaAs epilayer.

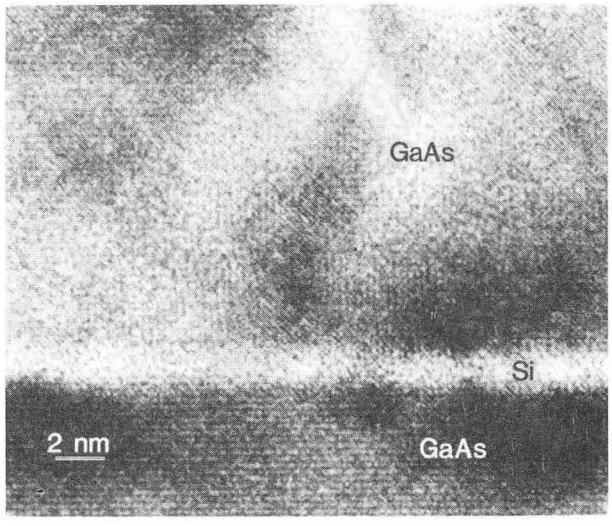

Fig. 2: High resolution image of the GaAs/Si/GaAs interface taken in <100> projection. Steps at both interfaces are visible.

Many antiphase boundaries were observed in these layers as well. To ensure that the observed contrast was associated with antiphase boundaries the sample was placed in a Phillips 400T electron microscope where convergent beam electron diffraction (CBED) patterns were taken in particular domains. The sample was tilted to fulfill the condition of coupling two odd reflections with the (200) reflection in order to observe the black (or white) cross in the (200) disc.

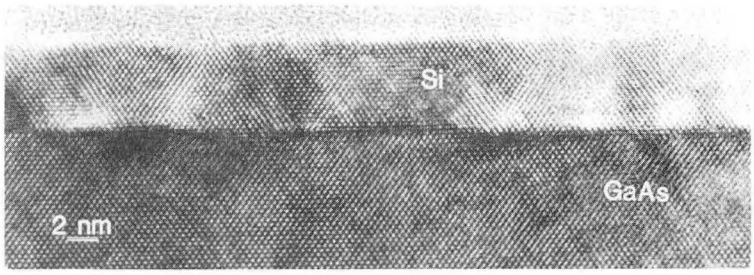

Fig. 3: High resolution image of the Si/GaAs interface taken in <110> projection. Thickness of the Si layer is ~ 6 nm. Note high density of stacking faults present in the Si epilayer and lack of pure edge type of misfit dislocations at the interface.

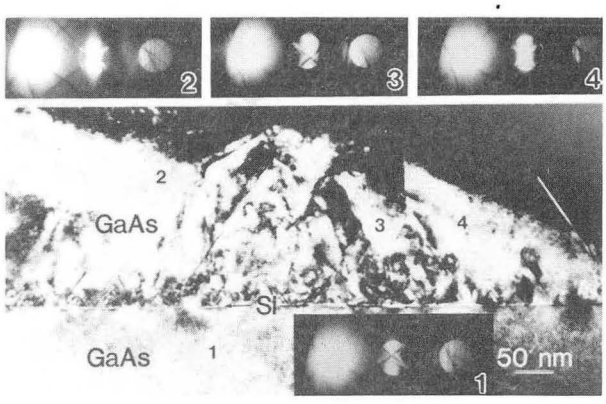

Fig. 4: Dark field image of the GaAs/Si/GaAs interface. Numbers 1, 2, 3 and 4 indicate the position of the electron beam where convergent beam diffraction pattern was taken in order to determine the polarity of the crystal. CBED patterns show the reverse polarity (see the crosses in the (200) disc) of the GaAs epilayer. Only the grain 3 has the same polarity as the underlying epi-GaAs.

This CBED method was previously successfully applied to check the crystal polarity [5,6]. A black cross was observed in the (200) disc in the GaAs buffer layer (Fig. 4 - beam position 1), which changed to white when the beam was placed in the GaAs epilayer above the Si layer (Fig. 4- beam positions 2 and 4). Only in a few places (beam position 3) was the polarity of the domain identical with that of the substrate. This observation shows a preferred GaAs-Si interface orientation which is consistent with preferential bonding of As to Si [7], although some domains have the same polarity as the underlying GaAs buffer layer. The defects in the final GaAs epilayer appeared to originate at the upper GaAs-Si interface. TEM revealed steps at both the GaAs-Si and Si-GaAs interfaces.

It is very difficult without image processing to decide if some misorientation of this thin Si layer took place, because the Si layer is visible in most cases only as a white band. This white band may be associated with impurities during growth or contamination during TEM sample preparation. When a 60 Å thick Si layer was grown, lattice imaging of the layer was very easy, and no white band was observed (Fig.3). This 60 Å thick Si layer was highly defective. Stacking faults with one partial dislocation at each interface were observed. This study shows that even when only a few monolayers of Si are grown, the differences in lattice constant and thermal expansion coefficient of Si and GaAs cause a high defect density in the top GaAs epilayer.

This GaAs-Si-GaAs structure was compared to low-temperature epitaxial GaAs heteroepilayers grown on Si. The latter had a high density of defects, mostly stacking faults, dislocations and antiphase domains (Figs. 5, 6). It was observed that any irregularities at the interface, such as surface contamination, could lead to the formation of small grains (polycrystalline material) and stacking faults (Figs. 6 and 7).

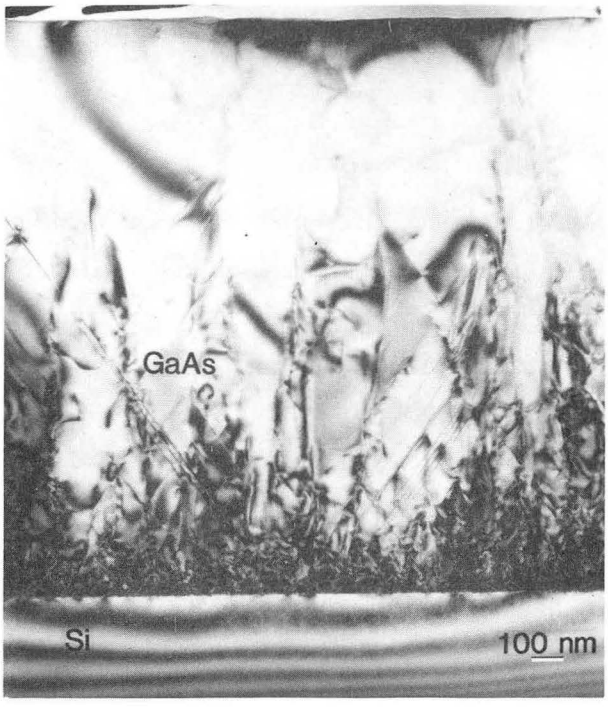

Fig. 5: Bright field image of GaAs deposited at 300°C (LT) on Si substrate. Note high density of microtwins, stacking faults and dislocations present in the GaAs epilayer.

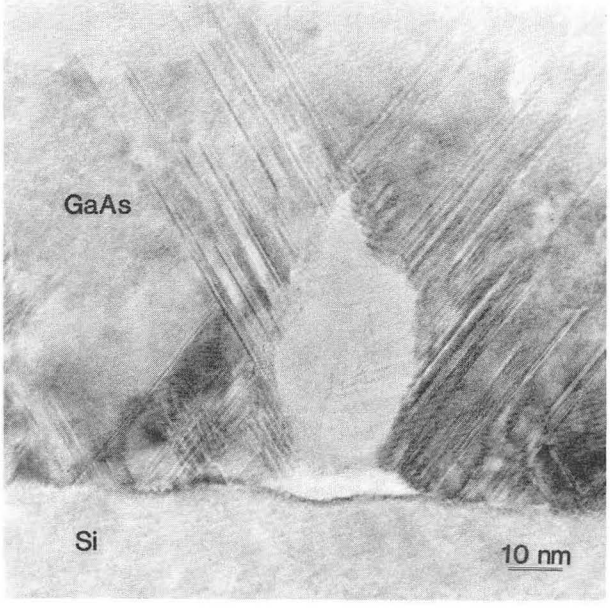

Fig. 6: High-resolution image of the GaAs (LT) on Si interface taken in <110> projection. Note that interface contamination is the source of polycrystallinity and other defects.

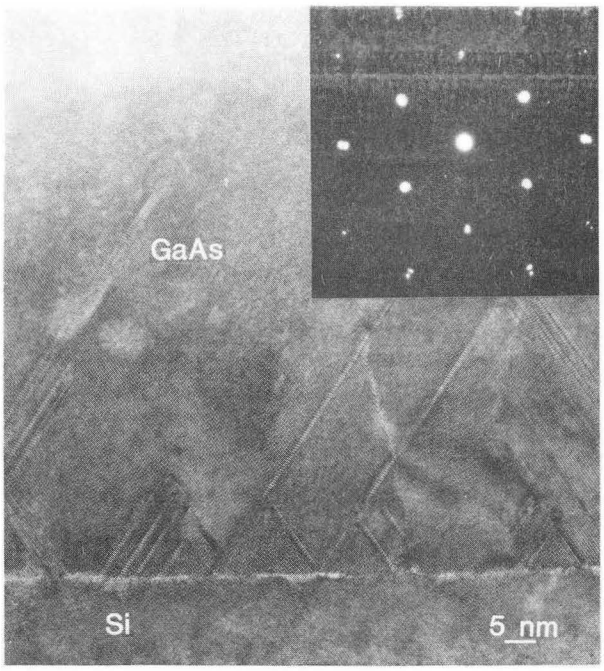

Fig. 7: High-resolution image of the GaAs (LT) on Si interface taken in <110> projection. Note lack of pure edge type of misfit dislocations at the interface.

Annealing of the LT-GaAs structures at 600°C did not reduce dislocation density significantly but drastically reduced stacking fault density (Figs. 8 and 9). It was observed that dislocations in postannealed samples were more tangled than in as-grown samples.

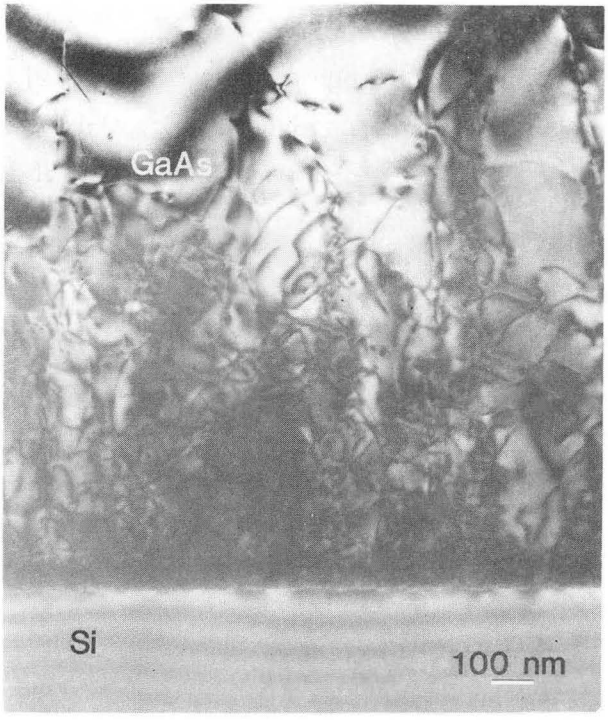

Fig. 8: Bright field image of the GaAs deposited on Si substrate at 300°C (LT) and annealed at 600°C with As overpressure. Note that density of microtwins and stacking faults drastically decreased, but many tangled dislocations are present in the GaAs epilayer.

Comparing these two types of materials, a higher defect density, especially close to the interface was observed for the LT GaAs grown on Si substrate. This correlated with an increased device speed but with very low sensitivity. MSM detectors on these epilayers showed autocorrelation response times under 50 ps [8]. The annealing step did not significantly effect the response time, but the relative sensitivity of the photoconductors increased significantly after annealing.

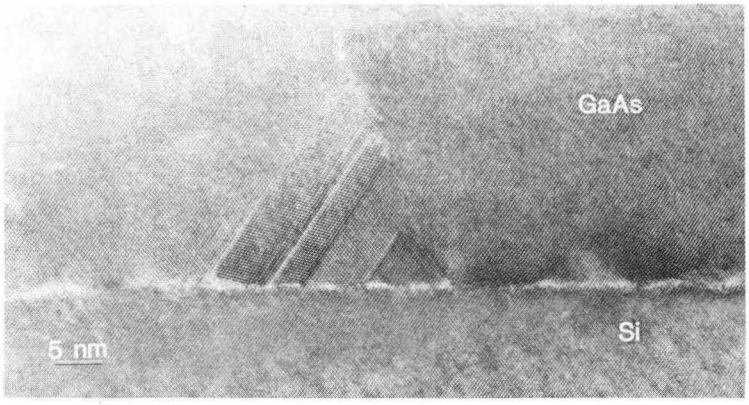

Fig. 9: High-resolution image of the GaAs (LT) on Si interface taken in <110> projection. Microtwins and stacking faults found at the interface only in some areas.

CONCLUSIONS

A study of the GaAs/Si/GaAs structures used for MSM detectors shows that the GaAs epilayer grown on 15 Å thick Si deposited on epi-GaAs substrate has reverse polarity to the substrate (antiphase relation), which is consistent with preferential bonding of As to Si. The number of defects formed in GaAs grown directly on a (001) Si substrate is high compared to the GaAs/Si/GaAs(001) structure, and this correlates with increased device speed.

Annealing at 600° C with As overpressure does not significantly reduce dislocation density or change the device speed, although it does increase the overall device quantum efficiency, which can probably be related to a decrease in the density of stacking faults.

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