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Front-End Electronics Development for the SSC

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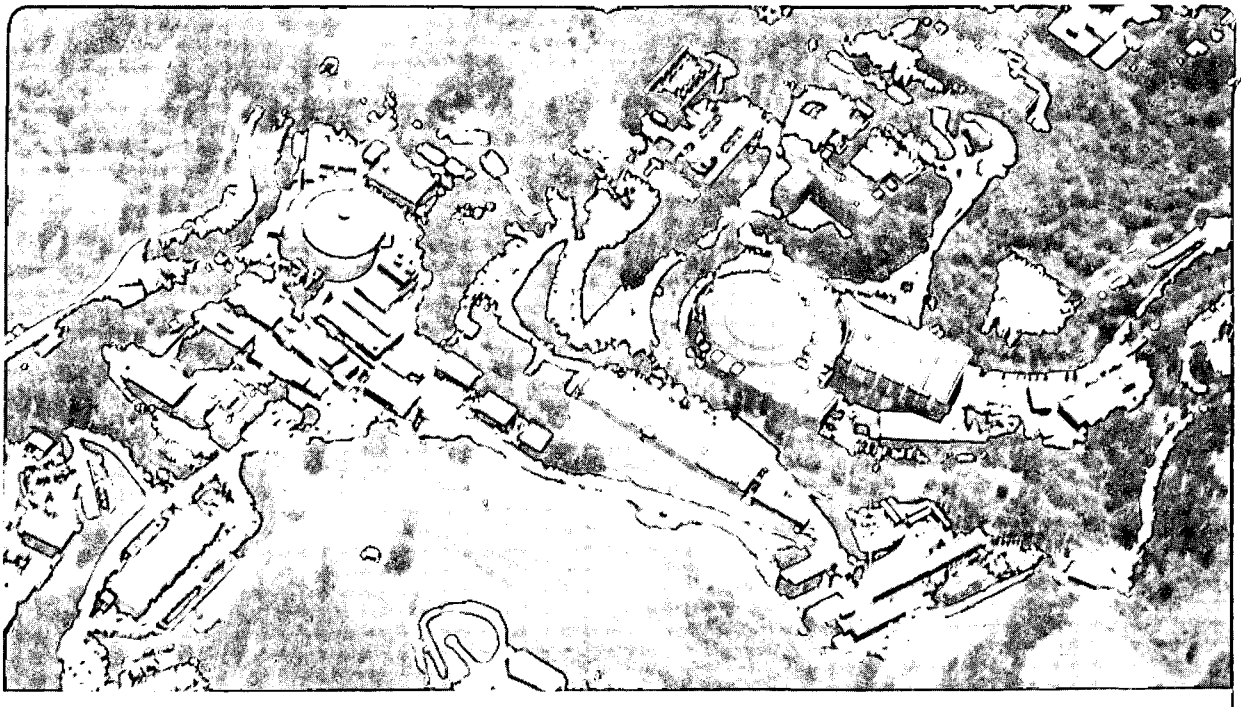

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FRONT-END ELECTRONICS DEVELOPMENT FOR THE SSC

Status Report on Electronics Development by the Front-End Electronics Collaboration

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FRONT-END ELECTRONICS DEVELOPMENT FOR THE SSC

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Abstract

This is a status report on electronics development undertaken by the Front-End Electronics Collaboration. The overall goal of the collaboration remains the development by 1992 of complete, architecturally compatible, front end electronic systems for calorimeter, wire drift chamber, and silicon strip readout. We report here a few highlights to give a brief overview of the work underway. Performance requirements and capabilities, selected architectures, circuit designs and test results are presented.

Introduction

The purpose of this project is to identify architectural and technical issues in the electronics designs for SSC detector front-ends. We have focused on issues that will significantly effect development and construction of the detectors. There remain significant issues where the success or failure of the research and development will alter the implementation of some of the detector concepts.

The electronics for signal detection and triggering for an SSC detector will be one of the most sophisticated electronics systems ever built by the high energy physics community. Signal processing must be performed on over one trillion analog samples per second. In comparison to previous experiments, at the SSC much larger sampling speeds, wider dynamic range, and larger channel counts are encountered and in the presence of significant constraints on power consumption, radiation hardness, and cost. Fortunately, high density CMOS and bipolar processes are available that can meet these challenges and provide the necessary signal processing power, signal shaping, analog to digital conversion and sophisticated addressing schemes including sparse or selective data readout and trigger buffering and selection.

In this report we will review the development efforts centered on: 1) architectural considerations and Level 1/Level 2 storage, 2) wire chamber drift time measurement, 3) liquid ionization calorimeter electronics, 4) signal shaping, 5) analog storage of liquid ionization or scintillator calorimeter signals, and 6) radiation hardness studies,. This work is a summary of the combined efforts of the Collaboration members.[1] Further discussion can be found in the Front-end Electronics Collaboration proposals.[1,2]

Architecture

One of the most important goals in the development of a front end electronics system for experiments at the SSC is the choice of an overall architecture which meets the requirements of all detector systems. While the characteristics of a particular detector may force minor variations in this overall architecture, the cost is likely to be minimized, and the reliability and ease of debugging optimized, if one can find an architecture which is nearly the same for all systems. It is in fact primarily for this reason that we included wire chambers, liquid ionization and scintillator calorimeters, cathode pad chambers, and silicon strip chambers within the scope of the overall front end electronics subsystem development.

The term "Front-end Architecture", is broadly used to describe the topology and functionality of the system of electronics that is physically located on the detector. In the case of an SSC detector, this includes a major portion of the total electronics system. The design of this portion includes the implementation, in integrated circuit form, of sophisticated components, including a complex system of data and control signals to "glue" these components into a cohesive system.

It is impractical (if not impossible) to move the data from every channel off the detector for every interaction. Usually, a trigger decision of a 1-2 μs latency is made to judge the value of the stored signals. These signals are then either discarded or digitized, processed, and transferred to computer systems. It is therefore desirable to filter the data through multiple levels of triggering. Thus, these systems usually require time delay via temporary storage of the signal to match the latency of the trigger and the bandwidth of the data processing system.

In the most likely scenario, data is stored during two successive levels of triggering prior to event readout. The architecture discussed could be utilized as well with a single trigger level if higher rejection factors are achieved with the Level 1 trigger or higher bandwidth of the readout is implemented. It is our judgement that for some systems and at the highest luminosities (e.g. > 10^{33}) it will be necessary to include Level 2 storage. In any event we have not yet identified any particular cost or penalty of including it other than a modest increase in circuit complexity.

Fig. 1 shows the basic organization of the data flow paths of the front end electronics. The portion above the dashed line - located on the detector - receives signals from the detectors, filters them with Level 1 and Level 2 triggers (trigger not shown), and delivers packets of digitized data off the detector for event processing.

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It is expected that two basic building blocks will be required - Front-end IC's (FE's) and data collection circuits (DCC's). Front-end integrated circuits accept signals directly from the detector elements, process and store the signals during the time necessary to form Level 1 and Level 2 triggers, and output digitized data selected by the Level 2 triggers. DCC's interface to a small data bus structure that interconnects a small number (e.g. 16) of FE's. They control the collection of digitized data from the FE's, and organize it for transmission off the detector.

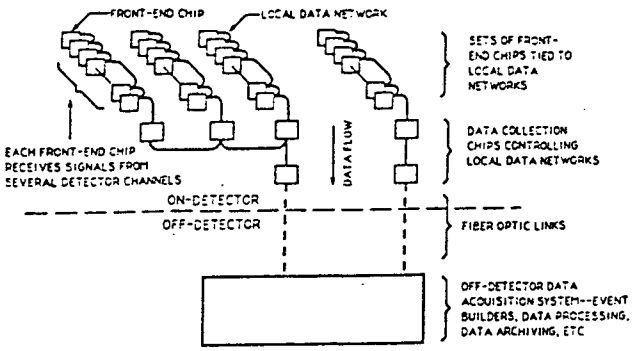

Fig. 1. The basic organization for the data collection scheme. The front end IC's (FE's) accept the signals from the detector and the Data Collection circuits collect the data from a set of FE's and prepare it for transmission.

Given the desire for Level 1 and Level 2 storage, there is still a broad range of possibilities. The various solutions may be distinguished by:

1. The Level 1 and Level 2 storage buffers are physically distinct.
2. The Level 1 and Level 2 storage buffers are not physically distinct, but only distinguished by address pointers (virtual pipelines).
3. Both the Level 1 and Level 2 storage are digital.
4. Both the Level 1 and Level 2 storage are analog.
5. The Level 1 storage is analog, but the Level 2 storage is digital.
6. The transfer from Level 1 to Level 2 occurs within a bunch crossing (16 nsec).
7. The transfer from Level 1 to Level 2 is buffered.

All these possibilities have been considered in our study of architectures. However, we are not pursuing a system in which Level 1 is digital with high priority since the utilization of 62 MHz ADC's implies rather large power dissipation and is not generally applicable throughout the detector subsystems. In addition for very high density systems (such as silicon microstrip detectors) there is insufficient space.

One of the simplest approaches is to transfer the information stored in Level 1 to Level 2 as soon as a Level 1 Accept for that particular crossing has been received. Since one may need to transfer information on subsequent crossings, either because another Level 1 trigger was received or because it is desirable to read out the data from several crossings for a given Level 1 trigger, the transfer must be accomplished in 16 nsec. This then requires a rather fast amplifier. To understand how much power is required for such a transfer, an operational amplifier was designed in a 1.6 micron CMOS process. A single stage folded cascode was used to enable maximum speed at minimum power. The conclusion is that even with a relatively advanced process, it requires approximately 4 to 5 mW to obtain bandwidths of 230 - 250 MHz at restricted dynamic range. These bandwidths are still not sufficient. Therefore this approach was abandoned (at least temporarily) in favor of a system incorporating either virtual pipelines or buffered Level 1 to Level 2 transfers.

In summarizing each of the investigations, we considered separately "data driven" systems which naturally sparcify the data and are appropriate for low occupancy detectors, and systems in which sampling is performed regularly every 16 nsec as is likely to be used for the calorimeter readout.

Besides these specifications, we have followed several other considerations in developing the architecture. We have tried to design a system with inherently low power consumption. This means that fast analog-to-digital (ADC) data conversion is avoided. We want to minimize the number of digital control lines connecting the front end circuit with the trigger and DAQ system. We therefore have avoided centralized bookkeeping that forces us to move information between the trigger system and the front end.

We are also constrained by the practical considerations of implementing sensitive low-noise analog circuitry on the same chip where a significant amount of fast digital logic is occurring. We note that because of the asynchronous nature of the system, where one can have data being digitized at the same time that analog data is being recorded or transferred, the potential for noise pick-up is much more severe than earlier collider environments. We have therefore tried to reduce the total number of fast signal lines in proximity to the front end IC's. Other ways of reducing noise pick-up would be the use of low-voltage differential signals with slow risetimes. This drives us toward a system with as few components (and functionality) as possible in the front end.

Clock Driven Architecture

In the case of a clock-driven system, the simplest conceptual system is shown in Fig. 2. The data enters a FIFO in which the data is moved in synchronization with the machine RF. The FIFO is then a clocked analog delay element for the Level 1 trigger. At the end of the Level 1 delay, the data enters a Level 2 FIFO, now clocked by the Level 2 trigger decisions. Data which corresponds to events successfully satisfying a Level 2 trigger are then digitized and passed to the Level 3 trigger along read-out fibers.

As an alternative to this arrangement, with only a slight overhead in terms of complexity, is to leave the data in the storage element it is deposited in and use a pointer system to label data according to its Level 1, Level 2, or read-out status. The data does not move but remains in the same storage element until being digitized or discarded (overwritten). Since the order of Level 2 triggers in the storage array is not necessarily in any sequence, a scheme for keeping track of which trigger belongs to which storage element must be implemented. This "virtual pipeline" architecture, shown in Fig. 3, makes maximal use of the fact that Level 1 and Level 2 decisions are taken in order

(monotonic). The primary objective is to minimize power requirements and produce a read-out architecture with minimal dead-time.

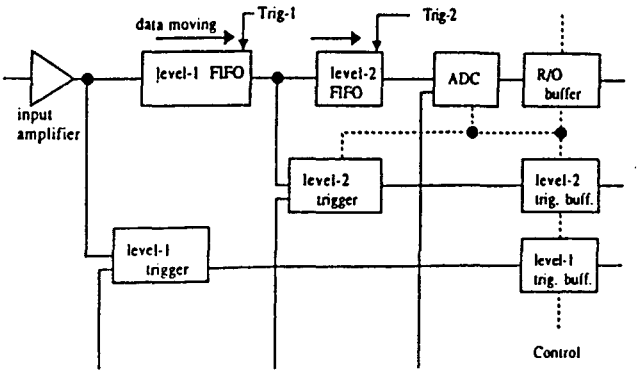

Fig. 2. Simplest Analog Front End

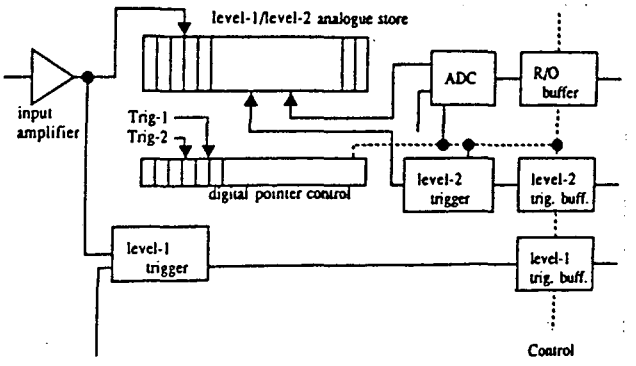

Fig. 3. Single Analog Store, Pointer-Address Architecture

It is also inherent in this scheme that there is not a one to one correspondence between a particular Level 1 or Level 2 address and a particular storage location. A significant consideration is the fact that, unlike the scheme of Fig. 2, there is a potential need for calibration constants for each cell in the storage array. Hence it is very desirable that the variations in gain and offset between the various storage locations be sufficiently small that they may be ignored. This is a very desirable goal for any system utilizing analog storage.

Data Driven Architecture

The case of data driven storage folds in another layer of complexity to each of the stages presented in the clock-driven schemes. The potential advantage is that considerably less data need be stored.

The technique is to record only when there is data present. An input pulse which exceeds an input threshold causes the data to be stored, along with a number recording the RF bucket to which the data belongs. Since both data and address must be stored this architecture is applicable only to low occupancy channels.

In spite of the greater complexity, calculations suggest that data-driven systems become clearly advantageous when the channel occupancy is less than ~ 10^{-3}. At higher occupancies a more careful consideration of the specific trade offs becomes necessary.

The number of buffers in the Level 1 storage, Level 2 storage, and the readout FIFO depend on the occupancy of the detector the front end IC is designed to read out, the Level 1 and Level 2 trigger latencies, and the Level 1 and Level 2 trigger rejection rates. Our model assumes that the occupancy is relatively low ($< 10^{-3}$), although a similar architecture would probably work for a device that is not data-driven or that has high occupancy.

Throttling the Data Flow

In the data-driven scheme, the prevention of data corruption due to the overflow of buffers or bandwidth must be performed on-chip, since the trigger system itself has no way of knowing how many buffers are available to process data pending Level 1 and Level 2 accepts. When the data-processing capability of the front end is insufficient, some data loss is unavoidable.

It is possible to have situations where the amount of Level 1 storage is inadequate to handle all of the signals from the channel. Although the number of buffers should normally be sufficient to avoid this problem, one can imagine scenarios where this could occur. One obvious case is that of a relatively "warm" channel that has an occupancy of 30% or more. In this case, the amount of data that could be generated is vast, far exceeding the internal bandwidth of the chip. To handle such cases, it is probably necessary to provide some mechanism by which the entire channel can be disabled, by for example providing a bit that would disable the signal from the comparator. However, there are several places in the chip where some additional control must be provided.

Several overflow conditions must be detected:

1. If a flood of data comes in, the first problem will be that all of the available Level 1 storage buffers will become full.
2. The Level 2 FIFO may become filled.
3. A similar problem exists in the readout FIFO, though we believe that it can be made fast and deep enough to take whatever data rate the Level 2 digitization can produce.

Loss of data is automatic in only the first two situations. It would be preferable to signal those cases where loss of data might have occurred. This can be accomplished by signaling these different error conditions to the data acquisition by inserting the necessary error information into the data stream.

Drift Chamber Electronics

For a high precision drift tube or straw tracking system, it is necessary to accurately measure the time of arrival of the first electron at the anode. While many possible schemes exist for making this measurement, our initial judgement was that an inherently analog measurement scheme would offer both lower power and greater resolution than an equally complex digital system. In addition, we realized that it would be necessary to incorporate all of the desired system features (connection to trigger and DAQ

systems, for instance) in any usable design in order to keep power and mass of the final system under control.

The minimum set of specifications necessary for a successful time measuring device would seem to be:

- < 0.5 ns time accuracy, ~ 0.2 ns time resolution
- Deadtimeless operation
- High rate capability
- Local storage of data during the trigger decision

In the straw tube tracking systems being proposed for SSC, each straw tube sensor will require a preamplifier, shaper, discriminator, time converter and sparsification unit. Analog bipolar technology offers optimal performance tradeoffs for the preamplifier, shaper and discriminator. It's high gain-bandwidth at low power is unmatched by any other commercially available technology as is the noise performance for shaping times of less than 20 ns and the matching of the control voltage between transistors. CMOS technology offers significant power advantages for functions such as analog memory and digital logic when operating below 100 MHz. For the time conversion and sparsification blocks, it is clearly the technology of choice.

Measurements with Straw Tubes

Under the *Generic Research* program we have developed a fast, low power and low noise monolithic preamp and shaper based on design goals suitable for a proportional drift tube tracking detector at SSC.[3] A prototype version was fabricated in the AT&T ALA200 Semi-Custom bipolar process. The design is based on a cascoded common emitter preamplifier configuration requiring only a modest supply voltage of 3 to 4 volts. The power dissipation is therefore relatively low.

The shaper has one zero matched to cancel the dominant pole of the preamplifier and three equivalent integrations that limit the bandwidth and maintain pulse symmetry. The pulse symmetry realized by use of multiple pole shaping is demonstrated in Fig. 5.

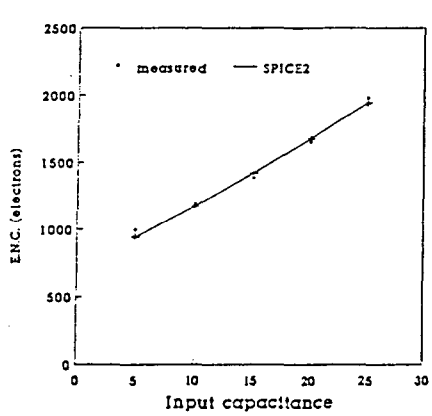

Fig. 4. Comparison of simulated and measured noise levels for a 5 nsec peaking time.

The intrinsic amplifier noise, shown in Fig. 4, is primarily determined by the size of the input transistor and it's quiescent current. In the design stage, the noise performance was optimized for an amplifier with a pure detector capacitance of 5 - 10 pF. The quiescent current was set to about 0.5 mA and an input transistor of 75μm emitter length was used to achieve a base resistance of about 15Ω.

Fig. 5 shows a signal in a 2 meter prototype straw tube at Indiana University due to a cosmic ray. The waveform in this figure shows the output of the prototype amplifier when attached to a passive detector tail cancellation network. The signal that extends beyond the 5 ns measurement time creates a *detector tail* that must be compensated or cancelled in high rate systems. The detector tail is eliminated by adding a set of poles and zeroes to the shaping function.[4]

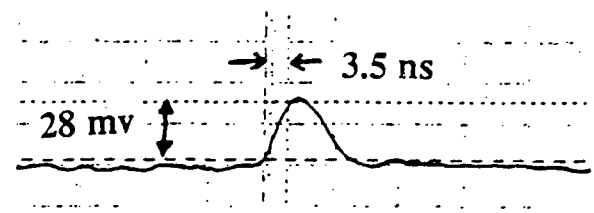

Fig. 5. Signal from a 2 meter straw tube filled with CF^4. The waveform shows the output of the prototype amplifier attached to a detector tail cancellation circuit. The scale from this digitizing oscilloscope is 10 nsec/div on the abscissa, and 20 mV/div on the ordinate.

Time to Voltage Converter/Analog Memory

We have implemented in CMOS a data driven architecture which is suitable for wire chamber readout (and could be extended to silicon microstrip detectors). The circuit includes a time-to-voltage converter (TVC) needed to convert the output of the preamp/shaper to a drift time measurement. This required the development of threshold discriminators, and an analog comparator.[5,6] The block diagram of the TVC is shown in Fig. 6. The accuracy of the TVC is shown in Fig. 7.[7] In the design of the prototype time-to-voltage converter/analog memory unit (TVC/AMU), we have limited the number of Level 1 analog memory locations to eight, which should suffice given the necessarily modest occupancies of any viable tracking system. A block diagram of the TVC/AMU is shown in Fig. 8.

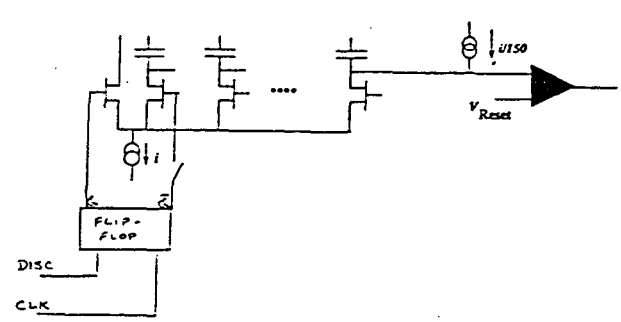

Fig. 6. TVC block diagram.

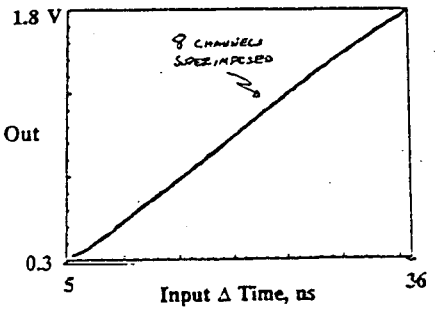

Fig. 7. TVC output voltage vs. input time difference with 8 independent channels superimposed. In scale shown 1 ns = 50 mV.

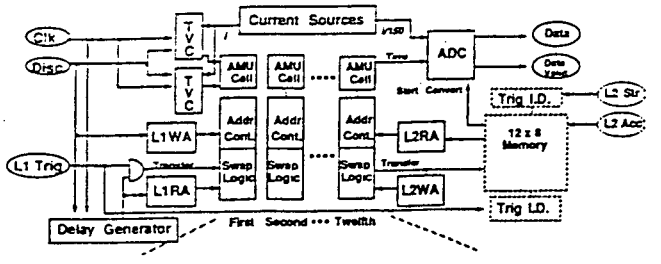

Fig. 8. TVC/AMU block diagram.

Additional control logic is included in the circuit to implement the data driven architecture, including logic to manipulate Level 1/Level 2 buffers, and time stamp information required to retrieve the data.

The system consists of

- A circular Level 1 storage buffer, containing both an analog memory and storage for a relatively small (~ 4-bit) local bunch counter (LBC). This buffer stores all data pending a Ll trigger decision.
- Two Level 1 storage write and read address counters (LlWA and LlRA).
- A Level 1 Read Address FIFO (LlRF) with a depth of about 4 elements and a width of order 15-20 bits. This feature effectively buffers the Ll-L2 transfers and allows for a relatively low bandwidth analog transfer without increasing the deadtime of the system.
- A circular Level 2 storage buffer, providing storage for analog data and ~ 10 bits of digital data and consisting of order 5-10 locations.
- Two Level 2 write and read address counters (L2WA and LlRA).
- An ADC that will digitize the data associated with events passing the Level 2 trigger.
- A digital readout FIFO of up to 5-10 elements.

Each storage location consists of an analog memory and a 4 bit digital memory, which will store the value of a local bunch counter (LBC). The LBC counter is incremented at each beam crossing and wraps around itself (the number of bits for this counter is determined by the maximum number of crossings that need to be read out for each Ll trigger).

Given the non-deterministic nature of a data driven architecture, it will be necessary to include in each data packet a crossing identifier. The simplest time stamp, would be a crossing counter - advancing every 16 nanoseconds. However, for Level 2 storage times of 50 μs or more plus realistic DAQ pipeline delays of many tens of microseconds, a 13 or 14 bit crossing counter would be necessary in order to avoid ambiguity. Instead, a more robust scheme should be implemented, with much longer unambiguous periods. Here, only the Level 1 trigger Accepts are counted. Even at 10^5 Hz an eight bit Trigger I.D. Counter would remain unambiguous for 2.5 ms.

In the case of multiple samples per trigger, it is necessary to have a small two to four bit counter, enabled by Level 1 Trigger, and clocked by the crossing clock, to completely specify the time. This counter is enabled by Level 1 Trigger true and counts until Level 1 Trigger goes false.

Simulation Studies of Front End Architectures

The front-end and data acquisition architectures we have been considering are sufficiently complex that their overall system behavior is difficult to predict without detailed simulations of the various components. This is particularly true in our case where the front end architecture alone is quite complex. A component of our R&D effort has therefore involved the development of behavioral models of the various front end architectures. This effort is particularly relevant to the task of defining the interfaces between the front end, trigger and data acquisition (DAQ) systems. Our initial task was a detailed gate-level simulation of the prototype TVC/AMU chip.

We have started the development of a comprehensive behavioral model of the front end system using the Verilog software package as the platform for this simulation. The first task was the development of a model for the signals generated by the trigger system, as those form one of the primary inputs to the front end chip. We have also developed a model for the output of a wire chamber discriminator, which forms the other primary input to the front end chip, as the initial thrust of this work has been to model a wire chamber readout system. We have implemented a model of a wire chamber readout chip employing the buffered Ll-L2 transfer scheme, using as input the simulated trigger and wire chamber signals.

We have tried to define a "minimal" interface between the front end system and the trigger and DAQ systems. One proposal for the trigger interface consists of the set of signals as described:

- **L1 Synch** that signals to the front end when a Level 1 decision is available (can be generated from the system clock); and
- **Ll Accept** that communicates the Level 1 trigger decision for that crossing.
- **L2 Synch** that signals to the front end when a Level 2 decision is available for the next Level 1 trigger still waiting for a Level 2 decision; and
- **L2 Accept** that communicates the Level 2 decision for the next unprocessed Level 1 trigger.

These signals appear to be the minimum set of signals necessary between the trigger and the front end chip. They assume that the Level 1 trigger is synchronous, with a

decision for a crossing becoming available a fixed number of crossings later. They also assume that the Level 2 trigger is monotonic (the next Level 2 trigger decision is always made for the earliest Level 1 trigger still to be processed), and is asynchronous, i.e. the Level 2 trigger decision is available a variable number of crossings after the Level 1 trigger.

This scheme has several advantageous features: for example, it is not necessary to propagate an event ID flag at each Level 1 or Level 2 trigger as the front end chip is responsible for generating this information.

We have assumed that the digitized information after a Level 2 trigger is "pushed" to a data collection circuit (DCC) where the data from several chips are collected and formatted into a packet that is then transferred via the DAQ to the Level 3 system.

An example of the information provided by this simulation is shown in Fig. 9, where we show the occupancy distributions of the Level 1 buffer, Level 2 buffer and the Level 1 read FIFO for this system with the following system parameters:

- A Level 1 acceptance rate of 0.1%, with a delay of 60 crossings.
- A Level 2 acceptance rate of 2.0%, with a gaussian Level 2 decision time distribution with mean of 500 crossings and a width of 500 crossings. The minimum separation between Level 2 decisions was 0.1 μs.
- A channel occupancy of 0.05 hits/crossing with a pulse width of 20 ns.

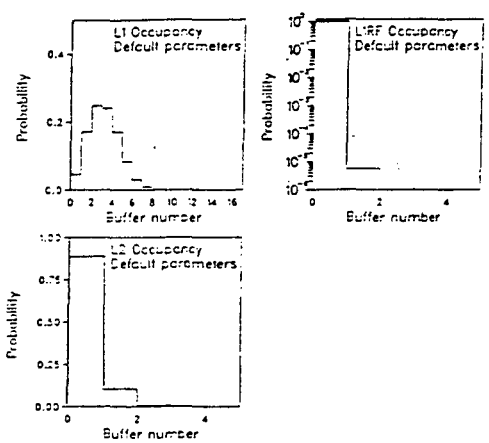

Fig. 9. The occupancies of the Level 1 buffer, the Level 2 buffer, and the Level read address FIFO in the Verilog simulation. Parameters of the simulation are given in the text.

The simulation employed 16 Level 1 buffers, 4 Level 2 buffers, and 4 buffers in the Level 1 read FIFO. On each Level 1 accept, any hits occurring within 3 crossings of the Level 1 accept were transferred to the Level 1 buffer. A Level 1 to Level 2 transfer time of 100 ns and a Level 2 to DAQ transfer time of 100 ns was assumed (neither of these are necessarily realistic). The Level 1 occupancy shows a mean of ~ 2.7 hits, which is in good agreement with the naive calculation when one takes into account the 20 ns pulse width included in the simulation. The mean occupancy of the Level 2 buffer is ~ 0.1, which is also in good agreement with the naive calculation. There was essentially no loss of data due to Level 1/Level 2 buffer overflow conditions. However, preliminary studies with this simulation have shown that the actual loss of data due to buffer full conditions grows more rapidly than the loss calculated if one assumes that the buffer occupancies obey Poisson statistics. This is a result of the delays involved in the Level 1/Level 2 and the Level 2/DAQ data transfer.

Although the parameters of this simulation are not representative of all of the expected features of the circuit or the trigger system, they illustrate the information that is available from such a behavioral model.

Analog Signal Processing for Calorimetry

The basic components of the signal processing chain for scintillation and liquid ionization calorimetry are depicted in Fig 10. The components comprise:

1. Preamplifier and charge calibration system.
2. Data recording chain, with additional gain (x 1 and x 64), first and second level buffer (analog "pipeline") and multiplexed readout.
3. Trigger forming chain, with additional gain, summing amplifiers, fast pulse shaping.
4. Control circuits for calibration, sampling, memory and multiplexing.

Analog sums of signals from large sections of the calorimeter will be formed for trigger purposes. These will result in a much smaller number of fast outputs, of the order of 1-3 x 10^3, for which more sophisticated shaping circuits may be employed. Several integration times (e.g., 50, 100, 150 nsec for ionization calorimeters and 16-48 nsec for scintillator calorimeters) may be used, so that pileup and electronic noise can be minimized for different experimental conditions.

The data recording chain contains memory units required to store information until Level 1 and Level 2 trigger decisions. The data are initially stored for each sample taken at 16 nsec intervals. None of the known techniques for analog storage and for fast analog to digital conversion can cover the large dynamic range required (15 to 17 bits), due to thermal noise limitations. Thus at least two data storage channels per signal channel with overlapping scales are needed, each covering 11-12 bits.

Preamplifiers are followed by two fast amplifiers with different gains, indicated as x 1 and x 64 in Fig. 10, which drive the memory units. The impulse response from the detector electrodes to the preamplifier output may have a rise time of no less than about 40-50 nsec, for ionization calorimeters, due to the charge transfer time from the electrodes to the preamplifier. For scintillator calorimeters the peaking time might be as short as 16 nsec though 32-48 nsec is more likely to allow adequate integration of the current from the calorimeter. In order not to increase further the response time of the system, the fast amplifiers should have a rise time of less than about 15 nsec.

The fast amplifier response, together with the charging time constant of the memory unit, provides sufficient band limiting at high frequencies to satisfy the Nyquist criterion.

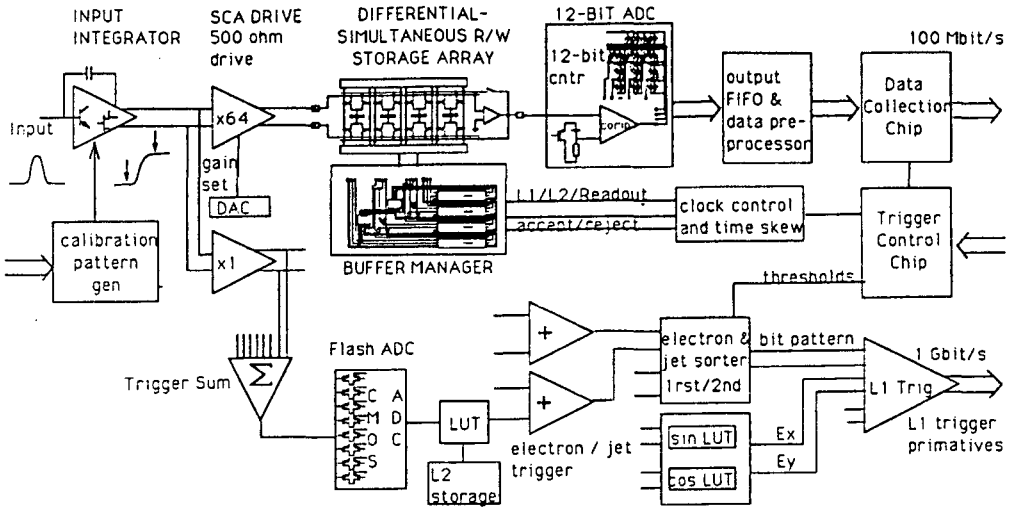

Fig. 10. Calorimeter front-end block diagram

Low frequency cutoff may be realized in the preamplifier and additionally in the fast amplifier, to provide a short enough decay time in the response that the pileup in any single channel does not restrict the dynamic range. Thus no elaborate pulse shaping would be performed prior to the memory. The actual optimal shaping for a given counting rate will be realized as a weighted sum of a number of samples. This shaping should be programmable so that the pileup and the electronic noise could be minimized for a particular experiment. This type of signal processing is equivalent to pulse shaping by conventional time invariant circuits. A wide range of weighting functions can be realized.

Preamplifiers for Ionization Calorimeters

Charge preamplifiers for ionization chamber calorimeters must have a low noise, a short response time and a low power dissipation. In addition, their apparent input resistance created by the feedback should be within a certain range to provide an aperiodic transfer of charge in the presence of inductance in the connections between the detector and the preamplifier. One of the most difficult requirements is a very large dynamic range. In the electromagnetic part of the calorimeter the dynamic range will be at least 2×10^4 and may be as high as 10^5. A linear response over a large dynamic range requires certain currents and voltages resulting in a high power dissipation. It appears that a power dissipation in the range between 75 and 200 mW is necessary depending on the type of capacitance matching. For liquid argon, the preamplifiers should be able to operate immersed in the liquid for optimal signal to noise and minimum charge transfer time.

The input amplifying device should have the device time constant C_{fet}/g_m as short as possible (<0.5 nsec), the equivalent series noise resistance should be close to the theoretical value ~ 2/3 g_m, and the parallel shot noise should be negligible. Junction field-effect transistors satisfy all these requirements. However, their optimum operating temperature range with respect to noise is 120 K<T<300 K. Development of devices which could operate at ~ 90 K (directly in liquid argon) is being pursued in collaboration with industry (INTERFET Corp., Garland, TX.).

Monolithic JFET Preamplifier Processing

A monolithic preamplifier using exclusively n-channel diffused JFET's has been designed and is now being manufactured by INTERFET Co. (Garland, TX) by means of a dielectrically isolated process which allows preserving as much as possible the technology upon which discrete JFET's are based.[8]

The new technique will still allow the use of an epitaxially formed channel and a diffused gate, as in standard JFET processing. The epitaxially grown lattice is free of defects created by ion implantation which only in part can be annealed.

Dielectric Isolation Method

Fig. 11 depicts the basic steps needed to achieve dielectric isolation. A standard slice of the needed resistivity is first oxidized and then patterned through a photoresist process. The slice is then etched by means of an orientation dependent etching process to form "V" grooves which will achieve electrical insulation. Another layer of oxide is then applied followed by a polysilicon grow to fill the grooves and to build up a thickness comparable to the original wafer. The slice is then turned over and most of the original silicon is lapped away until the tips of the V-grooves are exposed. This results in single crystal silicon islands ("tubs") isolated by silicon oxide and supported by a thick polysilicon substrate. A single layer of n-type epitaxial silicon is grown over the dielectric insulation substrate and provides a uniform channel of controlled thickness for the JFET.

Planar Process:

If a standard planar process is used with multiple tubs, adjacent JFET's will be connected by back-to-back diodes and

a high value resistor due to the polysilicon bridge as in Fig. 12. This should not cause isolation problems except perhaps increased noise in the input device.

"Mesa" Isolation:

If true isolation is needed, V-grooves can be etched to leave a free-standing "mesa" of silicon on a silicon dioxide base. Metallization across this groove to connect devices on adjacent "mesas" may degrade the yield, so it may be better to use the simpler planar process.

Double Epitaxy and V-Groove Isolation Method:

This method utilizes an n-type silicon substrate on top of which a p-type layer for the back gate and an n-type layer for the channel are epitaxially grown. Next, V-shaped grooves are etched deep enough to reach into the n-substrate thereby separating the back side gates. A true isolation is not achieved with this method since adjacent devices are connected by back-to-back diodes through the common substrate.

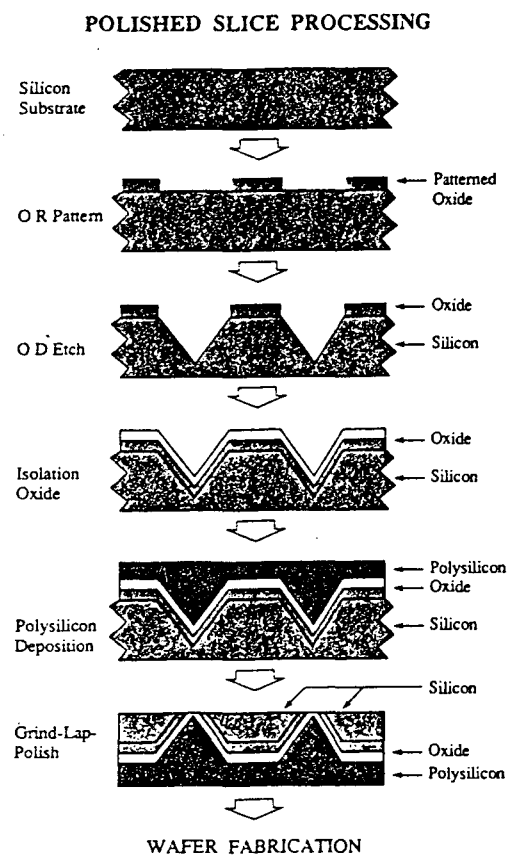

Fig. 11. Dielectric Insulation Wafer Fabrication. A silicon slice is first oxidized. After patterning, anisotropic etching is used to produce the "V" grooves which will become the barriers between circuit elements. Oxide and polysilicon are successively grown over the entire surface. The slice is then flipped over and most of the original silicon is lapped away until the tips of the V-grooves are exposed. This results in isolated single crystal islands ("tubs").

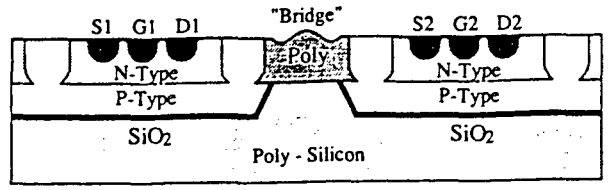

Fig. 12. Dielectric Isolation Process. Devices built in adjacent "tubs" are connected by back-to-back diodes in series with a high value resistor due to the polysilicon bridge shown above.

First Experimental Results

Up to the present only a preliminary silicon lot using the double epitaxial method has been manufactured, packaged and delivered. This first lot was manufactured on available material, which has a higher *p*-epi resistivity (about 1 Ωcm, instead of the design value of about 0.01 Ωcm). This increases the gate spreading resistance in series with the back gate, thus degrading the noise performance.

Fig. 13 compares the g_m and g_m/I_d characteristics for a monolithic and discrete JFET of W = 11400 μm and drain-to-source spacing of 16 μm (corresponding to an effective gate length of about 5 μm). At higher currents (I_d >1.5mA) they are almost identical.

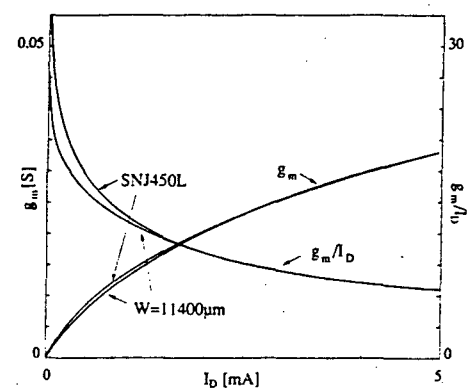

Fig. 13. Comparison of Discrete and Monolithic JFET's with L = 5 μm, W = 11400 μm.

Preamplifier Circuit and Experimental Results

An all JFET charge sensitive preamplifier has been manufactured in the dielectrically isolated process (see Fig. 14 for schematic). In applications with large capacitance detectors the input device J1 should be made as large as the production technology in order to take advantage of the better transconductance to current ratio attainable at low current density and reduce the noise at fixed current. For the prototype, a channel width W = 11400 μm, corresponding to an input capacitance C_{iss}~50 pF has been chosen.

The noise performance has been evaluated and is consistent with the additional gate spreading resistance in series with the back gate due to the low *p*-epi doping.

As soon as an improved version of the preamplifier is ready, it will undergo low temperature testing and evaluation

of its resistance to neutron and ionizing radiation as well to electrostatic discharge.

Both circuit performance and neutron resistance can be improved by reducing the channel length (and thus the active volume) of JFET's. A systematic study of the optimum doping levels in the channel region is necessary for the development of a JFET with optimum noise performance near liquid argon temperature (90 K).

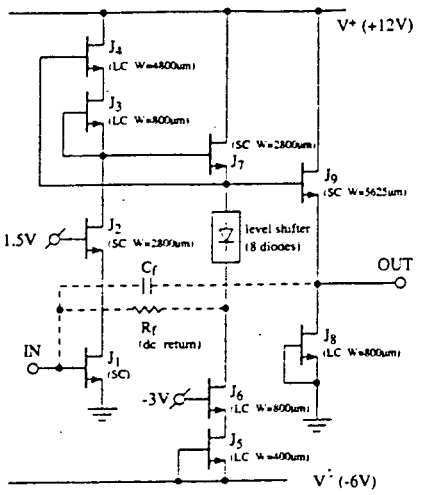

Fig. 14: Circuit Schematic of the JFET Charge Sensitive Preamplifier. SC: devices with short channel, L = 5 μm; LC: devices with long channel, L = 7 μm. The feedback resistor and capacitor (R_f and C_f.) are shown connected with dotted lines since they are outside the monolithic chip.

Voltage Programmable Shapers

As discussed above, calorimeter signals, as well as signals from other detectors, will require some form of shaping prior to analog storage. In principle, digital signal processing can be employed off-line to implement any desired weighting function, but even in this case, an anti-aliasing filter must be employed prior to analog storage. A more complete shaper implemented in hardware is however essential if one is to include the signals in a first or second level trigger. Off-line signal processing can still be used for enhancement of signal to noise ratio.

The challenge in design of integrated circuit shapers is to compensate for the process variations which inevitably occur in fabrication while maintaining good linearity over a wide dynamic range. The signal shape should be reproducible at the few percent level, while resistor and capacitor variations for even high quality bipolar processes are typically 25%. Various techniques for the design of externally programmable filters exist in the literature and are being studied for this application. MOSFET-C filters have been extensively described but it appears that they do not provide adequate linearity over the several volts of dynamic range required.

Translinear circuit techniques have been used for several decades in accurate analog multipliers, square and square root circuits and other analog function modules. These circuits utilize the accurate exponential current-voltage relationship of bipolar transistors explicitly to generate desired functions. We are investigating a new class of voltage programmable filters which utilize translinear circuit methods.

Our goal is to implement a bipolar pulse shape with a peaking time somewhere in the range of 75 to 150 ns for ionization calorimeters. For scintillation calorimeters, shapers of peaking time 32 - 48 nsec will be considered. For the bipolar pulse shape the required transfer function is composed of two differentiator sections and two integrator sections. The basic cell used to implement these functions consists of a resistor, a capacitor, and a current programmable current gain cell; a "Gilbert gain cell". The gain cell is used to provide Miller multiplication of the capacitor and therefore provide tuneability of the filter. In addition, the gain cell configuration is known to provide high linearity over a wide dynamic range. A bipolar implementation of the basic cell is shown in Fig. 15.

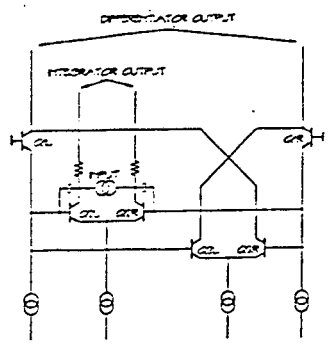

Fig. 15. Schematic of bipolar implementation of basic "Gilbert cell".

The gain of the cell is the ratio of the Q2 (and Q3) collector current to the Ql collector current and is externally programmable. Furthermore, the gain is constant for signals almost up to the limits of the bias current of the transistors. Cells formed in this way are fully differential and may be cascaded to form a variety of filter transfer functions. A bipolar pulse shape formed by two differentiators and two integrators is shown in Fig. 16 for several values of gain cell gain. We are doing detailed design work on this approach.

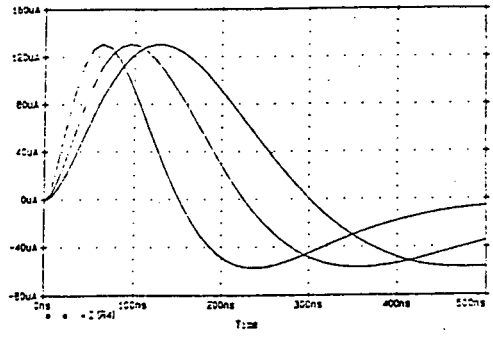

Fig. 16. Output pulse shape simulation of two differentiators and two integrators for several values of the "Gilbert cell" gain (i.e. different collector currents).

Level 1/2 Analog Storage for Calorimetry

The development of readout electronics for calorimeters is focusing on further refinements of the switched capacitor array (SCA) analog memory under development at LBL.[9] The analog memory will allow for the retention of data during the trigger decision.

The SCA circuit contains 2048 sample and hold cells subdivided into 16 parallel channels of 128 cells per channel. Each of the 16 channels has a dedicated analog input which is connected to a bus distributing the input signal to 128 sample and hold cells. Each sample and hold cell consists of a complementary CMOS transmission gate (complementary switch) and a 1 pF double polysilicon capacitor. An externally supplied reference voltage is applied to the bottom plate of all capacitors. The voltage stored on each sample and hold capacitor then corresponds to the difference between the input signal from a given channel at the time its sample and hold switches are opened and the applied reference voltage. The reference voltage can be adjusted to shift the baseline for better level matching.

An address decoder turns on and off sample and hold switches using a "break before make" action. During the readout sequence each sample capacitor is placed in the feedback path of the reconstruction op-amp. There is one reconstruction op-amp per channel. Before readout of each sample, stray charge on the signal distribution busses are cleared by shorting each amplifiers inverting input nodes and output nodes through a reset switch. This prevents charge remaining on parasitic nodes from the previous samples from influencing the next read out sample.

SCA Circuit Performance

Non-uniformities in the sample and hold elements limit dynamic range unless corrections are applied. The SCA readout scheme is not sensitive to capacitor values to first order, but non-uniformity of the sample and hold switches can be important, as the charge injection from these switches (due to gate to drain capacitance) will then vary. These switches are complimentary, and therefore the charge injection is canceled to first order, but variations still exist.

In order to achieve 12 bit dynamic range the pedestal variation of each of the storage elements in a channel must be less than one part in 4096 of the full scale voltage range. A channel operating with a full scale range of 4 volts would then require less than 1 mV of pedestal variation per element.

To achieve 12 bit dynamic range 8.3 charging time constants must elapse in each 16 nsec write operation to charge the sample and hold capacitors, this fast input bandwidth requires a large input charging switch. For increasing switch sizes the amount of parasitic charge injection from the switch will also increase. In the version tested, with a 2 nsec charging time constant, the cell to cell pedestal variation at a 50 MHz acquisition rate was 0.4 mV rms.

The measured incoherent noise on any given single cell when operated with a 62.5 MHz acquisition rate is less than 0.6 mV rms. Thus, the total dynamic range (single cell) could exceed 8000:1, or 13 bits. In previous versions of the IC the clocking noise feedthrough was well below one millivolt; however, in the current version inadequate separation of the on chip digital and analog power lines have increased the clocking noise feedthrough to several millivolts. The clocking noise is absent in a differential manifestation of the IC and is expected to be absent in the next corrected version of the IC. The measured parameters of the SCA are summarized in Table 1.

Table 1. Measured performance parameters of a simultaneous read-write switched capacitor array integrated circuit. Measurements were performed at a 50 MHz acquisition rate, but not utilizing the simultaneous read write capability.

Analog Store Parameters	Achieved Performance
No. channels/chip	16
No. of elements/channel	128
Power consumption/channel	23 mW
Non-linearity	+/- 0.9%
Cell to cell pedestal variation	0.3 mV rms
Charging time constant	2 ns
Channel dynamic range	4000
Maximum sample rate	90 MHz
Maximum readout rate	200 KHz
Noise floor	0.7 mV rms
Input voltage range	0.5-5.5 Volts
Capacitor droop rate	0.1 mV/msec
Output settling time (0.02%)	1.2 µsec
Gain variation from unity	+/- 1.5%

Operation of the integrated circuit has been verified on a sample of test pulses simulating the SSC calorimeter detector signals. Shown in Fig. 17 are a sequence of successively faster single cycle sinewaves, the pulses simulate the signals seen from the slowest to the fastest of the considered calorimeter detectors.

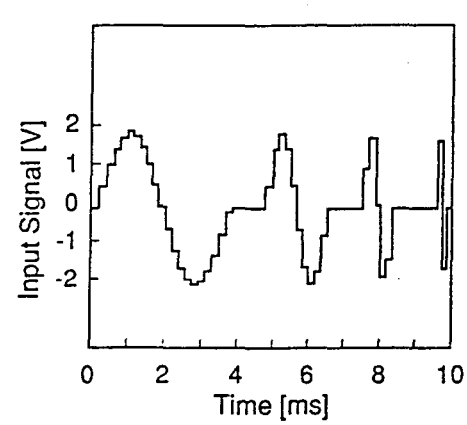

Fig. 17. Shown is the recorded input signal, 400, 200, 100, and 40 nsec period sinewaves of duration equal to the period. The SCA acquired this waveform while running at an acquisition frequency of 50 MHz.

Virtual Multiple Pipelines and the ALP

In the classical implementation of trigger delay pipelines, multiple physically distinct pipelines buffer data during multiple levels of trigger decisions. One principal problem is that the transfer of analog data with high dynamic range within 16 ns is extremely difficult and necessarily power consuming. The virtual multiple pipeline approach simulates the existence of essentially any number of sequential pipelines within one analog memory (SCA).[9]

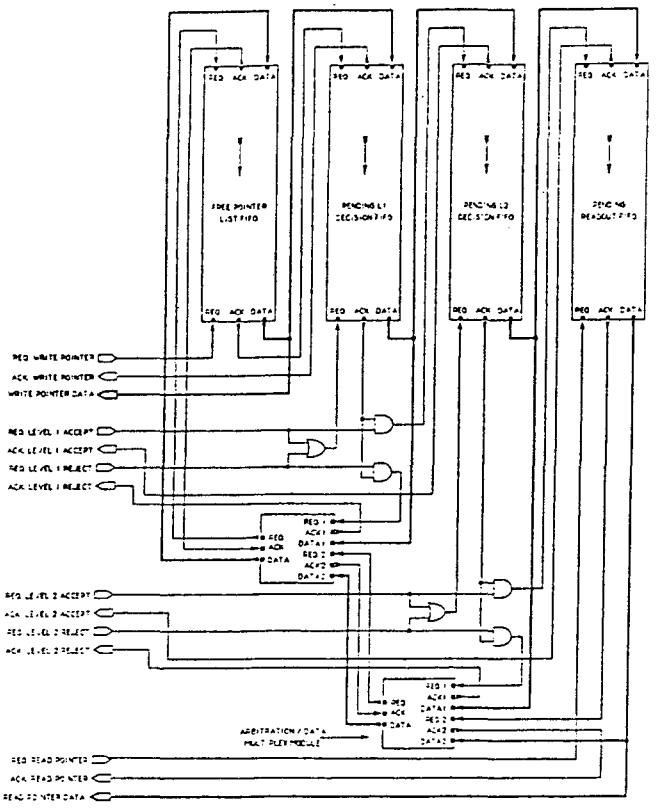

Fig. 18. Block diagram of the address list processor, showing the four FIFO memories for the address pointer lists for: unused cells, pending Level 1, pending Level 2, and pending read-out.

An address list processor (ALP) substitutes the movement of analog data with digital (the address of the analog data). The address list processor, presently in fabrication and shown in Fig. 18, contains four digital first-in-first-out (FIFO) memories. A prototype FIFO has already been fabricated. The four FIFO's contain addresses of SCA storage locations. The presence of a given address in a given FIFO indicates the state of the corresponding storage location. In this diagram, the four possible states are free (empty), pending Level 1 trigger decision, pending Level 2 trigger decision, or pending readout. With each beam crossing, a data word moves from the free list to the pending Level 1 trigger list. From there, data may move back on to the free list (on a Level 1 reject signal) or onto the pending Level 2 trigger list (on a Level 1 accept). From that list, the data may also move back onto the free list (on a Level 2 reject) or onto the pending readout list (on a Level 2 accept). The pending readout list buffers readout requests during the readout of prior events.

Radiation Effects on JFET's

The SSC poses the most severe test for semiconductor devices because of the anticipated high luminosity and confined geometry of detectors within the collider. We expect fast neutrons of about 1 MeV up to a few times $10^{12}/cm^2$ per year and up to 10 Mrad per year of ionizing radiation can be expected both within the central tracking region and in the calorimeter at the luminosity of $10^{33}cm^{-2}sec^{-1}$.[10] Fast neutrons produce displacements in the active detector volume which act as generation centers for excess leakage current. Photon interactions and most of the energy loss by very energetic, light, charged particles create ionization which leads primarily to surface effects at the interface of silicon and its passivating oxide. Radiation testing has been pursued on silicon detectors, on JFET's, on the AT&T CBC-U bipolar process, and on the radiation hard 1.2 micron CMOS process of UTMC.

Hybrid preamplifiers developed in the BNL Instrumentation Division are representative of analog components that would be at risk to ionizing radiation and can be studied conveniently. A set of BNL I0-535 single unit preamplifiers were exposed up to 1.45 Mrad of ^{60}Co at room temperature in air and the noise power spectrum was checked at intervals during the exposure.

Measurements were made over a range of amplifier shaping time constants; 100 pF was added to the preamplifier inputs to enhance high frequency series noise. Half of the preamplifiers were radiated with power on and half were not powered. Fig. 19 shows the increase of the noise in rms electrons (σ) after the irradiation, mainly for preamplifiers which were powered and at higher shaping time constants, suggesting a parallel noise source. The input JFET is an INTERFET 2N6451, which is guard-ringed,[11] and is expected to be reasonably tolerant to ionizing radiation. However, an unguarded 2N4416 is placed across the input as a protection diode and is a clear suspect. Fig. 19 shows that on removal of this diode, the noise in the powered devices returned to the pre-irradiation value. The effect power on is explained by the fact that under this condition some bias appears across oxides adjacent the channel, directing holes to the $Si\text{-}SiO_2$ interface forming interface states therefore charging the interface positively.[12] The fixed positive charge inverts the light *p*-diffusion, isolating the device (in the unguarded geometry), creating a parasitic leakage path and increasing the gate leakage current, the observed parallel noise source. In the unpowered preamplifiers, most of the ionization produced in the oxide recombined and little charge was directed to the interface.

Several preamplifiers from this experiment were annealed at 65°C and later at 120°C for periods of 1000 hours. In agreement with others, little improvement was noted at 65°C, but apparent full recovery was observed after the 120°C anneal. However, a small further increment of dose, 10^5 rad, returned the parallel noise to nearly its post radiation value. The 120°C anneal permits electrons from the

silicon to tunnel to the interface charge and neutralize it but does not substantially decrease the interface trap concentration.

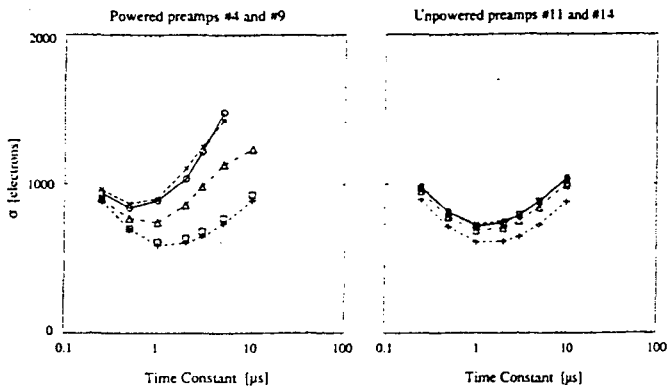

Fig. 19. The effect on observed noise σ (in rms electrons) of removing the protection diode from preamplifiers irradiated at room temperature with (at left) and without (at right) power applied. Legend: + = pre-irradiation, Δ = 0.5 Mrad, o = 1.1 Mrad, × = 1.45 Mrad with diode protection, ȯ = 1.45 Mrad without diode protection.

Powered and unpowered type I0-475 preamplifiers designed for operation in liquid argon were irradiated to 12 Mrad in a cryostat held at 120 K, and were also exposed to 10^{13} neutrons/cm^2 while under power and at ~120 K. A substantial increase in parallel, low frequency noise was observed only in the powered devices and a relaxation of the noise was observed when power was removed. Some increase in noise was observed at low frequencies. At pulse shaping times of 100 nsec or less, the noise increase was negligible.

Radiation Effects on Bipolar's

Measurements were performed on the degradation of bipolar transistors, particularly as characterized by decreases in the value of the current gain h_{fe}, after exposure of bipolar transistors from the AT&T CBC-U process to both neutrons and photons. The results are summarized in Fig. 20 and 21. Given a reasonably conservative design, circuits implemented in this process should operate after doses of 10^{14} n/cm^2 and up to doses of > 2 Mrads of ionizing radiation.

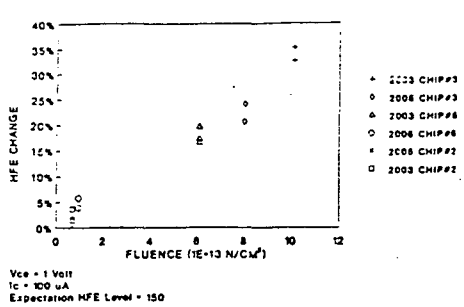

Fig. 20. Fractional decrease in current gain, h_{fe}, for npn transistors as a function of neutron fleuence.

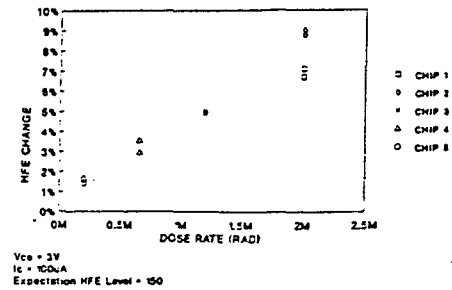

Fig. 21. Fractional decrease in current gain, h_{fe}, for npn transistors as a function of total dose exposure.

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