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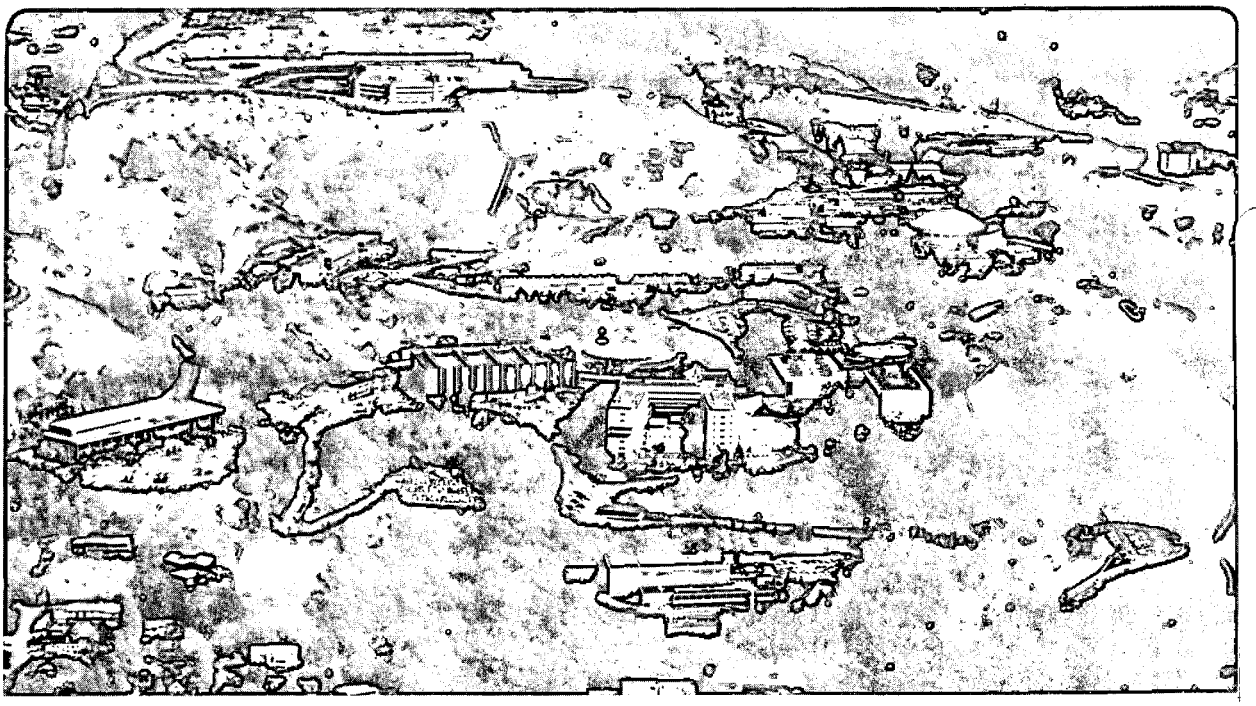

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High Speed Data Transmission for the SSC Solenoidal Detector

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Abstract

High speed data transmission using fiber optics for the Superconducting Super Collider solenoidal detector has been studied. The solenoidal detector system will consist of nine subsystems involving more than a total 10^7 channels of readout electronics. Consequently, a new high performance data acquisition system, incorporating high-speed optical fiber networks, will be required to process this large quantity of data.

I. INTRODUCTION

The Superconducting Super Collider solenoidal detector will consist of nine subsystems involving more than a total of 10^7 channels of readout electronics. This will require a new data acquisition system using high-speed optical fiber networks to process the large quantities of data from the detector subsystems. Also, extensive on-line processing must be used to reduce the amount of data per interaction and data rates to amounts that can be handled by present storage techniques and computing capacity.

The solenoidal detector system as planned will consist of the following subsystems: a silicon tracker having pixel and silicon strip detectors, a central straw-tube tracker, an intermediate wire tracker, a central calorimeter consisting of tower and strip subsystems, a forward calorimeter and a muon detector[1]. The muon detector will consist of a wire chamber and trigger counter units. The number of channels for each detector subsystem is summarized in Table I.

Table I
SSC Solenoidal Detector Summary

Detector Subsystem	Number of Channels
Silicon Tracker	
Pixel Vertex Detector	3.9×10^7
Silicon Strip Detector	8.5×10^6
Central Straw-Tube Tracker	188×10^3
Intermediate Wire Tracker	50×10^3
Central Calorimeter	
Tower Subsystem	41×10^3
Strip Subsystem	25×10^3
Forward Calorimeter	7×10^3
Muon Detector	
Wire Chamber Subsystem	108.4×10^3
Trigger Counter Subsystem	16.1×10^3

II. SYSTEM CONFIGURATION

A simplified block diagram of the proposed new data acquisition system architecture incorporating optical fiber networks is given in Fig. 1. The architecture of the system is based on a number of earlier workshops on triggering and data acquisition organized by the SSC Central Design Group[1,2]. The system will consist of the following subsystems: the detector front-end electronics using custom integrated circuits, an efficient high speed data collection and transmission system using fiber optics, a parallel event building network, special purpose processors for prompt triggers, calibration, and data compression, online processing units and a large data storage unit. Using an open architecture, the data acquisition system will be capable of processing data rates of several thousand Gbit/s from detector elements to the online processing subsystem. High speed data transmission will be implemented by optical fiber network consisting of optical transmitters, receivers and associated electronics.

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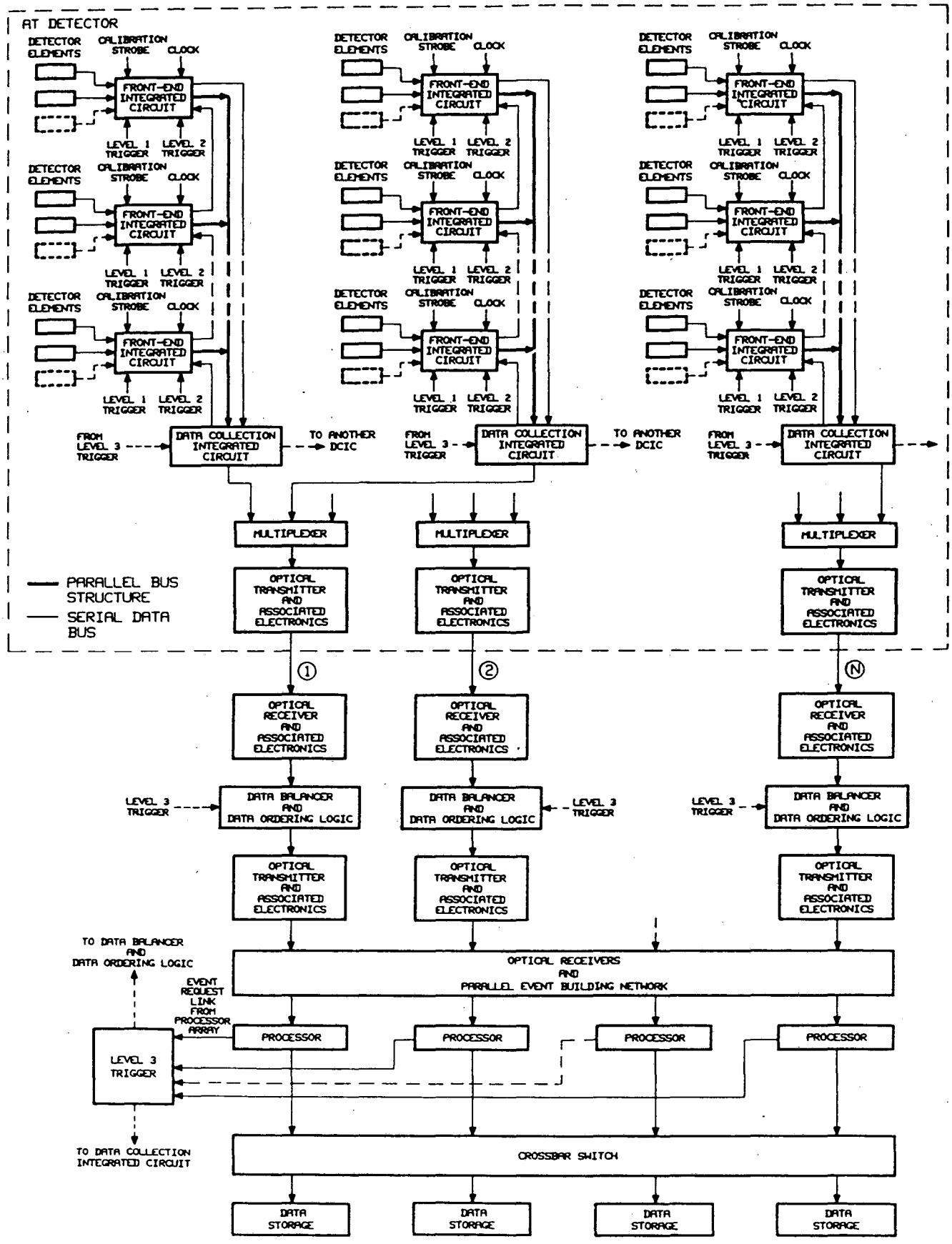

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Fig. 1 Data acquisition architecture for the SSC solenoidal detector.

The front-end integrated circuits accept signals from the detector elements and store these signals during the time necessary to process level 1 and level 2 triggers. Data collection integrated circuits collect the data from a set of front-end integrated circuits and prepare them for multiplexing[3].

As shown in Fig. 1, event data are transmitted, in parallel, over a large number of high speed serial fiber optic links. These links operate at typical data rates from 1 Gbit/s to 2.5 Gbit/s. The data balancer shifts multiplexed data into the different fiber optic links of the parallel event building network. The event building network simultaneously collects its input information from several detector channels. Also, the network simultaneously transmits totally built events to its multiple output ports. This makes possible the highest system throughput since all event data sources to the building network have similar amounts of data when averaged over a large number of events.

It has been shown earlier that the application of optical data transmission in the SSC data acquisition system will significantly increase its data rate capability, reduce electromagnetic interference and eliminate ground currents. Also, maintainability, hermeticity and reliability will be improved, because of the reduction of the cable plant size and simplification of the overall architecture[4-8].

Optical fiber networks will also be applied for the distribution of fast timing signals, such as the 60 MHz clock, the level 1 and level 2 triggers and calibration strobes. Outside the detector, optical fiber networks, incorporating subassemblies having low power dissipation, will be used for the high speed data transmission for data and control signals, and the interconnection of special purpose devices in trigger subsystem. For example, in the system shown in Fig. 1, the data can be transmitted from multiplexers to data balancers by means of 1000 parallel high speed fiber links. At present, a signal optical fiber data transmitting channel can operate with a data rate of 2.5 Gbit/s with a high reliability[9]. Consequently, the combined data rate capability of the system is 2.5×10^3 Gbit/s.

III. Design Considerations

The process of moving data from the front-end integrated circuits to optical transmitter is controlled by a handshaking protocol between front-end IC's and data collection IC's[3]. Data are organized in packets which include additional information such as time and location. The readout of data from front-end IC's is accomplished by connecting a group of these circuits to a single data collection IC using a local data network. As shown in Fig. 1, groups of data collection IC's can be assembled in a tree structure. The local data network consists of parallel and serial data bus structures. The parallel bus structure will be used to move event data packets, handshake control signals, and triggering/timing signals. The serial bus provides control information to front-end IC's. Furthermore, this bus also carries status information from the front-end IC's back to the control computer.

Processing capabilities of the data collection integrated circuit may be desirable for some detector subsystems[10]. Capabilities, such as pedestal subtraction, zero suppression, gain correction, data formating and feature extraction can significantly reduce the bandwidth necessary for the data acquisition system. Other tasks, such as monitoring, calibration and trigger functions, could be also accomplished by data collection circuits. Therefore, a communication link should be established between the level 3 trigger, generated by a processor array, and the data collection circuits, data balancers and data ordering logic. For a particular detector subsystem a cost/benefits ratio should be determined between the complexity of data collection circuit and benefits obtained by its processing capability.

A. High Speed Multiplexer Interface

A functional block diagram of the high speed multiplexer interface is shown in Fig. 2. This interface device is capable of operating with a serial data rate up to 2.5 Gbit/s and it is intended to implement the high speed data transmission systems. A Synchronous Optical Network (SONET)[11] may serve for this purpose.

The SONET transmission standard was developed by the American National Standards Institute in collaboration with industry. It establishes an international telecommunication protocol for optical digital data transmission. The basic SONET signal, having a 51.84 Mbit/s data rate, is comprised of digital frames each 125 ms long. The frame consists of the synchronous payload envelope containing the actual data to be transmitted and a part assigned for transmission of overhead information. The transmission overhead information is used to maintain the integrity of digital links and contains bytes for the frame boundary identification, data parity, channel identification and user specific functions. The frame is arranged in nine rows of 90 bytes each. In each row 87 bytes are reserved for actual data and 3 bytes for transmission overhead. The SONET standard defines a synchronous optical hierarchy to carry many different signals. This is accomplished by a multiplexing procedure resulting in a family of standards and formats which are integer multiples of the basic rate of 51.84 Mbit/s. The multiplier values are 1, 3, 9, 12, 18, 24, 36 and 48. Consequently, electronic circuits capable of operating up to 2,488 Gbit/s data rates are required. These circuits use gallium arsenide technology and a MOSFET process to obtain the required high speed with relatively low power dissipation.

The high speed multiplexer interface consists typically of a 8:1 multiplexer and a self-positioning timer. The multiplexer accepts eight parallel data inputs at rates up to 312.5 Mbit/s and multiplexes them into a serial bit stream output at rates up to 2.5 Gbit/s. The internal timing unit is designed to use a 2.5 GHz high speed clock. The parallel data inputs are clocked to on-chip input registers with an externally supplied ECL input signal operating at the same rate as the data inputs. An internal word clock is used to transfer the data to a set of buffer

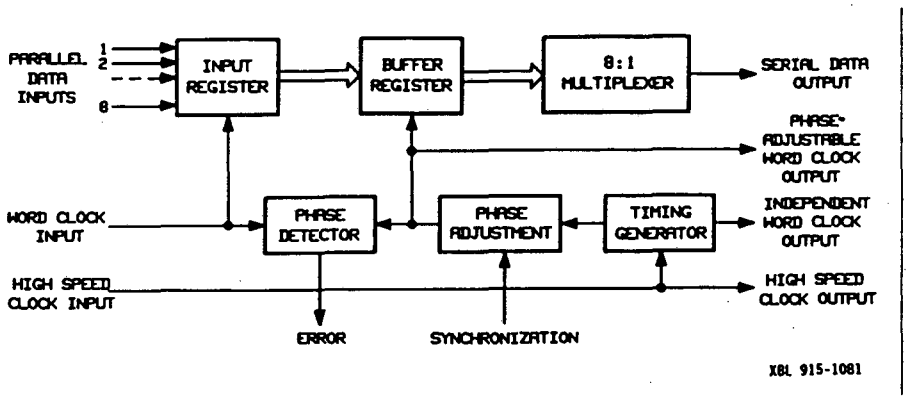

Fig. 2 High speed multiplexer interface.

registers. The internal word clock operates at 1/8th the frequency of the high speed clock. This internal word clock signal is also available from the multiplexer interface chip.

Internal circuitry continuously monitors the internal and external word clocks and generates an error signal if a timing error is detected. The error signal can be connected directly to the synchronization input. A synchronization signal shifts the interface timing, positioning it properly against the external word clock.

An independent word clock output is also available from the multiplexer interface. The phase of this clock is not affected by the self adjusting circuits. Therefore, it can be used as a system reference clock.

B. High Speed Demultiplexer Interface

A functional block diagrams of the demultiplexer interface is shown in Fig. 3. The interface consists of a 1:8 demultiplexer and frame recovery circuit. The 1:8 demultiplexer accepts a serial data input at rates up to 2.5 Gbit/s and converts it into eight parallel ECL data outputs at rates up to 312.5 Mbit/s. The interface also contains a frame recovery circuit. This circuit is enabled by the falling edge of the frame recovery clock. The frame recovery circuit searches for the framing sequence. When the frame is detected a confirmation signal is sent from the interface. The confirmation signal also disables the frame recovery circuit.

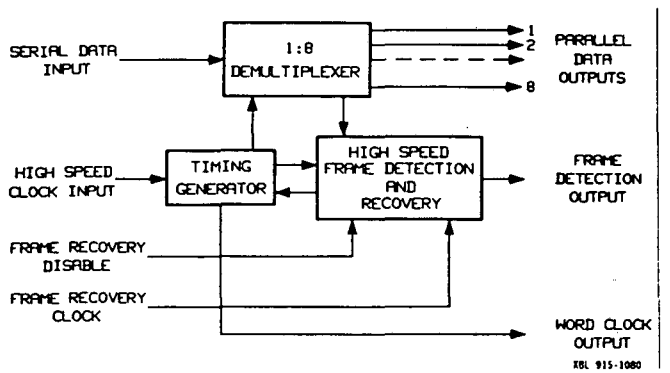

Fig. 3 High speed demultiplexer interface.

The frame detection circuit monitors the demultiplexed data and senses the boundary between two strings of bytes. The signal generated by this circuit will reset the frame recovery circuit. Therefore, no further resynchronization will occur. Typical power dissipations of the multiplexer and demultiplexer interface are 2.3 and 3.0 W, respectively.

For systems operating up to 1.5 Gbit/s, a 16:1 time division multiplexer and 16:1 demultiplexer have recently become available[12]. The 16:1 multiplexer accepts 16 parallel ECL data at rates up to 93.75 Mbit/s. The 16:1 demultiplexer accepts a serial ECL data input at rates up to 1.5 Gbit/s. The demultiplexed parallel data are clocked into a 16 bit output register. The multiplexer and demultiplexer have been primarily designed for SONET fiber optic transmitter and receiver. Typical power dissipations for multiplexer and demultiplexer are 0.95 W and 1 W, respectively.

For the design of a high speed data transmission point-to-point links, many additional circuits are needed to support the operation of multiplexer and demultiplexer interfaces. They include the light source, light detector and appropriate interface electronics. Recent advances in fiber optic components for high speed data transmission have been recently reviewed[9].

IV. Conclusions

For the SSC solenoidal detector suitable subassemblies for high speed point-to-point data transmission are presently commercially available. These subassemblies, such as multiplexer and demultiplexer interfaces, are capable of operating up to 2.5 Gbit/s data rates. Because the subassemblies have been developed for the internationally accepted synchronous optical network, their cost will be significantly reduced in future years. In general, the multiplexer and demultiplexer interface need an additional fast light source, photodetector and associated electronics for the implementation of data transmission links. These components are now available and they are compatible with the above described multiplexer and demultiplexer interfaces[9,13,14].

Also, for data rates up to 100 Mbit/s the optical transmitter-receiver pairs have become available with incorporated light sources and photodetectors[15].

The detailed design and choice of technology for the optical fiber network for a particular solenoidal detector subsystem require the following specific information for each subsystem: number of channels, average and peak data rates, permissible bit error rate, ionization radiation level and reliability. At present, only the number of channels for solenoidal detector subsystems are known, as indicated in Table 1. Other subsystem parameters are still under consideration. However, for the pixel vertex detector the preliminary parameters are known. From these parameters, one can calculate the approximate total bit rate of the data transmission link for the whole detector. The following preliminary parameters for this detector are: total number of pixels = 3.9×10^7, number of pixels per event = 10^3, number of bits per pixel = 48, number of bits per event = 48×10^3, mean value of the event rate 10^5/s, and peak value of the event rate = 5×10^5/s. The number of required bits per pixel is calculated from the following bit requirements: number of bits for the integrated circuit chip = 8, "x" address = 8, "y" address = 8, analog-to-digital converter = 6, chip protocol overhead = 8 and subsystem prototol overhead = 10. This makes a total of 48 bits per pixel. Therefore, the approximate total data rate is 4.8 Gbit/s for a mean value of the event rate of 10^5/s.

The data transmission network can be implemented on a number of ways for the above given total data rate. The detailed design of the optical fiber network will depend on availability of subassemblies, their power dissipation and cost. Also, the design will depend on the component ionizing radiation sensitivity, required reliability, redundancy and maintainability of the network. For example, two cases of the network implementation can be considered for the pixel vertex detector. A network can be implemented by using the data transmission link with rate capability of 100 Mbit/s or 1 Gbit/s. The network consists of 48 links when employing the 100 Mbit/s individual link capability. In this case, the total power dissipation of optical transmitters using a light emitting diode and associated electronics is approximately 320 W. Using 1 Gbit/s individual link capability, the network consists of 5 links, with the total transmitter power dissipation of approximately 40 W. In this case, optical transmitters employ the index-guided injection laser. Consequently, using a high speed capacity link the power dissipation is reduced by a factor of 8. Also, the most high speed data rate capacity networks employ GaAs integrated circuits for their implementation. These circuits are inherently more radiation resistant than even hardened silicon integrated circuits. Furthermore, GaAs technology offers lower power dissipation for the same speed of operation. However, at the present, networks using the 1 Gbit/s capacity links are approximately 20% more expensive than those using 100 Mbit/s links.

In addition to the data, trigger, strobe and clock signals transmission, the fiber optics will be used for transmission of data from various temperature sensors, detector bias voltages and interlock controls. Data from a large number of sensors and monitoring and control points will be multiplexed and transmitted by a sensor and monitoring fiber optics network to a group of signal processors at high data rates and with rapid reconfiguration time. The heart of this network will be an electronic crossbar switch which is capable of operating at an appropriate detector subsystem data rate and reconfiguration time with an acceptable bit error rate.

Further studies are needed on the network topology, the bandwidth requirements, and network reliability and redundancy of all above mentioned applications of the high-speed data transmission using optical fibers in the SSC solenoidal detector. Reliability and failure modes of these networks, electronic subassemblies and optical components must be assessed to determine a necessary level of redundance.

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