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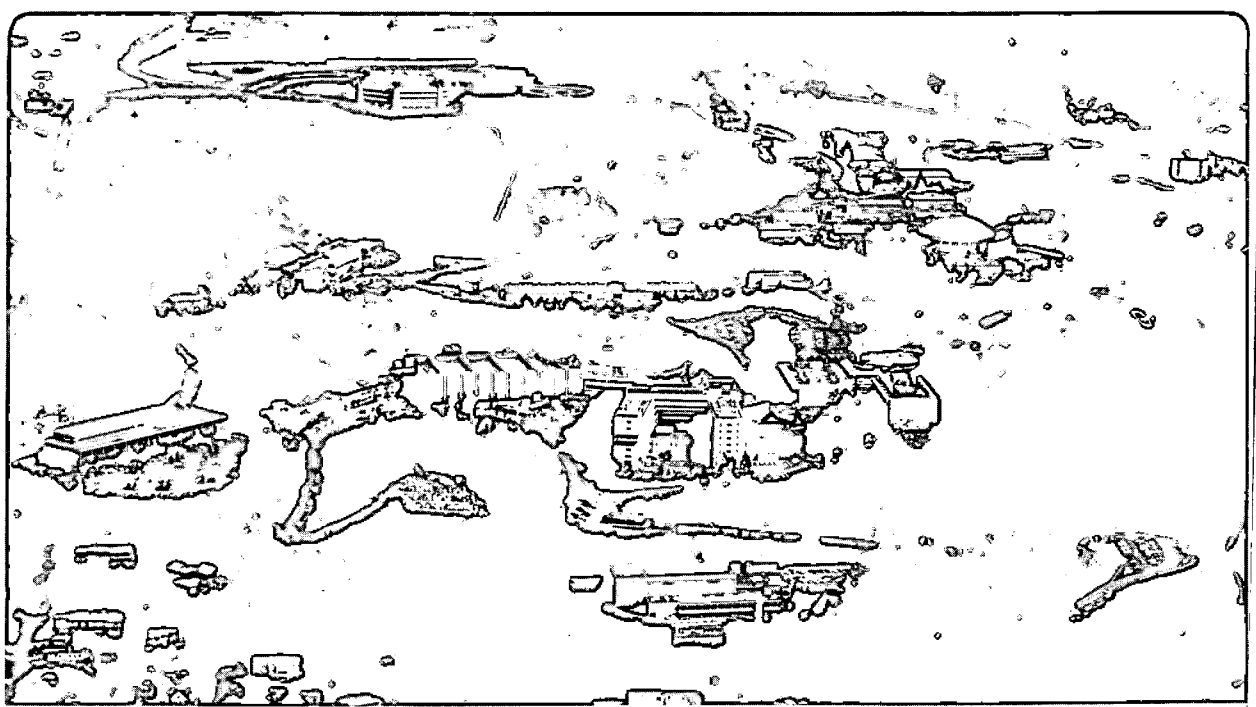

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A Pixel Unit-Cell Targeting 16ns Resolution And Radiation Hardness In A Column Read-Out Particle Vertex Detector

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A pixel unit cell (PUC) *circuit architecture*, optimized for a column read out architecture, is reported. Each PUC contains an integrator, active filter, comparator, and optional analog store. The time-over-threshold (TOT) discriminator allows an all-digital interface to the array periphery readout while passing an analog measure of collected charge. Use of (existing) radiation hard processes, to build a detector bump-bonded to a pixel readout array, is targeted. Here, emphasis is on a qualitative explanation of how the unique circuit implementation benefits operation for Super Collider (SSC) detector application.

1. Background

The first pixel detectors for high energy physics were top-illuminated silicon charge-coupled devices (CCDs) borrowed from the light imaging field [references 1, 2]. CCDs have limitations for high energy physics (HEP) use in fast hadron colliders [3]. Hybrid detectors meant for military infra-red imaging were inspiration for today's HEP-optimized designs [4]. Elegant monolithic detector-plus-readout processes have been demonstrated [5], but could be years from radiation hardness, and are not, yet, designed for SSC speed or read out function. Hybrid circuit designs are further advanced than their monolithic counterparts [6]. When the monolithic, or composite wafer, processes are hardened, hybrid circuits may well be mapped to them.

No published pixel read-out chip, known to these authors, has shown operation adequate for SSC detector particle rate and speed, even before radiation [7,8,9,10,11]. However, many of the functions required have been demonstrated individually. Researchers have demonstrated ±1.5 μm resolution (root-mean-square) in beam tests [12], sampled data PUCs of 50 μm by 150 μm [13], continuous-time filter PUCs [14], monolithic detector and readout [15], radiation hard CMOS [16], 40 ns time walk [17], and row-column (X-Y) readout [18]. Row-column readout schemes have been complex, slow, or lacking in functionality [19].

In this paper, a new column-only read out architecture is *proposed*. A new PUC, developed for this architecture, is *described*.

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1. Objectives

1.1 Radiation Hardness

The final pixel chip is expected to be manufactured with a radiation-hardened bulk CMOS from United Technologies Microelectronics Center. It is a single poly, double metal generic CMOS. Radiation damage effects are better published for this process than any other known to these authors [20].

A non radiation-hardened prototyping process is used to save time and money. The prototyping is through MOSIS using Hewlett-Packard's 1.2 μm CMOS. Only layers and biasing directly mappable to the radiation-hardened production process are used in the prototype. We expect to prototype using UTMC's process through the National Security Administration's RMOSIS, or equivalent, when the service becomes available to us.

1.2 Speed For Time Stamp Resolution

Particles are to be time-stamped to a resolution of 16 ns, which is the beam-crossing rate. Landau fluctuations and detector charge sharing and angled tracks cause input signal amplitude fluctuations leading to time delay variations in the time stamping. This *time walk* is simulated at 8 ns in the PUC, for a 1 to 8 fC input range and 95% of the deposited charge collected in 10 ns. If the readout system knows the time walk and the collected charge (amplitude) of each hit, then all hits may be mapped to a corrected time stamp. This may allow an order-of-magnitude reduction in the PUC power dissipation. There are substantial, negative, effects on data storage (column buffer) depth associated with increased time walk, depending on how early in the signal path walk correction is performed.

1.3 Chip Tiling And Area Efficiency

The pixel chips are to be tiled so that there are no holes where particles may pass through a pixel plane without detection. The array periphery and chip sparse readout must not occupy the majority of the chip area. Incredibly, this can be difficult to avoid with row-column readout (see section 2), especially when ambiguous position resolution, jet handling, and deep time-stamp buffers for higher luminosities are employed. The column-only readout architecture is expected to simplify the periphery at the expense of a larger PUC. A chip on the order of 2 cm^2 is desired, and may yield adequately when care is taken to reduce the ability of any defective PUC to corrupt an entire row, column, or array.

1.4 The Readout Process, With Jets

On average, a 50 by 300 μm PUC that is 6 cm from beam center at nominal SSC luminosity encounters a 340 Hz hit rate. A 2 cm^2 array contains about 16K PUCs with an overall 5.6 MHz hit rate. The peak hit rate in any level 1 trigger (T1) delay time (up to 4 μs) may be far above 5.6 MHz due to jets. There should be no loss of data or readout function for higher than nominal luminosities. No published architectures appear fully adequate to these authors.

Each PUC, when hit, produces a Hit pulse whose width is proportional to its collected charge. This Hit pulse drives a trace to the periphery logic shared by every PUC in the column. One trace is not enough to allow the 3 or more pixels that share charge with most hits to deliver their charge information to the periphery, let alone the jet case (unless time dispersion is employed). If every third PUC Hit output, in a single column, is wire ORed to 1 of the 3 traces to the periphery, so that a single hit produces 3 charge measurements, then full position resolution might be attained. However, a particle jet saturates the 3 traces. In this PUC, an analog store is provided, as an option, to retain full position resolution with jets.

1.5 16K Integrators With Crossed I/O

Pixel arrays require attention to basic grounding and shielding rules. Consider the

potential problems caused by routing a digital Hit output trace from a PUC to the periphery of an array. The 2 cm digital Hit trace will pass through all PUC's in a row, under 300 μm of detector and by every input. With a 3 V Hit transition, capacitive coupling of only 20 aF to the adjacent input injects a 1000 e- signal equal to the discriminator threshold! The capacitance of a minimum width metal trace is on the order of 100 fF. The indium bump-bond layer on the die surface can not be used for a ground plane because of its mass. No dynamic signals are allowed on the top layer of metal. Only current outputs driving virtual grounds are used in this PUC, unless the trace is fully shielded. The PUC requires no dynamic input signals to operate except a reset only after a hit. Continuous-time filtering is used.

2. Row-Plus-Column Read-Out

The column-only read out concept was born as a possible solution to the demonstrated and perceived problems with the complexity, area, and read out speed of the row + column architecture. We review row + column requirements and problems here, before introducing proposed solutions in section 3.

Pixel read out architectures must efficiently and quickly find which PUCs were hit when, and read out those that match the trigger beam crossing time stamp. It is easy to envision building a PUC which puts a hit signal on a horizontal and vertical trace shared by all the PUCs on that row and column. If the traces drive a time stamp pointer memory pattern buffer, then the x, y, and t coordinates are known.

Read in, figure 1, is conceptually simple. Electrical isolation (see section 1.5) remains a risk. Note that all pixel chips demonstrated to date have not had read out activity during read in, though this will be required at the SSC. Further, none have had adequate speed, (this will affect isolation); and one simple array, with no read out on chip, showed severe coupling problems.

Read out, figure 2, has proven more complex than read in, because of the details. There are ghost position ambiguities where 2 PUC write the same time stamp, forcing the periphery to test 4 x,y positions to find, for example, the 2 hit and 2 ghost locations. Traces from the periphery and hit latches in the PUC must be added for this ghost elimination. This activity occurs while all PUC remain active for contin-

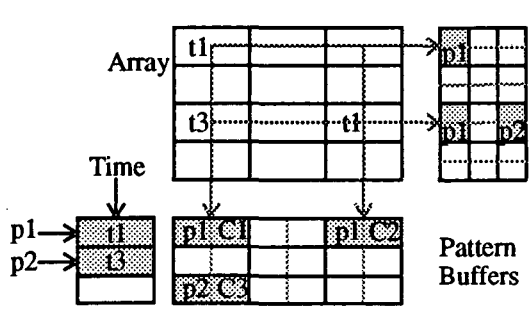


Figure 1. A row-column read-out architecture array sends hit signals to the row and column buffers that store pointers corresponding to when the hits occurred. A measurement of collected charge may also be stored in the pattern buffers.

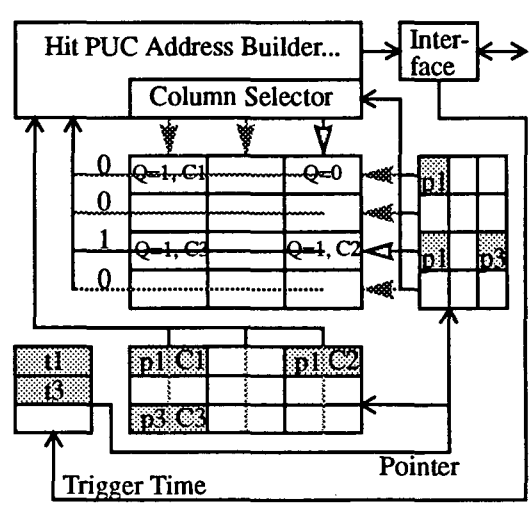


Figure 2. For read-out, each column of PUC are asked if they were hit. The time and pattern buffers function as content-addressable memory.

uous read in. Time stamps and pointers must all be sifted through upon level 1 trigger. The time stamp and pattern memory would function as content addressable memory. To lose less than 0.1% of the hits, the pattern buffer must be about 32 deep. The reset scheme must be able to find and clear PUC even when the buffers over flow, adding complexity. (Our row + column design adds a reset circuit in every PUC to avoid reset complexity [9].)

3. Column (Only) Read-Out

If a rectangular array of PUCs is allowed connection with the periphery only down columns, as in figure 3, then the row position information available using the previously reviewed row + column read out is lost. Position information is regained by having hit PUCs transmit their positions in the column to the periphery. (The row addresses are transmitted to the periphery only during read out of those events chosen by the level 1 trigger, for reasons explained below.)

Column read out adds to the area of the PUC; see figures 4 and 6. Area is saved when PUC addressing is shared by clusters of PUCs; see figure 5. Because of the area overhead per PUC, there must be good reason use the column read out architecture. We believe that there is. The area of the column buffers may be much smaller than that for row + column read out. This area is dead, non-detector, area. We expect level 1 trigger read out to be simplified and sped up. Also, the geometry and electrical isolation of the PUC array is improved.

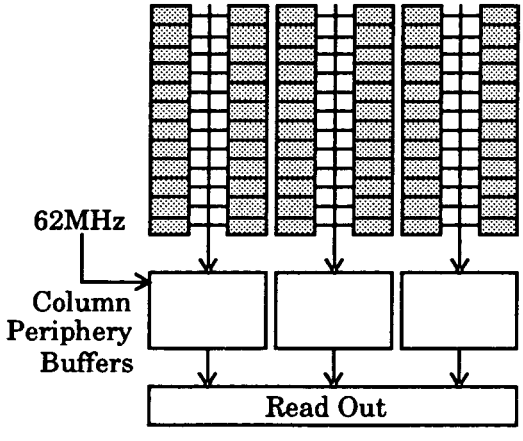


Figure 3. The Column architecture promises faster and simpler read out, smaller periphery, and a superior array layout with better input-to-output isolation.

Pixels, with their fine granularity and 3 dimension (plus time) resolution, could simplify SDC tracking [21, 25, 26] if sparsified hit data can be read off-chip rapidly.

3.1 Arrayed PUC Cross-Talk Reduction

The 50 by 300 μm PUC will tile a 256 row by 64 column 1.9 by 1.3 cm array. With row + column read out, one or more output traces pass in the 50 μm dimension. The metal must squeeze by the bump pad and input circuits, and uses an area equal to the metal pitch multiplied by the long PUC dimension, or 3.6*300 = 1080 μm^2. Traces passing in the other dimension occupy 300/50 = 6 times less area. Traces in one dimension are of metal 1, traces in the other dimension are of metal 2, making shielding of these dynamic signals impossible without significantly more area. The shielding problem is nothing a third level of metal would not fix, but no radiation hard process has a third metal option, of any pitch. Happily, with column read-out, there are no across-array traces along the short dimension of the PUC. The PUC may be narrower and smaller, for better position resolution. The read-out traces can all be in metal 1, allowing

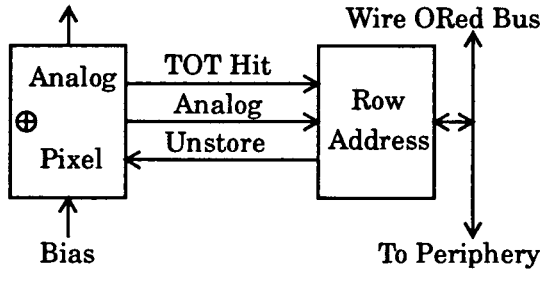
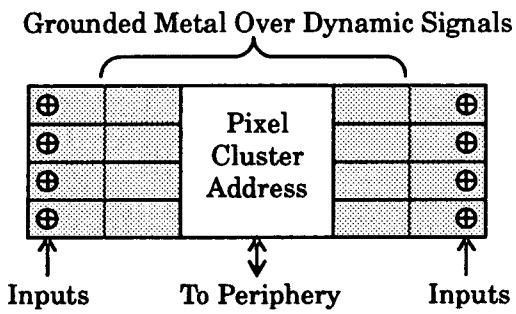


Figure 4. The PUC with column read out overhead.

Figure 5. A PUC cluster shares 7 bits of the 9 bit (256 PUC per column, 2 columns) address to save area.



all these traces to be shielded with AC grounded metal 2. When 2 columns of PUCs share traces to the periphery, then all PUC inputs are near neighbor inputs, instead of inputs next to outputs as in row + column arrays.

3.2 Column Periphery Buffer Size

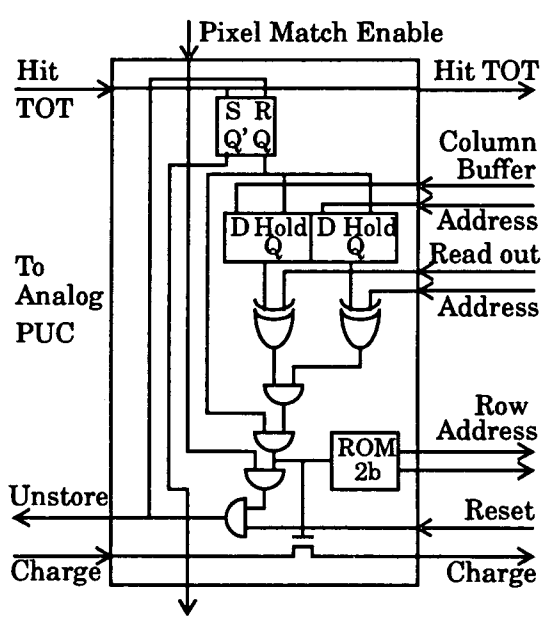


Figure 6. The PUC transmits its cluster row address when its column buffer address matches the read out address.

The average Hit rate, per column, is about 80 KHz. A 4-deep column periphery buffer loses less than 1-in-10,000 hits to a filed buffer, assuming SSC nominal luminosity and a 4 μs T1 delay.

The column buffers need not store a 1 bit hit plus 8 bit row address plus 1 bit left/right column (using one column buffer for every 2 PUC columns), 10 bit time stamp, and the measured charge. Instead, for a buffer depth of 4, it is possible to pass a 2 bit buffer address from the periphery to all the PUCs in a column. When a PUC is hit, it sends a TOT Hit to the periphery, sets its Hit latch, and stores the 2 bit buffer address. The column buffers store only pointers to beam crossing time stamps that registered hits. *The PUC array itself stores the position information.* Why add the position storage to the replicated PUC, instead of growing the column buffers? It is because of our goals of 1) minimum array communication activity, and 2) minimum non-detecting chip area, such as the column buffers. Keeping the hit and column buffer address memories on PUC allows communication of only hit addresses selected by T1, instead of transferral of all addresses. The area of six address traces is saved. The column buffer depth would need to be much larger to store all Hit PUC addresses. For example, in the case of a jet or a particle sharing charge between PUC or traversing at an angle and hitting many PUC, the column buffer need only save a single pointer to the beam crossing time, instead of up to 256 addresses. Note that the column buffer depth required for row + column read out is similar than to the column read out case storing all addresses, but that there are buffers on 2 sides of the array.

3.3 Periphery Buffer Implementation

The function of the column periphery buffer is to store time stamps, one for each hit received from the PUC column. At read out time, all time stamps in the buffers are compared to the beam crossing time stamp of interest from the level 1 trigger. For all matches, the buffer

address is sent to all PUC in the corresponding column, and all hit PUC are read out. The column periphery buffers would naturally be content addressable memory (CAM). If the system has time walk, and the trigger must ask for all hits over a time stamp range of a few beam crossings, then specialized custom CAM addressing must be added. Reset of all PUC from this periphery require that every time stamp in CAM be used in PUC resetting; see the next section. This requires a sequencer or a first in first out (FIFO) port on the CAM. Time walk and reset requirements make this CAM + FIFO buffer potentially large and complex.

If the level 1 trigger is implemented as a single pulse that, at every 16 ns beam crossing interval, signals the acceptance or rejection of any hits that occurred N beam crossings before, then the column periphery buffer function is that of a delay and gate. N equals 256 for a 4.096 μs level 1 trigger latency. Figure 7 diagrams a column periphery where 4 digital time delay circuits replace a 4 register CAM + FIFO. When a PUC is hit, a 1 is pushed into the input of an N bit shift register. N beam crossings later, the 1 appears at the output. If a level 1 accept is also present, then all PUC that stored the pointer to that shift register are read out (see the next section). If the pixel array exhibits time walk or if the trigger accept goes true for several beam crossings, then the output pulse from the shift register needs only to be widened. The digital delay of the shift register can be implemented more efficiently as an 8 bit non-binary sequence dynamic shift register counter. The digital delay periphery is expected to be smaller than the CAM + FIFO registers, and may occupy only the column width by 500 μm.

3.4 Sparse Readout And PUC Reset

The level 1 trigger will select approximately one in every 1000 of the hits stored in the PUC array. Our goal is to require the least communication activity inside the PUC array. Therefor, as written earlier, each PUC sends only a fast Hit signal to the periphery. Hit PUC address and collected charge information is transmitted to the periphery only when selected by the level 1 trigger. Any PUC that was hit longer than a level 1 trigger delay before is reset.

PUC reset of the Hit latch and analog store may be accomplished in at least 2 ways. Conceptually the most simple is an autonomous PUC that can self-reset. The PUC would store the hit information until the read out could not possibly need it any longer, by waiting a full level 1 trigger latency time of, say, 4 μs. Efficiency loss due to the probability of any single pixel being hit again while waiting the 4 μs is 0.0014. This method uses the most PUC area, but allows the lowest array activity and architectural complexity.

The second reset method accomplishes PUC reset by action at the periphery. The challenge

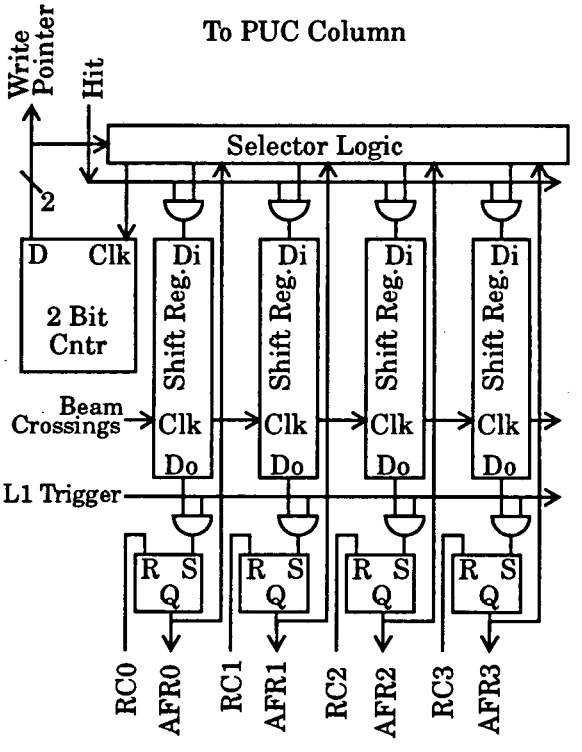


Figure 7. A column periphery buffer may be implemented as a digital time delay.

here is to guarantee 100 percent reset efficiency. It is not true that every PUC that sends a hit signal to the periphery will register separately there. For example, if a PUC generates a hit just after another hit, the periphery may miss the second hit due to periphery dead time. Happily, our level 1trigger read out method allows the resetting of all hit PUC that have aged a level 1 delay time or longer. When any periphery digital time delay circuit produces a true output, it is compared with the level 1 trigger select input. If there is coincidence, then the corresponding physical address of the time delay circuit that went true is placed on the pointer address traces to the column of PUC. Each PUC that finds a match is read out and reset. That includes the PUC that reported the first hit that started the periphery time delay *and* all those hit PUC in the column that sent hits that occurred in the dead time just after the first hit, for reasons such as time walk or consecutive beam crossings hits. When any periphery time delay circuit goes true and there is no coincidence with the level 1 trigger input, then the same read out and reset sequence occurs (possibly sped up), but the read out data is sent to the trash. With an appropriate PUC design, there can be no PUC that has tagged itself hit that did not store the pointer address of a periphery time delay circuit that does not go true at the delay interval. All hit PUC are than reset in the same, simple way.

3.5 Analog Addressing

Digital signals are assumed throughout the discussion of readout architectures. In some cases, a multi-bit signal bus may be replaced by a single trace with an analog signal. The PUC could, perhaps, use two 16-valued traces to replace 8 binary coded traces. Each PUC might have 2 resistors that form a voltage divider to generate the analog addresses. The pointer memory in the PUC might then be capacitor, and the input pointer to stored pointer might then be implemented as a window comparator.

4. Pixel Integrator Operation

The integrator of figure 8 is of a standard configuration [22, 23]. A transimpedance amplifier performs as an integrator with the (unusually small) 1/2 fF feedback capacitor, for a gain of 2 V/fC.

The detector is patterned on its n^+ side, such that radiation-induced transmutation doping, leading to increased depletion voltage, moves the depletion region away from the p+ back side. Charge collection is thereby slowly degraded, in contrast with the double-sided strip's loss of charge collection. Electrons are collected, inducing a positive-going pulse at the integrator output. The detectors are DC-coupled. Leakage currents after 10 years of nominal operation, even for 50 by 300 μm pixels at 0 Celsius are expected to be about 5 nA and 50 nA operation is a goal. 50 nA is 50 fC per μs, causing a huge 100 mV per ns slew rate at the integrator output. At the 50 nA leakage level, the integrator would require resetting every few ns if not for the synthetic inductive reset circuit (or AC coupling, which is harder to do in a pixel than a strip, detector, because one high-value bias resistor per pixel is required)!

4.1 Small-Signal Operation

A synthetic RC-CR noise-shaping filter is implemented. The roll-off of the 3-stage integrator is complex, but can be approximately modeled as 3 poles nominally at 20, 40, and 80 MHz (current setable).

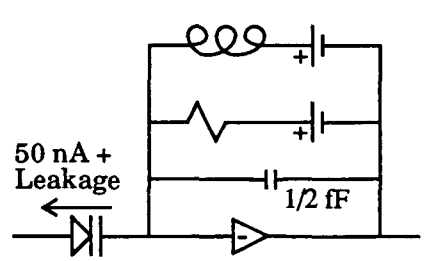


Figure 8. PUC integrator with synthetic resistive and inductive reset.

One filter zero is provided by the (synthetic) resistive reset, another zero by the (synthetic) inductive reset, nominally 5 and 1 MHz respectively (current setable). Figure 9 details how the integrator is implemented with transconductors. The reset transconductor, G_R, forces the integrator output voltage to V_b. G_R attempts to cancel any (noise) signal; it contributes the CR. The time constants are

$$\tau_{RC(1)} = \frac{A_V|^{integrator}_{closed-loop}}{gain-bandwidth} \approx \frac{C_{input-node}}{C_F(2\pi f_{GBW})}$$

$$\tau_{CR}|_{resistive} = \frac{G_R}{C_F}$$

$$\tau_{CR}|_{inductive} = \frac{G_L}{C_F}$$

where G_R is the effective transconductance of the reset circuit and the integrator gain-bandwidth product is for the integrator amplifier viewed as a single stage, since it is operated closed loop. This circuit may use a differential pair in weak inversion, where G_R is, approximately

$$G_R \approx \frac{1}{2} \cdot 27 \cdot I_R$$

where IGFET transconductance is 27 Siemens per Amp. Requirements for AC small-signal closed-loop stability may be approximated

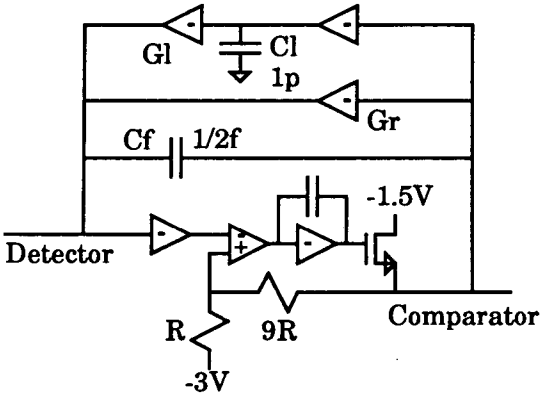


Figure 9. The integrator uses transconductors, capacitors, and (IGFET) resistors.

$$\tau_{RC(2)} \ll \tau_{RC(1)} \ll \tau_{CR}|_{resistive} \ll \tau_{CR}|_{inductive}$$

The 2 poles must be at different frequencies to give the integrator positive phase margin and AC stability. For similar reason, the resistive zero must be slower than the slowest pole for the integrator-transconductor loop. (This restriction is comfortably met, because the signal-to-noise-ratio falls if any zeroes are faster than any poles, causing the signal to fall faster than the noise.) A 40 dBV per decade transition with greater than 0 dBV loop gain is seen when the 2 zeroes are at the same frequency. The resulting classical saw-tooth large-signal oscillation is not tolerable in this application.

The synthetic resistor and inductor require transconductors with small phase shift, as compared with a reactive lead/lag of 90 Deg., to beyond the band width of the closed loop integrator. These circuits operate with 1 nA bias currents to get the time constants to the needed values, so greater than 20 MHz band widths can be a problem for all but a few circuit topologies. See the reset section below.

The required integrator closed-loop speed and gain are surprisingly high and strip-like.

$$A_V|_{closed-loop} \approx \frac{C_{det} + C_{FET} + C_{misc} + C_F}{C_F} + 1$$

$$A_V|_{closed-loop} \approx \frac{420 + 250 + 80}{0.5} + 1 \approx 1500 \approx 64dBV$$

The closed-loop bandwidth, f_{CL}, must be about 20 MHz for a simulated 8 ns time walk. The gain-bandwidth required is then

$$f_{GBW} \approx \frac{A_V|_{closed-loop}}{2\pi\tau_{RC1}} \equiv 30GHz$$

This f_{GBW} was not achievable in 1 transistor stage, with this process and input capacitance situation. The following idealized example will illustrate why more than 1 gain stage is required. Assume we have designed a f_{GBW} = 3 GHz amplifier that uses 10 μW. Assume that

the input transistor is in strong inversion. To reach 30 GHz, the input transistor current of the 3 GHz amplifier must be increased 100-fold, dissipating 1000 μW. Instead, if 3 of them are placed in series the gain-bandwidth is 27 GHz at 30 μW, about right. Since the integrator must retain its 60 Deg. phase margin with 3 phase shifting stages instead of 1, each of the 3 amplifiers is sped up by a factor of 3 over the single amplifier case, and the input transistor currents by a factor of 9. The 3 cascaded amplifiers now dissipate 270 μW. The 3 stage integrator amplifier uses about a third of the power of the single stage, at the cost of larger area, complex AC stability criteria, and poorer large-signal response. A large number of multi-stage integrator amplifiers were simulated. Two and 3 stage designs were tried, including popular RF topologies. The integrator amplifier must be inverting. Possibilities included 3 common-source stages, or a common-source and non-inverting stage. Open loop stages with controlled (low) voltage gain were tried. The closed-loop buffer configuration chosen worked best. Closing a feed back loop around the buffer pole-splits, resulting in 1 slow pole and many fast. The integrator middle stage is drawn as a differential input transconductor in figure 8. In reality, it is an asymmetrical input, where the inverting input is a gate of degenerated common source N IGFET, and the non-inverting input is the source. The resistors are IGFETs of about 6 and 60 KΩ The resistors are not desirable because they dissipate a constant power at a fixed bias point. When the pixel user sets the bias currents 10 times below nominal to achieve 16 ns time binning with a long time walk, using a delay look-up table function to save power, the resistors consume a dominant 17 μW.

A PSPICE small-signal analysis of the voltage-driven integrator, figure 10, shows the amplitude response of the gain-of-10 booster and the overall integrator. The 4 MHz CR response of the resistive reset and the steep high frequency roll-off are shown. The inductive reset is turned off.

4.2 Large-Signal Operation

Assume that the integrator reset transconductor is simply a differential pair with current source bias on the common sources. With C_F = 1/2 fF, the 2 V per fF gain of the integrator leads to large voltage swings at the diff. pair input. These large signals fully switch the diff. pair, the reset G_R goes to 0, and the small-signal time constant of the high pass goes to 0. The reset bias current is effectively switched to the input. This current-steering action causes the integrator output to ramp the signal back to base line. If the reset bias current, I_R, is 2 nA, or 2 fC per μs, then a 8 fC collected charge is reset in 4 μs. See figure 11.

If the discriminator threshold is small compared to the signal, then time above integrator baseline is synonymous with time above threshold. With this integrator reset scheme, the time above threshold is proportional to input charge. *The time above threshold remains proportional to input charge even if the integrator output saturates with the signal pulse.* Reduction in supply voltage is no longer limited by the signal, and ±1.5 V supplies are used for minimum power dissipation. *There is no hard limit to the maximum permissible input charge.* However, read-out is simplest

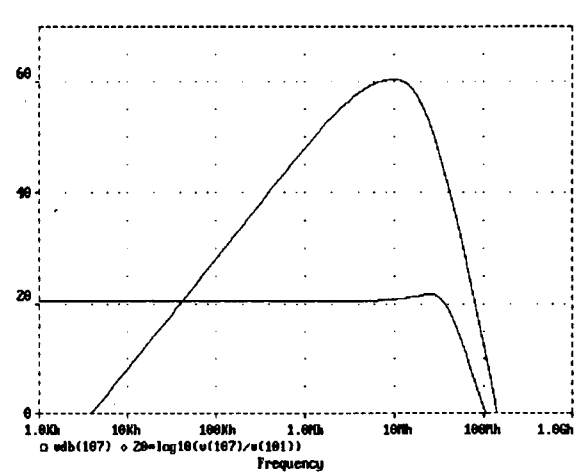


Figure 10. Simulation of the small-signal response of the voltage-driven integrator and internal booster. The Y axis is in units of dBV.

when the collected charge is known in a T1 delay time.

4.4 Reset Circuit Constraints

The integrator reset circuit is at the core of the PUC functions of time-over-threshold (TOT), active RC-CR filtering, and discriminator threshold. Unfortunately, the smallest and fastest reset circuits that implement these functions most naturally with just a few transistors, do not deliver the correct transconductance, TOT pulse width, and threshold accuracy at once. For example, when the small signal time constants are set, then the TOT pulse ends up too long. The reset circuit is over-constrained.

The first PUC prototypes are implemented with a 1 IGFET (insulated gate field effect transistor) reset circuit. It is fast, small, and uses little power. When a 2 nA bias current is used, the correct 2 μs per fC TOT pulse width is achieved. However, the small signal transconductance is too large, and the closed loop integrator is not AC stable. One solution is to use capacitive voltage division from the integrator output through the feed back beta network to the reset IGFET or diff. pair high speed transconductors. The capacitor network phase shift gets better as the frequency goes up, which is good. But this technique remains

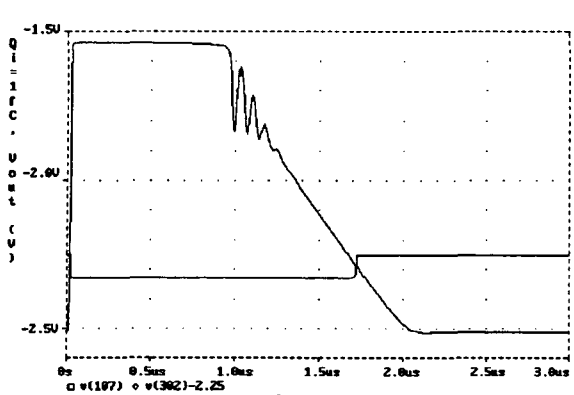


Figure 11. A circuit simulation showing the TOT response of the discriminator Hit. The integrator return-to-baseline over shoot is small, though there is ring off swing limit.

troublesome when using a process with no low parasitic capacitors. Additional bias stages are required, degrading the control over the integrator output DC level, and so the discriminator threshold match.

We have done preliminary simulations on a new technique that promises to produce the correct TOT pulse width, small signal time constant, and low discriminator mismatch all at once. With this technique, we use the 1 IGFET reset, with its optimum low area, speed, and mismatch. We set its transconductance with a 1/2 nA current source. The too-long TOT pulse width is reduced by switching in an additional 1.5 nA reset current when the discriminator produces a true TOT output. This is a fed back loop around the entire greater discriminator, with its own special stability criteria. Note that the gain of a circuit in slew or overdrive limit has collapsed to 0, and cannot oscillate around the feed back path (internal minor loops may still oscillate). We are taking advantage of this signal dependant variation in stability criteria to dynamically alter the transconductance and TOT pulse width. Fast switching of the 1.5 nA current with low charge injection is critical.

4.5 Reset Ringing And Rectification

Designing the integrator and reset to return to baseline adequately is the most difficult part of the circuit design. If the integrator returns to below baseline after a signal pulse, there is no false discriminator triggering. But most over shoot will ring the output around the baseline, threatening false triggers. Since the integrator is a complex multi-stage design, there is a tendency to ring. To meet the 4 μs TOT pulse width, the CR time constant ends up being too low, leading to ring. The integrator is like many MOSFET amplifiers whose output swings to the rails- the overload recovery time causes the output to stick high too long, and then overshoot the correct output.

The inductive reset circuit is most sensitive to rectification errors. The circuit must have a

long time constant. Assume it is soaking up 40 nA of detector leakage current when a charge is collected. The charge produces a signal that slews the voltage on C_L by 0.1 mV, causing the 40 nA to rise to 40.1 nA, say. The integrator signal returns to baseline after the TOT pulse width of 4 μs. The total error charge caused by the 0.1 nA error is 0.4 fC, which causes the integrator to settle at a voltage 800 mV below the original baseline. The resistive reset circuit can drive ±0.5 nA, but it takes many TOT pulse width for the inductive reset to settle. The TOT Hit switched reset current boost technique can reduce this integrated rectification error by switching the drive current to the dominant pole capacitor off during TOT Hit. This design is active now.

5. Pixel Discriminator Operation

Figure 12 shows the PUC greater discriminator. The part of the PUC used for the address generation required for column readout is not shown here, but was shown in figure 6. The discriminator consists of an integrator with active DC restore (reset), a comparator, Hit latch, and analog store.

5.1 Comparator Threshold

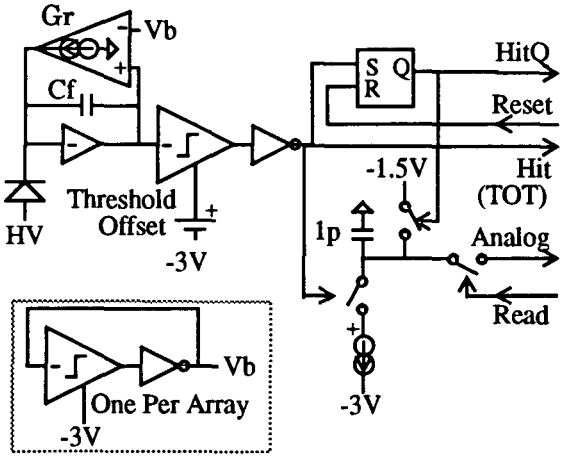


Figure 12. PUC time-over-threshold (TOT) discriminator and optional analog store.

The comparator input, like the entire signal path, must be single-ended for minimum power and area. As shown in figure 3, a replica comparator generates the threshold voltage, V_B. A voltage source *common to all pixel chips*, the threshold offset, V_{TO}, sets the discriminator threshold, nominally 1000 e^-. The temperature, process, and radiation effects are cancelled by operating the comparator and replica input transistors at the same current density at their switch points.

The discriminator threshold of each cell varies due to transistor current-conduction mismatch in the integrator reset and comparator input stages. This mismatch, V_{OS}, may be reflected and referenced to the comparator input, knowing the IGFET transconductances. Mismatch can be a problem. (The author's first pixel design, where V_{OS} was not quantified and controlled due to time constraints, showed a ±3000 e^- threshold mismatch that reflected to a ±70 mV (±1σ) V_{OS}, and others have reported excessive threshold mismatch[9].) V_{OS} falls in proportion to the square root of gate area increase. Gate area grows too quickly to reduce V_{OS} to the order of noise. To further lower threshold mismatch, gain was moved from the comparator to the integrator to increase the voltage that represents 1000 e^-. IGFET conduction mismatch constants have been measured and threshold mismatch is expected to be at the level of noise.

The comparator is a CMOS inverter. V_{TO} is 320 mV for a 1000 e^- threshold. The comparator input is driven off by 320 mV, which is sufficient to keep its quiescent current negligible. The full-speed charge range is 1 to 8 fC. Comparator over-drive would be 1.68 to 15 V over that range, but for integrator output clipping. Signals above 1 V are clipped, thereby offering a constant overdrive to the comparator to minimize time walk. Slew rate remains a function of input signal.

6. The Analog Store

The optional analog store uses the Hit TOT pulse to switch a known current into a capacitor. The IGFET capacitor is normally shorted to the -1.5 V supply. A hit charges the capacitor. The destructive readout shorts the capacitor to a wire-ORed trace to an integrator summing junction at -1.5V. The readout switch time constant is about 1 ns, so analog readout multiplex rate will be determined by the periphery circuits, which are shared by 256 PUCs in each column, and so can be relatively fast and power-hungry and still be a minor part of the power dissipation. The analog store saturates at a current-setable input charge level, nominally 8 fC.

7. Simulated Performance

Calculations of noise and excess noise, parasitic capacitances, transistor conduction mismatches, and circuit simulations have been performed. Table 1 is a short summary of expected electrical operation. Prototype PUC measurements will be reported in a follow-up paper.

Table 1. Expected Pixel Characteristics.

Time walk, Qi = 1 ~ 8fC	<16 ns
Time delay to Hit, Qi = 4fC	<32 ns
Noise charge, input referred	125 e^- RMS
Noise, 10 yr./ 10 MRad SiO_2	<200 e^- RMS
Disc. threshold offset set	-1000 ~ 3000 e^-
Disc. threshold variation	<noise
Thres. variation chip-to-chip	<noise
PUC size, PUC disc. & store	50 x 150 μm
PUC size, addressing and all	50 x 300 μm
Position resolution, 50μm dimen.	<2 μm
Res., 300μm d. 25μm from ends	<2 μm
Resolution, 300μm dimen.	<10μm
Time-Over-Threshold gain (setable)	2μs/fC
TOT gain variation	<5%RMS
Analog Store gain(setable)	188fC/fC
Analog store gain variation	<5%RMS
Power supplies	0, -1.5, -2, -3, V_{TO} = 0.32V
Power, 16ns time walk (setable)	144μW
Power, 16ns time binning (noise up)	30μW

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9. Conclusion

The proposed column read out architecture promises the advantages of better pixel array electrical isolation, smaller periphery area, better read out speed, and simplicity over previously reported architectures. There appear to be no brick walls at higher than nominal SSC luminosities. The pixel chip will retain good position resolution for particle jets, using in-PUC analog stores.

Column read out and the steered-current integrator reset concept greatly affect the pixel unit cell. The proposed column read out architecture exacts an area penalty in the pixel unit cell, as compared to the row + column read out approach. Because row + column read out requires its own area penalties, the extra area may be small. We expect to achieve an pixel unit cell size of 50 by 300 μm or less.

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[18] See [4] and [7].

[19] See [4], [5], [7], [8], and [12].

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