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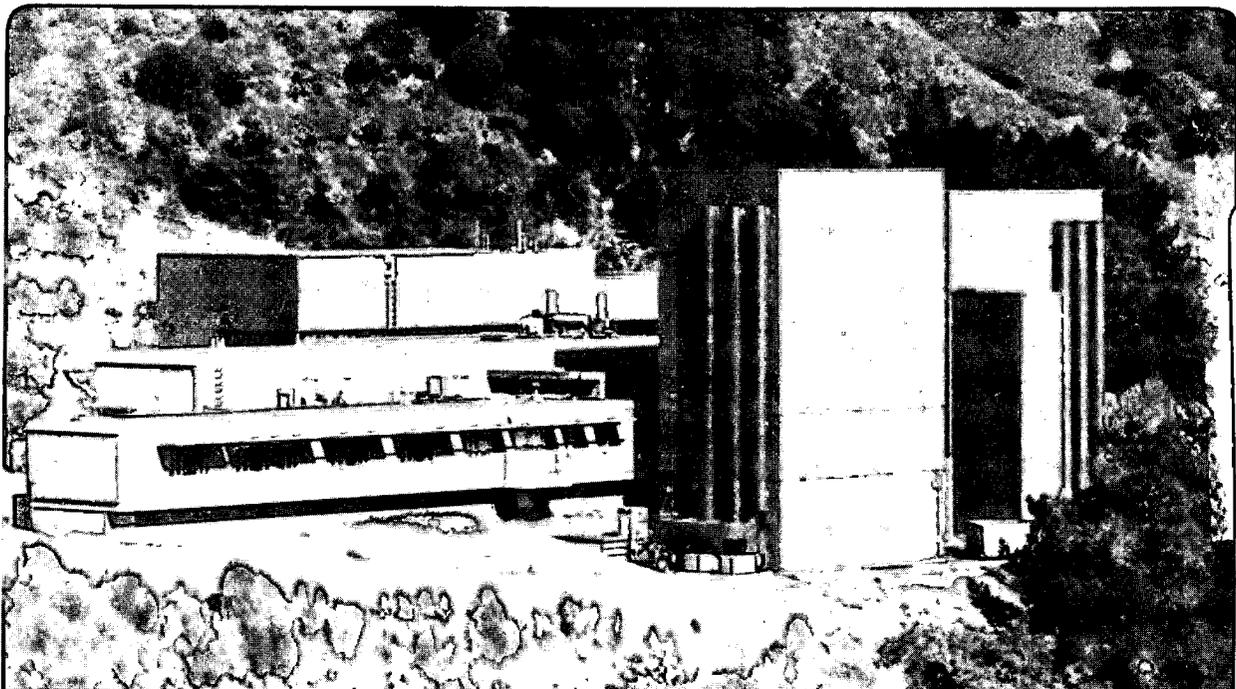
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Changes in Electronic Device Properties During the Formation of Dislocations

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**Changes in Electronic Device Properties
During the Formation of Dislocations**

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CHANGES IN ELECTRONIC DEVICE PROPERTIES DURING THE FORMATION OF DISLOCATIONS

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ABSTRACT

We describe the results of an investigation into the formation and properties of dislocations in electronic devices. We have made electron transparent specimens from metastable GeSi/Si p-n junction diodes and introduced dislocations into the devices by heating *in situ* in the electron microscope. A modification made on the specimen holder for our microscope enables us to measure the characteristics of these devices while they remain under observation in the microscope. We can therefore observe the changes in the electrical properties of the devices as dislocations form. We confirm that the introduction of dislocations has a deleterious effect on parameters such as the reverse leakage current through a diode. However the magnitude of the effect we observe can not be explained by a generation-recombination process and instead we suggest a model based on the creation of point defects or the diffusion of metals during the formation of dislocations. We also consider the kinetics of dislocation formation, and in particular how the extent of dislocation formation in a device depends on the subsequent processing steps which it undergoes.

INTRODUCTION

Structural defects in materials are known to have a deleterious effect on the properties of electronic devices [1] and this has motivated extensive efforts to create better materials for device applications. Modern bulk crystal growth techniques can result in substrates with very low densities of defects and excellent electronic properties. However for many new and proposed device geometries it is important to be able to grow on these substrates high quality films of a range of compositions and layer thicknesses, which are often not lattice matched to the substrate. Unfortunately for electronic applications, the epitaxial growth of a mismatched film on a substrate is limited by the formation of misfit dislocations at the substrate/epilayer interface, a process which is energetically favoured for sufficiently thick epilayers [2]. We have therefore developed an interest in investigating the kinetics of the formation of misfit dislocations in devices and the effect they have on the electrical properties of a device.

We can observe the formation of misfit dislocations by examining metastable heterostructures in epitaxial strained layer systems such as GeSi/Si. In these systems dislocation formation is energetically favourable and will occur if the material is heated to sufficient temperature. Heating electron-transparent specimens of these materials in the transmission electron microscope (TEM) therefore allows us to observe dislocation growth (and occasionally nucleation) dynamically in real time [3]. In order to correlate electrical changes with the formation of misfit dislocations, we have developed a method of recording the electrical characteristics of a device while simultaneously observing the introduction of dislocations [4]. This correlation of electrical and structural changes in an individual device represents a different approach from studies which rely on a statistical correlation between performance and dislocation density, the latter being measured subsequently using a destructive technique such as TEM. We have used the results of these experiments to investigate the electronic properties of the dislocations themselves, as well as to study the kinetics of the relaxation process in lithographically patterned and unpatterned structures.

In this paper we consider the behaviour of dislocations in GeSi/Si p-n junction diodes. We firstly describe the experimental method and show how it can be used to investigate the electrical properties of the dislocations. We find that a simple generation-recombination process [1] occurring at the dislocation cores does not adequately explain the changes we observe in electrical properties, and we suggest that device degradation due to the introduction of dislocations is related to the creation of point defects or the diffusion of impurities such as metals during the formation of

the dislocations. We then describe the kinetics of the relaxation process and discuss the strong dependence it has on device processing steps.

MEASUREMENT OF ELECTRICAL PROPERTIES DURING DISLOCATION FORMATION

Our experiments were carried out on p-n junction diodes fabricated in GeSi/Si heterostructures having a variety of doping levels, Ge content and layer thickness. The structures were grown by molecular beam epitaxy at a substrate temperature of 550°C and a rate of about 1 monolayer per second, using 3 keV ion beam doping of As and B with molecular species. The growth sequence consisted of an n⁺ substrate, followed by an n-doped Si buffer layer and a p-doped Ge_xSi_{1-x} layer (x = 0.10 - 0.30). On some structures a p/p⁺ Si capping layer was added. We also examined control structures with x = 0. Doping levels were chosen so that the depletion region at zero bias extended about half way through the GeSi layer; GeSi layer thicknesses were chosen to ensure metastability, in other words the GeSi layers were above the critical thickness h_c [2], but not so much greater that significant relaxation occurred during growth. On heating the material above the growth temperature, dislocations therefore nucleated and grew in the plane of the interface to relieve some of the stress. The dislocations formed have Burgers vectors $\frac{a}{2}\langle 110 \rangle$ [5] and glide on {111} planes, creating an orthogonal array when observed in plan view (figure 1a). The interfacial (misfit) segments are connected to the surface, or to another misfit segment at the upper GeSi/Si interface if the layer is capped, by a threading arm, and propagate to relieve stress as shown in figure 1.

To fabricate devices suitable for electrical characterisation, mesas of sizes ranging from 10x10 μm² to 500x500 μm² were formed in the junction region using reactive ion etching. The mesa sidewalls were passivated by a deposited oxide and metal contacts made by sputter depositing a 20nm 10%Ti-W contact layer (figure 1b); other diodes were fabricated using ultrasonic cutting to define a 2.3mm mesa, without the addition of a metal contact layer or passivation (these diodes of course showed inferior electrical characteristics). In both cases, electron transparent regions were formed by chemically etching from the back, enabling interface dislocations to be observed in plan view. We modified a Gatan single-tilt heating holder, which is capable of heating a specimen to above 1000°C, by adding a top surface electrical contact via a Ta wire ring and a lower contact through the furnace itself [4]. The temperature was measured using a Pt thermocouple which has been calibrated to within 30°C [6]. Experiments were carried out in a JEOL 2000FX electron microscope equipped with a Gatan image intensifier and a video recording system.

ELECTRICAL MEASUREMENTS ON DISLOCATIONS

Upon heating these devices *in situ*, we observe the growth of dislocations and simultaneously a degradation in the electrical characteristics. Figure 2a shows the increase in the reverse leakage current we observe as the defect density increases. Control structures with no Ge do not show this effect (figure 2b), demonstrating that these electrical changes are correlated with the formation of misfit dislocations.

It is clear that the effects we observe are not due to any action of the threading arms as "short circuits" through the depletion region. This mechanism would not lead to the proportionality between leakage current and dislocation length which we observe, since dislocation velocities at these temperatures are so high, in the range 1-10 μm sec⁻¹ at 700°C (see below), that most dislocations rapidly grow across the entire diameter of the mesa, as in figure 1b, and the number of threading arms is therefore not proportional to the total length of dislocation at the interface. We have therefore modelled the misfit segments themselves as generation sources for carriers in the depletion region when the device is in reverse bias [7]. The relationship between reverse leakage current and dislocation length can be used to calculate the efficiency of dislocations at generating current. Experiments with several diode geometries, including *ex situ* heating experiments on patterned mesas in which the dislocation density is determined subsequently by TEM examination (figure 3), suggest that each dislocation generates 10⁻⁵ - 10⁻⁴ A per meter of misfit length, or about 10⁴ - 10⁵ electrons per Å per second (this number is given at -5V but is somewhat dependent on reverse bias voltage).

We expect the generation rate for current, G , to be related to parameters of the trap states associated with the dislocations as follows [1]:

$$G = \frac{v_{th}\sigma_0 N_t n_i}{2\cosh\left(\frac{E_t - E_i}{kT}\right)}$$

where v_{th} is the thermal velocity, σ_0 the capture cross section (assumed the same for both electrons and holes), n_i and E_i the intrinsic carrier concentration and Fermi level, and E_t and N_t the trap energy and density in the depletion region.

The degree of dissociation and the possibility of decoration by metal impurities will affect the capture cross section and trap energy associated with the dislocations. However, using values for E_t measured in deformed silicon using transient junction capacitance techniques [8] and a value of 10^{-15} cm^2 for σ_0 [1], we can calculate N_t and thus in principle address the issue of whether special sites at or around the dislocation lines (such as kink sites) are responsible for the generation of electron-hole pairs.

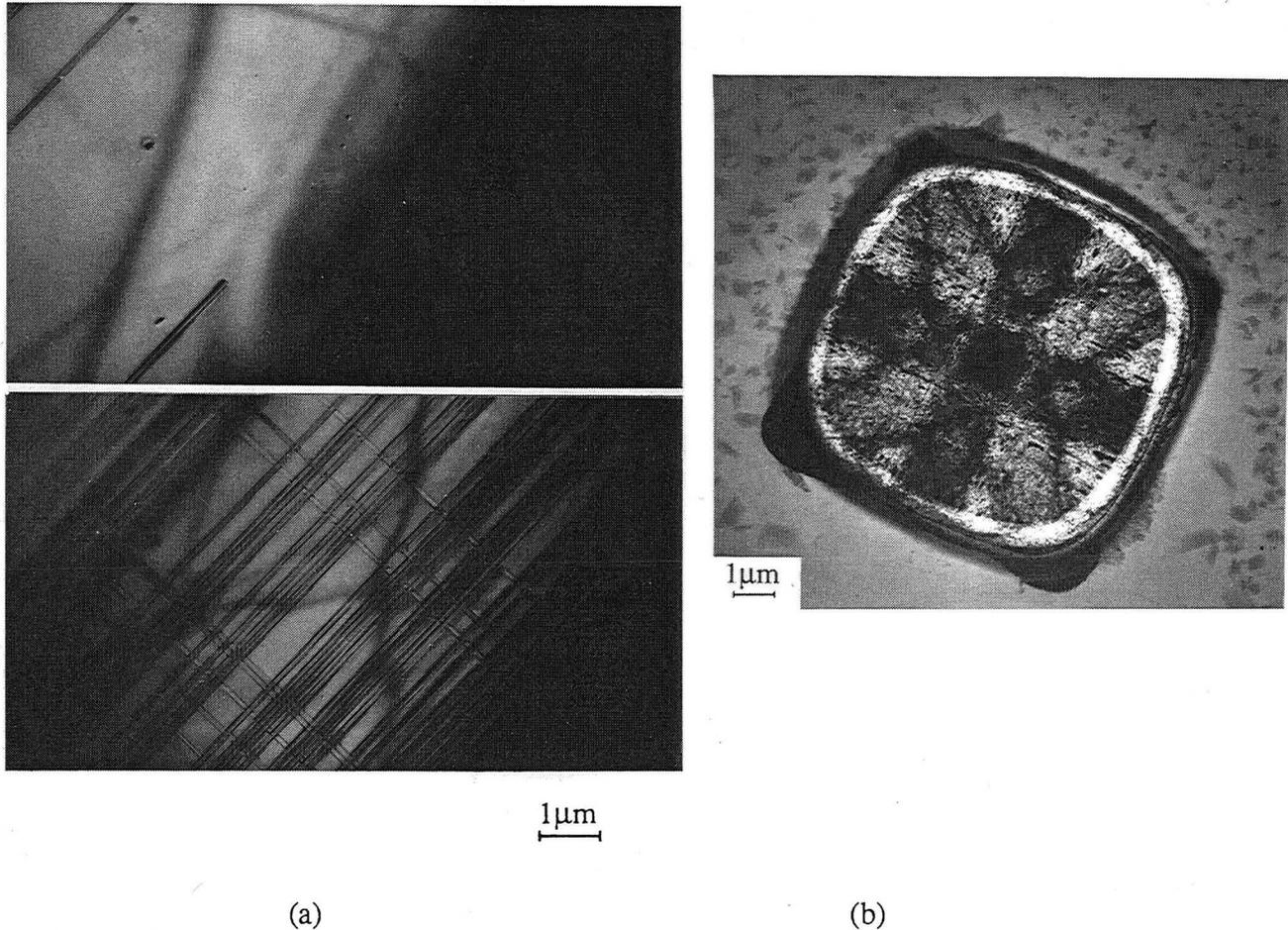


Figure 1. (a) Progress of relaxation in a GeSi/Si heterostructure consisting of 400nm p⁺/p-doped Si on 100nm p-doped Ge_{0.2}Si_{0.8} on an n⁺ Si substrate. We show 022 bright-field images in the plan view geometry. Initially no dislocations were visible in the field of view; after heating for 2.30 minutes to 650°C (upper image) dislocations appear in pairs, one at each GeSi/Si interface, linked through the GeSi layer by a threading arm. After 71.00 minutes at 700°C (lower image) further relaxation has occurred.

(b) Dislocations in a patterned mesa. 022 bright field image of a complete 10×10μm mesa, thinned from the back. The structure consisted of 20nm Ti-W on 200nm p-doped Ge_{0.25}Si_{0.75} on an n⁺ Si substrate. The bands are bend contours and indicate that the lattice planes are tilted by 2° at the edges of the mesa. Dislocations were observed (arrow) after a severe heating cycle of 14 minutes at 800°C.

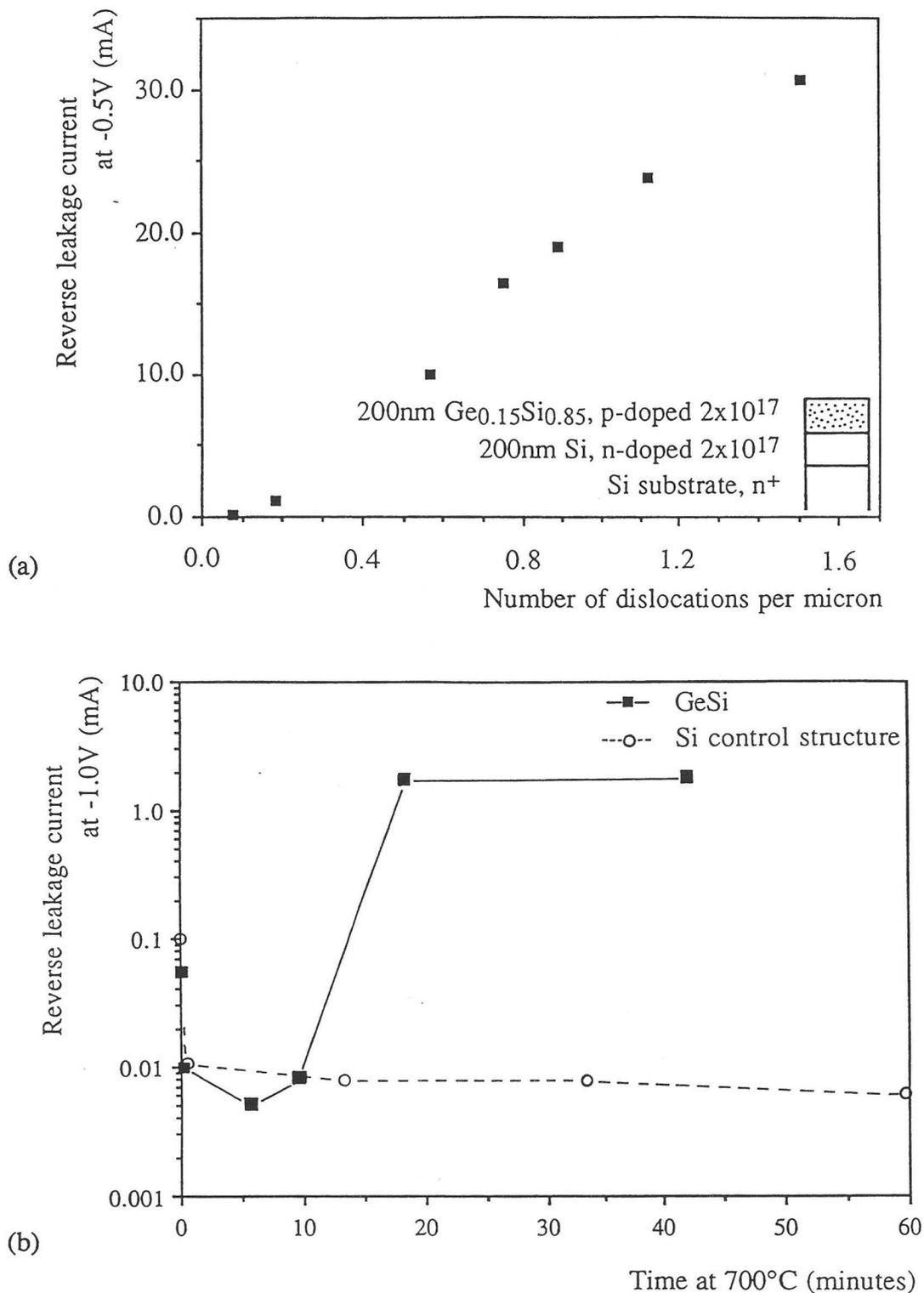


Figure 2 (a) The correlation between dislocation density and reverse leakage current for a 3mm diameter ultrasonically cut diode. The number of dislocations cutting a line is an average over several fields of view, and the current was measured at a fixed reverse voltage through the whole device. Note that a dislocation density of $16\mu\text{m}^{-1}$ would correspond to complete relaxation. In general even extensive heating does not lead to relaxation of more than 10-20% of the strain. (b) The increase in reverse leakage current at a fixed reverse voltage upon heating *in situ*, compared for an ultrasonically cut diode of the structure shown in figure 1a and an unstrained control structure. We believe that the initial improvement of the diode trace by a short anneal may be due to the removal of point defects produced during ion beam doping.

This calculation leads to surprisingly high values of N_t , typically 10^5 nm^{-1} of misfit line length. This is much greater than the total number of potential sites along the misfit segments by a factor of 10^4 to 10^5 . It is therefore clear that a model in which the only sources are special sites along the dislocation cores can not explain these data. The large number of traps we calculate must therefore be distributed over an extended volume around the cores, of at least 10 - 100nm in diameter and probably much greater. The traps may thus be associated with point defects in the material. The concentration of point defects is likely to be much higher around dislocations than in the bulk because of high defect-dislocation binding energies, leading to reduced formation energies (as have been calculated for bcc [9] and fcc [10] metals). Alternatively the traps may be associated with the *threading arms* as follows: as the dislocations propagate, the threading arms sweep through a volume defined by a (111) plane and of thickness determined by the threading arm Burgers vector, and the traps may be related to point defects remaining after the passage of the threading arms through this volume; EPR studies suggest that high point defect densities are in fact present following the motion of dislocations [11]. Even in this case, however, given the depletion layer widths in our materials there is still a shortfall of potential sites unless the thickness of the disturbed region is at least 10 - 100nm.

However, the presence of metal impurities is likely to be of even greater importance in these experiments. Even very low levels of metal impurities are known to have a significant influence on the electrical activity of dislocations, as observed for example by cathodoluminescence [12] and electron beam induced current [13]. Transition metal impurities in silicon display a large range of diffusion coefficients [14], and diffusion along dislocations is likely to be much faster than through the perfect lattice because of the enhanced concentration of point defects. Diffusion will be comparable with the speed of propagation of the dislocations at 700°C for any metal with a diffusion coefficient greater than about $10^{-10} \text{ cm}^2 \text{ sec}^{-1}$ at this temperature (for example Fe, Cu [14]). Thus diffusing metal species may decorate either the planes of the threading arms or the misfit dislocation cores themselves as the dislocations propagate, giving rise to traps with different cross sections and energy levels. We are presently applying deep level transient spectroscopy to determine the energy levels of traps associated with the dislocations in these GeSi/Si diodes. We are also carrying out experiments in which the GeSi/Si interface is placed at different distances from the depletion region, so that the effects of the threading arms and the misfit segments can be examined separately.

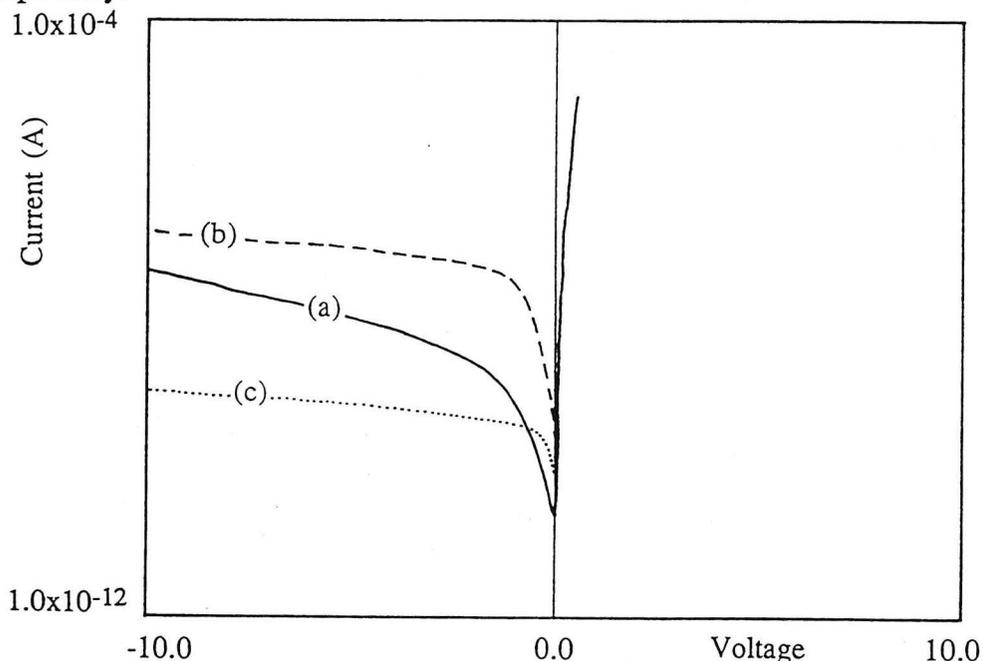


Figure 3. Calculation of the efficiency of dislocations at generating current. I-V curves show the changes in the diode characteristic of a $100\mu\text{m} \times 100\mu\text{m}$ patterned metallised diode after *ex situ* heating. The structure is as shown in figure 1 but with 25%Ge. (a) As received; (b) After 8 minutes heating at 740°C , which led to a dislocation density of $0.47\mu\text{m}^{-1}$; (c) Si control structure after the same heat treatment. Comparison of (b) and (c) suggests a current density of $1 \times 10^{-5} \text{ A per meter of misfit dislocation at } -5\text{V}$.

It is clear from the preceding discussion that it is advantageous to avoid dislocations in the active regions of devices. In this context we have found that the degree of relaxation of a metastable heterostructure depends strongly on the processing steps which it has undergone during its formation into a working device. To quantify this relationship we have examined the relaxation kinetics of a series of specimens which have undergone different processing steps, and we now present preliminary results from this study.

One group of specimens was formed from metastable GeSi/Si heterostructures unprocessed apart from ultrasonic cutting into 3mm discs and chemical thinning to form electron transparent regions. On some of these wafers 20nm W films had previously been deposited, by room temperature sputtering, with either compressive or tensile strains. The strain in the metal overlayer was controlled by varying the Ar pressure during sputtering [15] and both this and the strain in the GeSi layers were determined using wafer curvature measurements. We compared the relaxation kinetics of the unprocessed specimens with both the metallised specimens and the patterned, fully processed devices described above.

We firstly discuss relaxation kinetics in unprocessed structures. The velocity of existing dislocations is known to follow an Arrhenius law with an activation energy of about 2eV [6] and a prefactor which depends on the excess stress in the layers [16]. Typical velocities in the materials we have examined are of the order of 0.1 - 1 microns per second at 550°C and 10 microns per second at 700°C. However the *nucleation* of dislocations is not well understood and appears to be material dependent. The as-grown dislocation density in our materials was in the range $10^3 - 10^4 \text{ cm}^{-2}$ (i.e. at the detection limit for TEM). In the wafers with the highest densities, we found that the source for most of these dislocations consisted of polycrystalline silicon inclusions 2-4 μm in diameter, present at a concentration of about 10^4 cm^{-2} , which were probably debris flaked from the chamber walls during growth. In the low (<~1%) strain regime we do not expect homogeneous nucleation to occur and therefore most dislocations nucleate from such heterogeneous sources or from the edge of the specimen.

On heating, more dislocations appear, as in figure 1a. However even at increasing temperatures the increase in relaxation rate is not as fast as we would expect from consideration of dislocation velocity activation energies alone. This suggests that the nucleation of dislocations, rather than their growth once formed, is the rate limiting step in the relaxation process. We derive further evidence for the importance of nucleation sites by comparing the relaxation rates of capped and uncapped structures. We find that for a significant degree of relaxation, such as 10%, to occur within say 10 minutes, capped (i.e. Si/GeSi/Si) structures must be raised about 100°C above the growth temperature but uncapped (GeSi/Si) comparable structures only about 50°C. Furthermore, the relaxation of capped structures is less uniform with time and we observe waves of parallel dislocations which appear to come from an extended source, such as the edge of the specimen. Unlike the case of uncapped layers, surface imperfections can not act as sources and this lack of nucleation sites limits the rate of the relaxation process.

A comparison of relaxation rates of unpatterned and patterned structures confirms the importance of nucleation. Etched, metallised diodes show a surprising improvement in their stability to degradation. We find no change in electrical properties up to near 800°C, where the rectifying behaviour disappears (figure 4a). At about this temperature we see occasional dislocation formation (as in figure 1b) but most significantly a catastrophic roughening of the Ti-W/Si interface (figure 4b). The Ti-W-Si system is known to be stable to above 750°C when a ternary silicide $\text{Ti}_x\text{W}_{1-x}\text{Si}_2$ is formed [17, 18], and the large volume change (about 25%) associated with this reaction could account for the roughening we observe. To appreciate the extreme enhancement of stability which this represents, remember that dislocations will appear (over similar time scales) in the same metastable GeSi structures, before patterning, at temperatures about 200°C lower.

It is known that deposition onto patterned substrates decreases the dislocation density observed in the InGaAs/GaAs [19] and GeSi/Si [20] systems, because of the areal reduction in the nucleation opportunities for dislocations. However, in our experiments other features of the patterning process may also enhance the stability: there may be fewer dislocation sources on the well-passivated edges of these mesas; edge relaxation effects may ensure that sufficiently small mesas do not build up sufficient stress to drive dislocations (although this is important only for mesas of lateral dimensions less than about ten times the epilayer thickness [21], i.e. < 2 μm in this case); and finally the stress in the Ti-W film, particularly at the mesa edges, may also diminish or

remove the driving force for the formation or motion of dislocations. This effect is likely to be very significant because room temperature sputtered films of pure W are generally under a high stress, of the same order of magnitude as the stresses expected in the GeSi/Si structure itself (about 10^8 - 10^9 Pa), and whose sign depends sensitively on the deposition conditions [15].

To assess the importance of overlayer stress effects, we have compared the relaxation kinetics of GeSi/Si heterostructures on which compressive and tensile W layers have been sputtered, with results shown in figure 5. We find that the sign of the stress in the metal overlayer can alter both the onset of relaxation as well as the ultimate dislocation density.

For an infinitely large system, it is clear that a uniformly stressed overlayer can not influence the relaxation kinetics. (A non-uniform stress can influence dislocation movement, but since any non-uniformities in the stress in these films are likely to be on the order of the grain size, which is about the film thickness $t_w = 20\text{nm}$, such strain fields are not likely to penetrate deeply enough into the semiconductor to cause a significant effect.) We thus suppose that the strain in the metal is only important at the edges of the mesa. Preliminary finite element calculations support this conclusion. We have calculated that the W overlayer alters the stress in the GeSi layer within a region of width about $10t_w$ from the edge of the specimen. (We also calculate that because of substrate relaxation the stress is altered in regions where $t_{Si} < \text{about } 10t_{\text{GeSi}}$, i.e. at the edges of the electron transparent regions. This is not a consideration in results such as [3] where typically much thinner GeSi layers were used.) Given the importance of edge nucleation in these devices, we suggest that a strain in the metal of the correct sign can reduce or enhance the probability of formation of dislocations at the mesa edge. However we do not yet understand the intriguing reversal in behaviour we observe for capped and uncapped structures in figure 5.

If it is the stress in the metal overlayer which determines the stability of these strained systems, the possibility of controlling this stress by choosing appropriate metal deposition conditions suggests the interesting though speculative idea of engineering the stability of strained heterostructures via subsequent processing conditions.

CONCLUSIONS

We have demonstrated that it is possible to measure diode characteristics and dislocation behaviour simultaneously during the relaxation of strained layer p-n junction diodes in the transmission electron microscope. The correlation we observe between electrical degradation and the formation of misfit dislocations can be used to probe the electrical behaviour of the dislocations. We suggest that in our system electrically active defects are distributed widely around dislocation cores, or that the motion of threading arms is a significant feature of the degradation process, in terms of the creation of defects or the diffusion of metal impurities into the depletion region.

It is apparent in these experiments that the opportunities for dislocation nucleation have a dominant role in determining the overall relaxation kinetics of metastable structures. The way in which a strained layer material is fashioned into a device is significant in determining the amount of relaxation, and therefore the electronic quality of the finished result.

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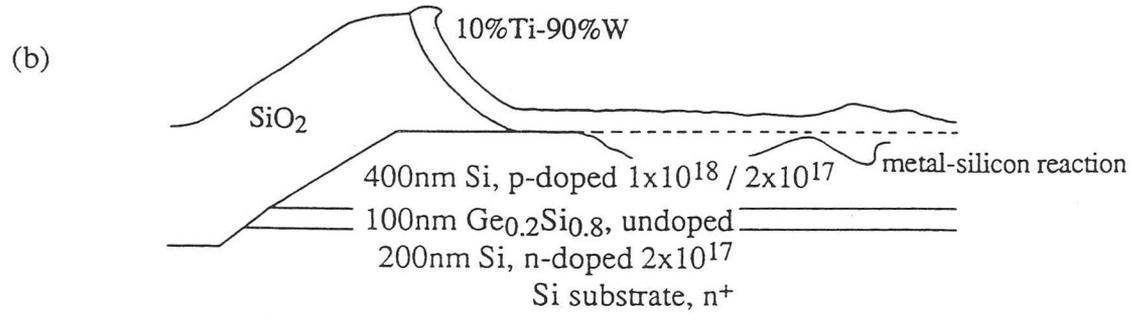
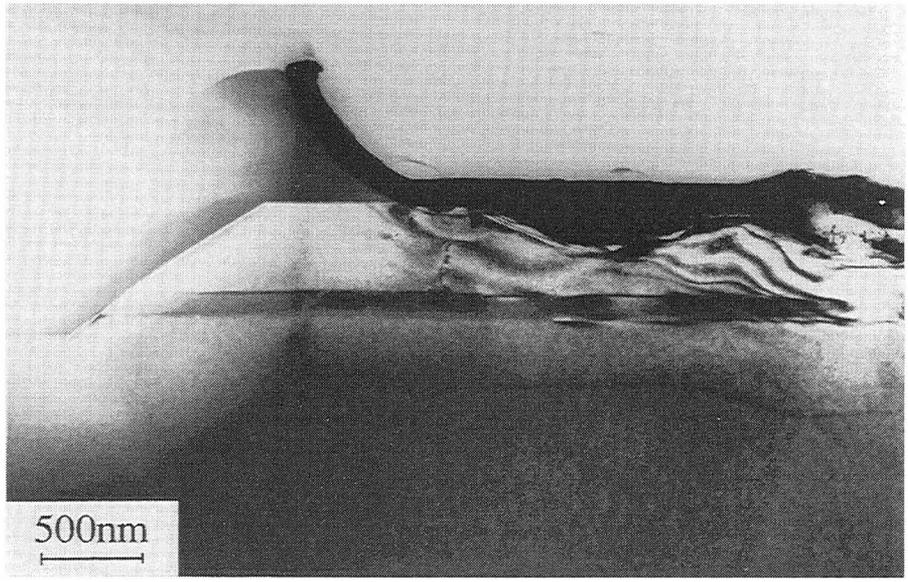
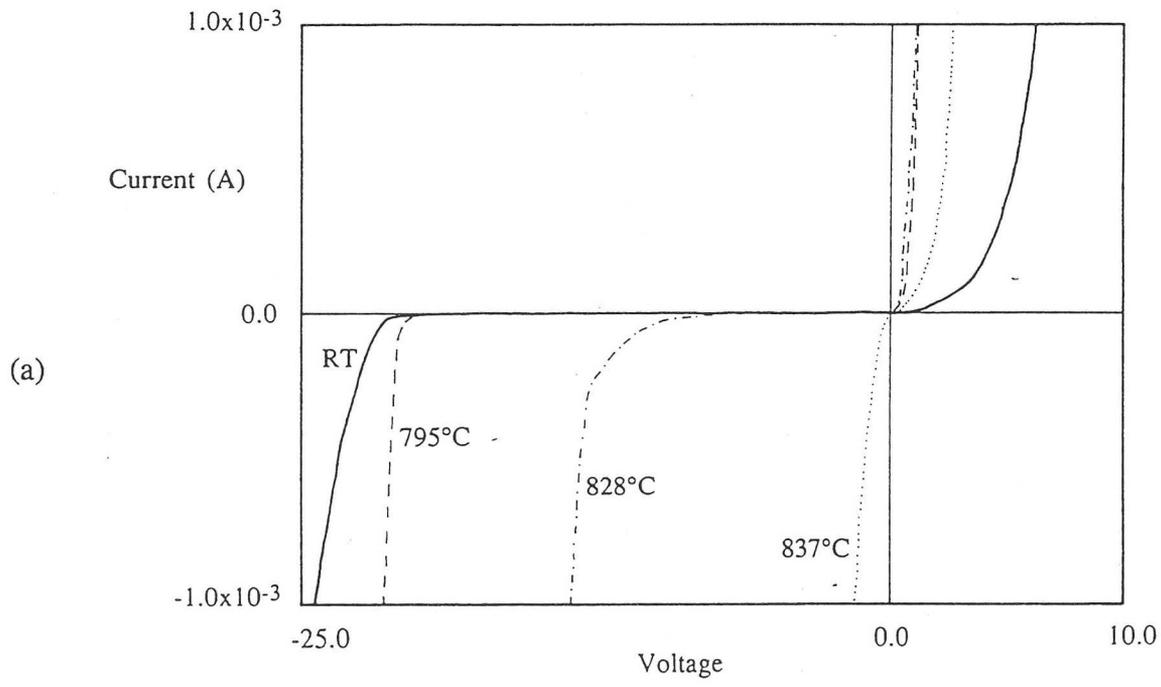


Figure 4 (a) Stability of a patterned, 500x500 μ m diode. Current-voltage characteristics are shown after heating cycles of 14 minutes at the temperatures indicated.
 (b) Bright field 022 cross sectional image of an identical diode after heating to 837 $^{\circ}$ C for 14 minutes.

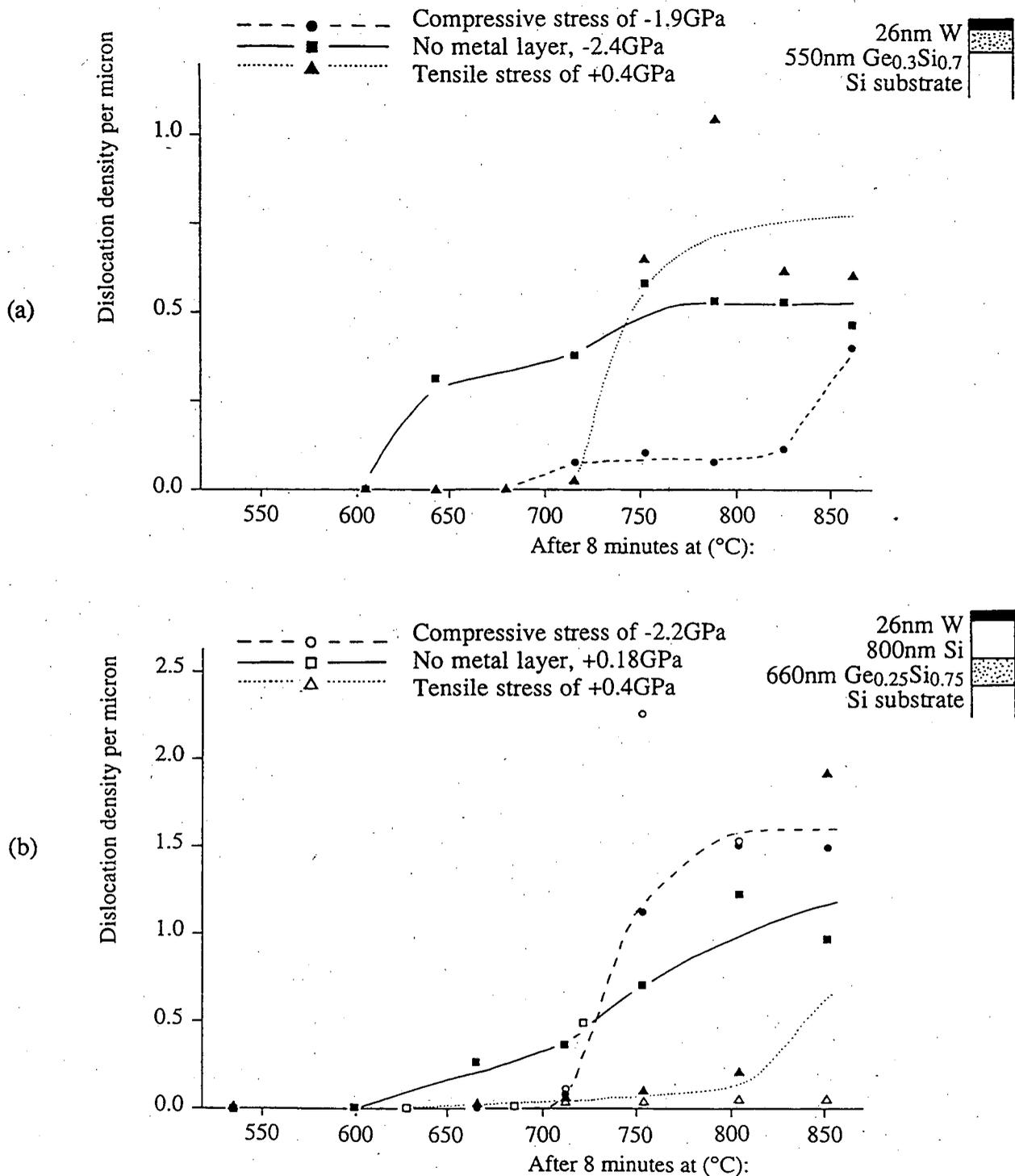


Figure 5. Dislocation density observed in the (a) uncapped and (b) capped GeSi/Si heterostructures specified in the insets. Specimens were successively heated *in situ* for 8 minutes at each of the temperatures indicated and the number of dislocations cutting a line was measured by averaging over several fields of view. The dislocation density was examined in areas at which the substrate thickness was of the order of ten times the overlayer thickness, as the stress terms there are within 10% of the values for an infinite substrate. The lines are for guidance only as the small numbers of dislocations observed result in a large statistical scatter. Filled and open circles in figure 5(b) correspond to two different specimens. Note that dislocation densities of 20 and 25 μm^{-1} respectively would correspond to complete relaxation of the two structures.

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