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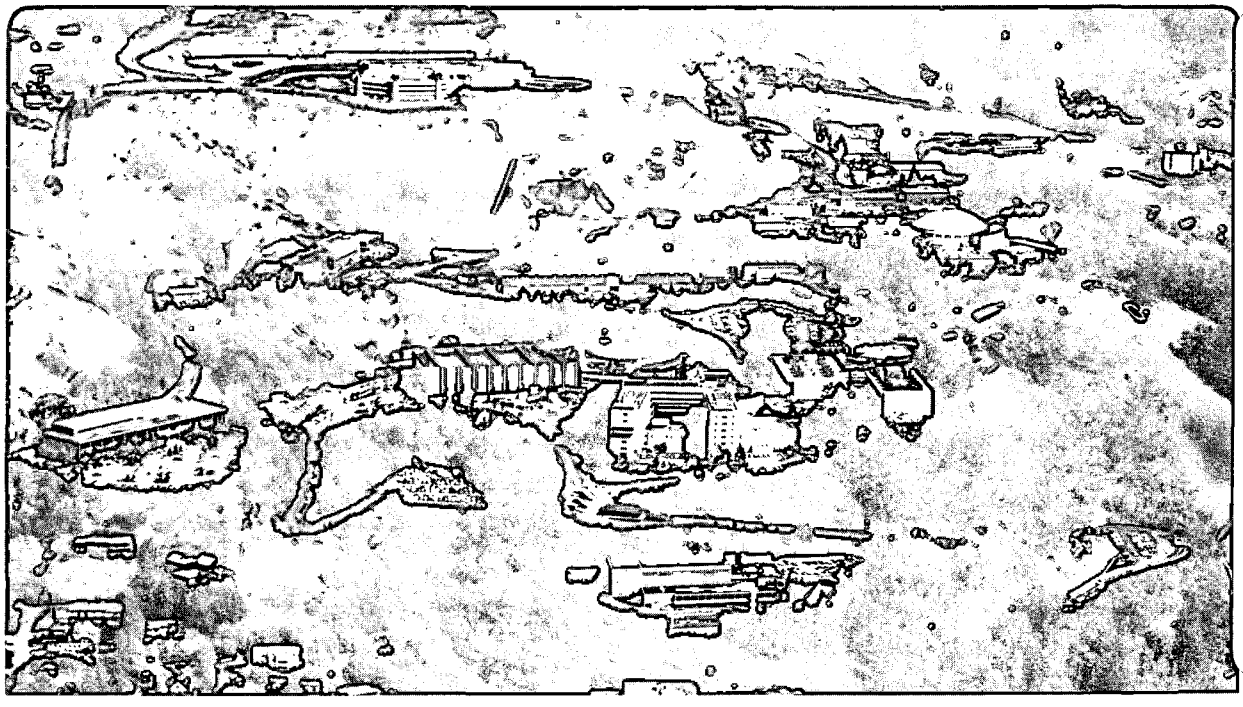

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Abstract

A fully integrated CMOS pulse shaping amplifier has been developed at LBL. All frequency dependent networks are included on the chip. Provision is made for tuning to compensate for process variations. The overall architecture and details of the circuitry are discussed. Test results are presented.

INTRODUCTION

The design of this chip relied on an analysis of the Equation of State (EOS) TPC shaping amplifier(14) and is an attempt to improve on that basic design. The EOS TPC shaping amplifier utilizes one high pass section followed by 4 low pass sections, all with the same time constant. All poles are real.

It was soon determined from SPICE simulations of the existing design that improved performance could be achieved if the four real low pass poles of the EOS TPC design were replaced by two identical complex pole pairs. This determination is confirmed by Fairstein (1) and others.

In any integrated circuit design, the circuit techniques available to the designer are severely constrained by the particular semiconductor process to be used. In the present case, this was the Orbit CMOS p-well, 2 micron, 2 poly, 2 metal process. This process, using +5 and -2 volt supply rails, made possible a new efficient circuit configuration using a fast operational amplifier and active filters utilizing high speed voltage followers. No part of the original discrete bipolar EOS TPC shaper circuitry was duplicated in the new configuration.

The Orbit process accommodates CMOS active devices of dimensions from 3x2 microns to an arbitrarily large size (384x4 microns is the largest used here). Resistors and capacitors are of polysilicon material. A sheet resistance of 19.2 ohms per square permits reasonably sized resistors while parallel plate capacitors are made of two layers of polysilicon material and have a capacitance of .451 femtofarads per square micron ($fF/\mu m^2$). Resistors of up to 20,000 Ohms and capacitors of up to 30 picofarads (pF) were used in this design.

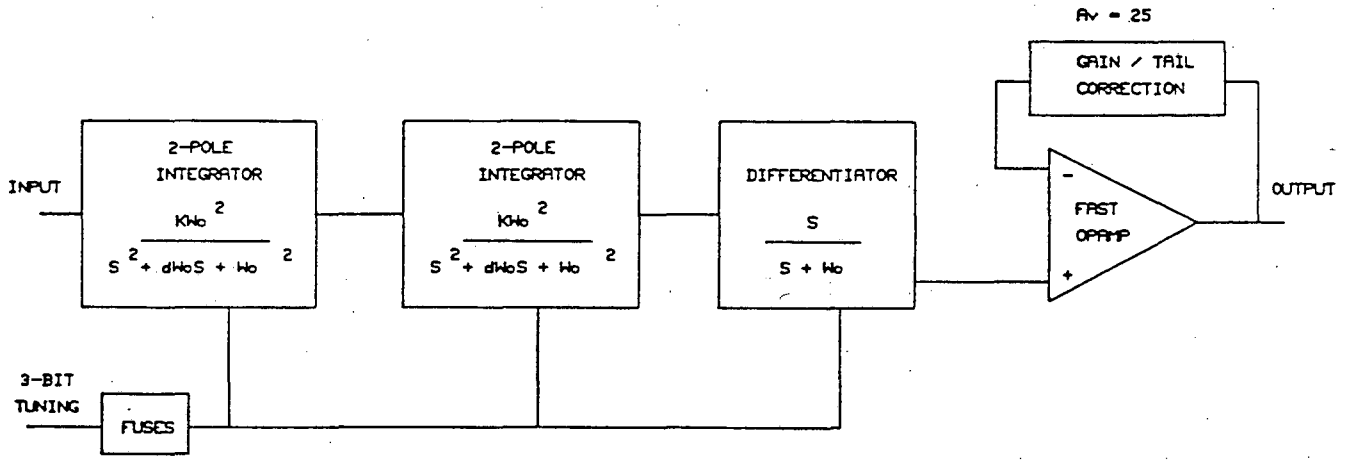

Fig.1. 16 Channel Multipole Pulse Shaping Amplifier Block Diagram

A principal objective of the design was that no external parts be necessary for its operation. This required that the architecture be organized around practically realizable and reasonably compact on-chip RC networks and active filters.

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SYSTEM ARCHITECTURE

Figure 1 is a block diagram of the 16 Channel Shaper. The first two stages are complex pole pair integrators utilizing low gain single stage amplifiers. The third stage is a passive differentiator, contributing a zero at zero frequency and a pole at W_0. The result is a shaping network with 5 poles and one zero.

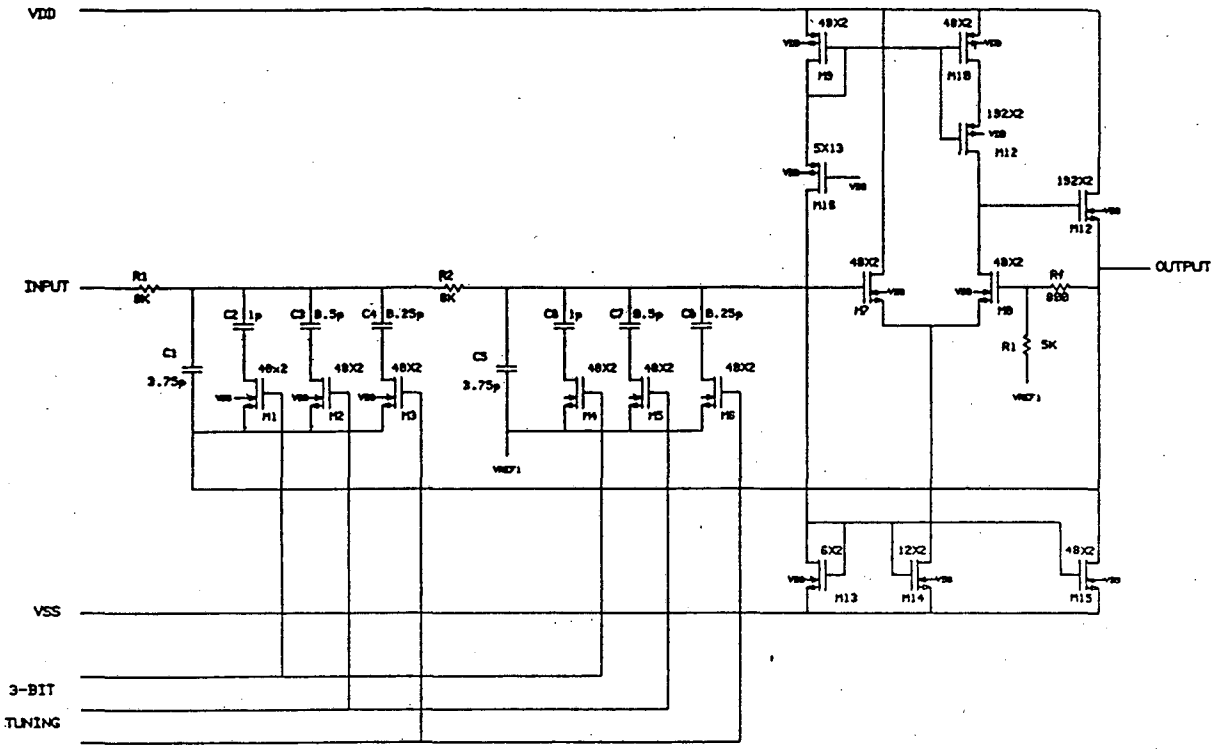

Fig. 2. Integrator With Complex Poles

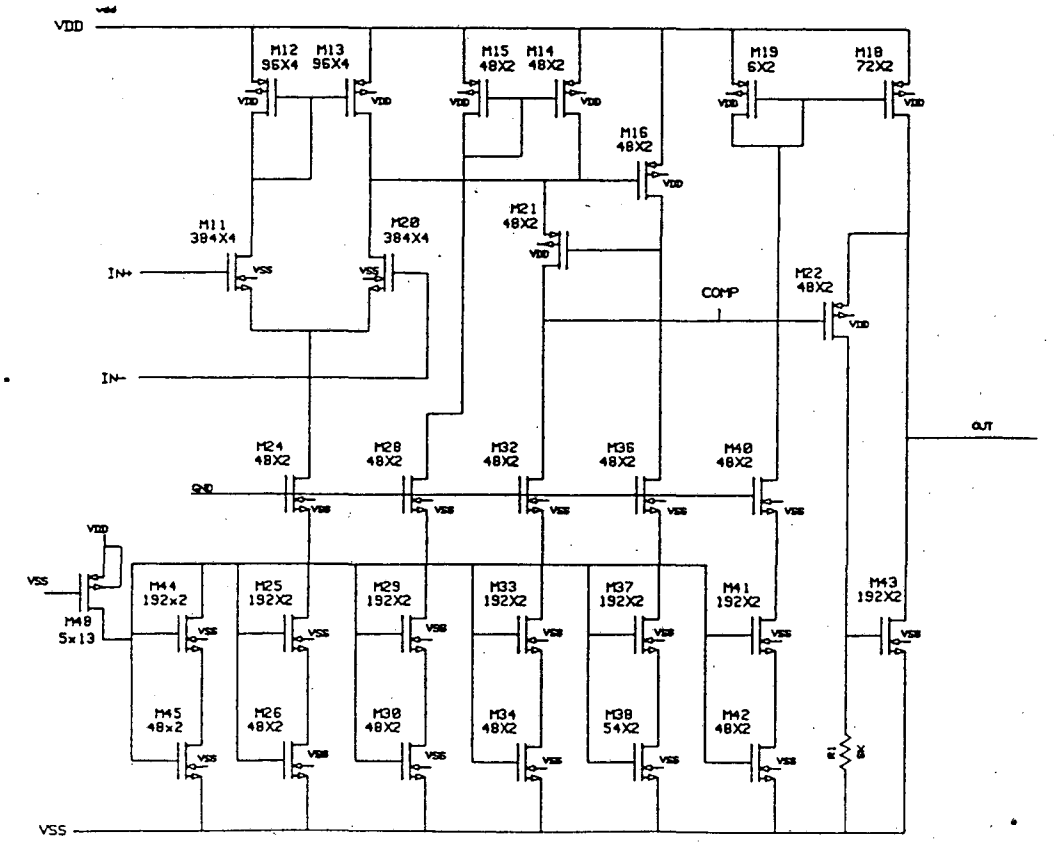

Fig. 4. High Speed Operational Amplifier

Because of the tolerance of on-chip capacitors and resistors, provision is made for fine tuning the peaking time by means of a three-bit binary code. All RC networks have identical values for R and for C and are tuned by switching in padding capacitors. The tuning range is about +/- 20% and tuning is accomplished during chip test by the burning of on-chip fuse links.

The output section utilizes a high speed operational amplifier capable of a bandwidth of better than 20 MHz at a closed loop gain of 25 and having a slew rate of over 100 V/Usec. This opamp was specifically designed for fast analog applications utilizing the CMOS process and +5V and -2V power supply rails. It has a low impedance output stage capable of providing a 3 volt output swing into a 20 pf load. Response is critically damped under a variety of gain and load conditions. The tail correction network (described later) has a rather long time constant and for this reason is placed in the feedback loop of the output amplifier, where circuit impedance is highest, minimizing the size of the required on-chip capacitor.

The circuit of Fig. 1 places the differentiator downstream from the integrators, allowing the dc level of the output amplifier to be set externally and so that the DC offset of the upstream stages is not amplified. Further, the placement of the integrators early in the circuit puts a low pass filter in front of all circuits and reduces effects of the slew limiting behavior of amplifier stages presented with fast rise input signals(11). From a small signal standpoint, of course, the order of placement is immaterial. The positioning of the gain stage at the output is less than optimum in that the broad band noise generated by the amplifier appears unfiltered at the output. This placement is a small compromise and is dictated by overriding circuit design considerations.

INTEGRATOR STAGE WITH COMPLEX POLES

The complex pole pair circuit used in the active integrator is shown in Fig. 2. M7-M15 constitute a simple wideband amplifier capable of stable performance when connected for unity gain. When used as a voltage follower, the amplifier nominally has a risetime of 7 nanoseconds and a gain of 0.98. The amplifier is linear within a percent over an input range of -.5 to +2.5 volts and is connected here as the active element of a Sallen - Key filter (3).

With this type of active filter, the position of the pole pair in the s-plane depends on the damping factor, d. The damping factor is defined as:

$$d = (R_f - 2R1) / R1$$

With the ratio $R_f/R1$ set at zero (i.e., $R_f=0$), the damping factor d is 2. This corresponds to a pair of real poles. As $R_f/R1$ is increased, the damping factor d decreases and the poles split and move vertically away from the real axis, describing a circle in the s-plane. As $R_f/R1$ approaches 2, d approaches zero. At d=0, the circuit becomes completely undamped, with the poles lying on the imaginary axis of the s-plane.

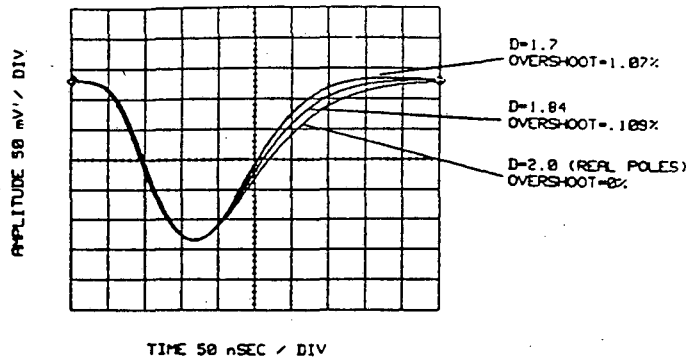

Fig. 3. Shaping Improvement Using Complex Poles

Fig. 3 shows the response of a five pole, one zero shaping amplifier (four integrator poles and a differentiator pole-zero pair) as the damping factor d of the integrator poles is varied. In this figure, the amplitude of the signals has been normalized. As the damping is decreased from a value of 2, the symmetry of the quasi-gaussian waveform is improved markedly. This improvement is accompanied by an increased overshoot which varies from 0 to +1.07% as the damping factor decreases from 2 to 1.7.

The question of how much overshoot can be tolerated in a pulse shaping amplifier is not simple. Normally, overshoot on the trailing edge of the shaped pulse is to be avoided. On the other hand, a certain amount of overshoot is sometimes used in shaping amplifiers as part of the tail correction compensation. In the design of the shaping amplifier discussed here, overshoot is held to about 0.1%, resulting in a corresponding modest improvement in pulse symmetry over an earlier pulse shaper design having 4 real integrator poles. In this design, with complex poles, the tail correction compensation is accomplished in the feedback network of the output amplifier. Future iterations may utilize some of the overshoot of the complex pole pairs as part of the tail correction, allowing further improvement in pulse symmetry.

OUTPUT AMPLIFIER STAGE

The Output Amplifier provides a voltage gain of 25. It must be capable of driving the (primarily capacitive) load of the SCA (switched capacitor array) chip as well as a significant stray lead capacitance. It must be capable of reproducing gaussian waveforms of less than 200 nanoseconds FWHM (full width half maximum) at amplitudes of three volts. This performance requires a closed loop bandwidth of better than 20 MHz at the required gain, a slew rate of better than 50 volts per microsecond, good stability when driving the required load capacitance (20-30pF), and an open loop gain of at least 70 db (Av=3000).

Recent CMOS operational amplifier designs (6) (8) (12) rely heavily on so-called "rail to rail" geometries, where the output stage is composed of complementary devices each connected in the common source configuration and with drains joined at the output. A rail-to-rail design was considered for the application and was rejected for several reasons. In

general, bandwidth and stability are degraded when these designs are subjected to capacitive loading. Further, the gain-bandwidth product of current rail-to-rail designs was found to be inadequate for the purpose.

The most serious drawback to the use of a rail-to-rail opamp in buffer applications is the high open loop output impedance of the open drain output stage. When these designs are loaded capacitively, an extra pole in the feedback loop results at the frequency where the open loop output impedance breaks with load capacitance. This leads to AC instability and requires increased compensation, which in turn further limits the slew rate. While some rail-to-rail designs are capable of impressive output currents(12), there is no substitute for low small signal open loop output impedance when a feedback amplifier is used in buffer applications.

The Output Amplifier used here is an enhanced gain single stage design using a compound source follower output stage capable of linear operation to within 1 volt of the +5v and 0v rails. Open loop output impedance is approximately 120 ohms (SPICE simulation), several times lower than rail-to-rail designs. Gain enhancement is accomplished by the use of an active (or "regulated") cascode stage which effectively decouples the gain from the gain-bandwidth product(7)(8). All the advantages of a single stage amplifier (stability, ease of comparison) are retained.

Fig. 4 is a schematic of the High Speed Operational Amplifier used in the output section. The supply voltage are -2.0 volts and +5 volts. The output stage, composed of M22 and M43, is a compound source follower. It has the advantage in this circuit of shifting the DC level of the output + 1.5 volts up from the high impedance load point at the drains of M21 and M32. The input differential pair, M11 and M20, run at 50 microamperes and drive the source of M21, part of the active cascode formed by M14, M16, and M21. This arrangement provides a very low impedance load to the output of M20 and at the same time provides a very high output impedance at the drain of M21. The high output impedance of the active cascode stage is matched by the high impedance load of the triple cascode M32, M33, and M34.

The open loop gain of a single stage amplifier with a transconductance gain of g_m and output load impedance Z_o is, from many sources, the expression

$$A_v = g_m \cdot Z_o \quad (13)$$

Neglecting the frequency response of the high speed source follower output stage, this is a good approximation of the overall open loop gain of the Op Amp. Zo is a complex quantity with a single pole at the frequency where the parallel resistance of the active cascode and its parallel load resistance break with its shunt capacitance so that, assuming that g_m is constant and real over the range of the frequencies of interest,

$$Av(s) = g_m \cdot [R_o/(R_o C_o s + 1)].$$

Where s is the complex frequency variable, $s = \sigma + j\omega$.

SPICE simulations and experimental tests confirm the well behaved single pole response of this Operational Amplifier. At a closed loop gain of 25, and driving a 20 pf load, the amplifier requires no compensation and has a frequency response flat to 23 Mhz with virtually no peaking. The pulse response under these conditions is critically damped with a risetime better than 20 ns.

TAIL CORRECTION

The shaping amplifier is driven by a charge sensitive preamplifier which amplifies the output of an anode pad of the Time Projection Chamber. The anode pad response is dominated by the flow of positive ions and their secondary and tertiary avalanche currents. The resultant waveform is a strong function of both the ambient temperature and electrode voltages of the chamber and bears no resemblance to the simple step waveforms produced by laboratory signal generators. For this reason, a shaping amplifier which is designed to produce an acceptable guassian waveform from step functions will produce a distorted output when processing an actual chamber signal.

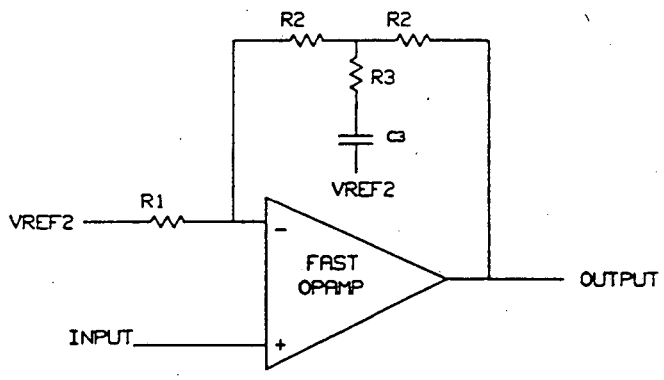

Figure 5. Tail Correction Network

In this shaping amplifier, as in the CERN experiment at HERA NA35/EOS-TPC shaping amplifiers, a first order correction network is used for tail correction. The network is shown in Fig. 5. The transfer function of this network is of the form

$$Vo(s)/Vi(s) = K2 \times [T1s + 1)/(T2s + 1)] \quad \text{where } T1 > T2.$$

To determine the time constants used in the shaping amplifier, data from the TPC simulator at CERN was first used to construct a SPICE waveform generator which duplicated the actual measured current from an anode pad. This signal was then integrated and used to drive a simulated shaper amplifier, and the time constants of the tail correction network were adjusted to minimize the waveform aberration. The reason for this approach is the relative difficulty of obtaining an analytic solution to the tail correction problem.

Using this approach, the best time constants for the tail correction network were found to be T1=277 ns and T2=185 ns. Before optimization of the tail correction network, the

shaper exhibited a 5% undershoot at 500 ns past the peaking time (180 ns nominal). This performance was measured on actual parts on the TPC simulator at CERN, and was also verified by SPICE simulations. After optimization of the tail correction network, SPICE simulations showed an overshoot of 0.48%. This is an improvement of a factor of ten over the uncompensated IC.

Tests on the LBL test chamber gave the expected degree of tail correction for the optimized chip. However, later tests on the actual NA49 chamber indicated that the tail correction was less effective, showing a residual overshoot on the pulse trailing edge of about 2%. It appears that the correction required is a strong function of chamber design, and to a lesser extent, of the gas mixture used.

OVERALL PERFORMANCE OF INTEGRATED SHAPER AMPLIFIER

Over the previous year, several runs of 16 channel shaper amplifiers were produced. Tests of 672 channels of shaper amplifier are summarized in Table 1. Three key parameters were investigated. These parameters were DC output level, pulse amplitude, and shaping time. Average, maximum, and minimum values and standard deviations within each run for each of these parameters were computed. Yield of certain parameters was found to be improved by selection, and for two of the runs (N26E and N29X) some "bad" channels were eliminated. Whenever a channel was eliminated, data for the entire chip was thrown out, and the yield ("Performance Yield") was recalculated. The low functional yield (44%) indicated for run 075AH was due to a single wafer with a large number of non functional parts. Chips from other wafers in run 075AH were separately tested and found to have yields consistent with the other two runs. Because of minor circuit changes, run N29X has slightly higher gain than the other two runs. Standard deviations of all tested parameters fell well within project design goals.

Other parameters of interest are power supply current, noise, and crosstalk. Average power supply current for the Shaper Amplifier chip is 43 milliamperes, or 2.7 milliamperes per channel. Noise and crosstalk have been measured in conjunction with a charge sensitive preamp.

	N26E 20 IC's 320 ch	N26E 17 IC's 272 ch	075AH 11 IC's 176 ch	N29X 11 IC's 176 ch	N29X 9 IC's 144 ch	N29X 7 IC's 112 ch
Functional Yield	100%	-----	44% of Wafer 1	92%	-----	-----
Performance Yield	100%	85%	100%	100%	82%	64%
Test V2ref	3.0 v	3.0 v	3.2 v	3.2 v	3.2 v	3.2 v
Input Pulse Level	300 mv	300 mv	300 mv	240 mv	240 mv	240 mv
DC Output Voltage Level						
Avg (volts)	3.01	3.00	3.15	3.16	3.16	3.16
Max (volts)	3.63	3.50	3.37	3.69	3.55	3.53
Min (volts)	2.45	2.59	2.92	2.66	2.77	2.86
Std dev (volts)	0.18	0.16	0.09	0.16	0.16	0.15
Output Pulse Amplitude						
Avg (volts pk)	1.95	1.95	1.84	1.79	1.79	1.79
Max (volts pk)	2.06	2.06	1.94	1.86	1.86	1.86
% of Avg	6.01 %	5.69 %	5.45 %	4.08 %	4.11 %	4.09 %
Min (volts pk)	1.75	1.84	1.77	1.70	1.70	1.70
% of Avg	-10.01 %	-5.53 %	-3.91	-4.66 %	-4.63 %	-4.64 %
Std dev (volts pk)	0.05	0.05	0.03	0.03	0.03	0.03
% of Avg	2.65 %	2.45 %	1.45 %	1.66 %	1.74 %	1.82 %
Peaking Time						
Avg (nanosec)	196.26	196.22	191.37	175.52	175.79	176.48
Max (nanosec)	212.00	212.00	198.00	184.00	184.00	184.00
% of Avg	8.02 %	8.04 %	3.46 %	4.83 %	4.67 %	4.26 %
Min (nanosec)	185.00	185.00	183.00	168.00	168.00	169.00
% of Avg	-5.74 %	-5.72 %	-4.37 %	-4.28 %	-4.43 %	-4.24 %
Std dev (nanosec)	6.15	6.06	3.11	3.60	3.63	3.27
% of Avg	3.13 %	3.09 %	1.63 %	2.05 %	2.07 %	1.85 %

TABLE 1.

Tests of Three Runs of 16 Channel Shaper IC's

A preamp/shaper chip embodying minor changes in the design presented here had an equivalent input noise of about 900 electrons with 14pf total input capacitance. Crosstalk, difficult to measure because of the crosstalk inherent to any test fixture, is measured at approximately 0.34% between adjacent channels. Crosstalk between non-adjacent channels is no more than half this amount.

FUTURE APPLICATIONS OF 16 CHANNEL SHAPER AMPLIFIER

Requirements of the NA49 and STAR project were for an integrated preamplifier/shaper chip. The shaper amplifier discussed here was designed to be compatible in both processing and signal levels with an existing integrated preamplifier design developed at LBL and already in use in several applications(14). In late 1992, a chip was produced at LBL which combined the two circuits in a 16 channel form. After some circuit refinements were added, which reflected the results of actual chamber tests at CERN, the preamp/shaper chip (PASA4) was deemed to meet NA49 specifications. The STAR project, which has different specifications, is seeking further design refinements at the time of writing of this paper.

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