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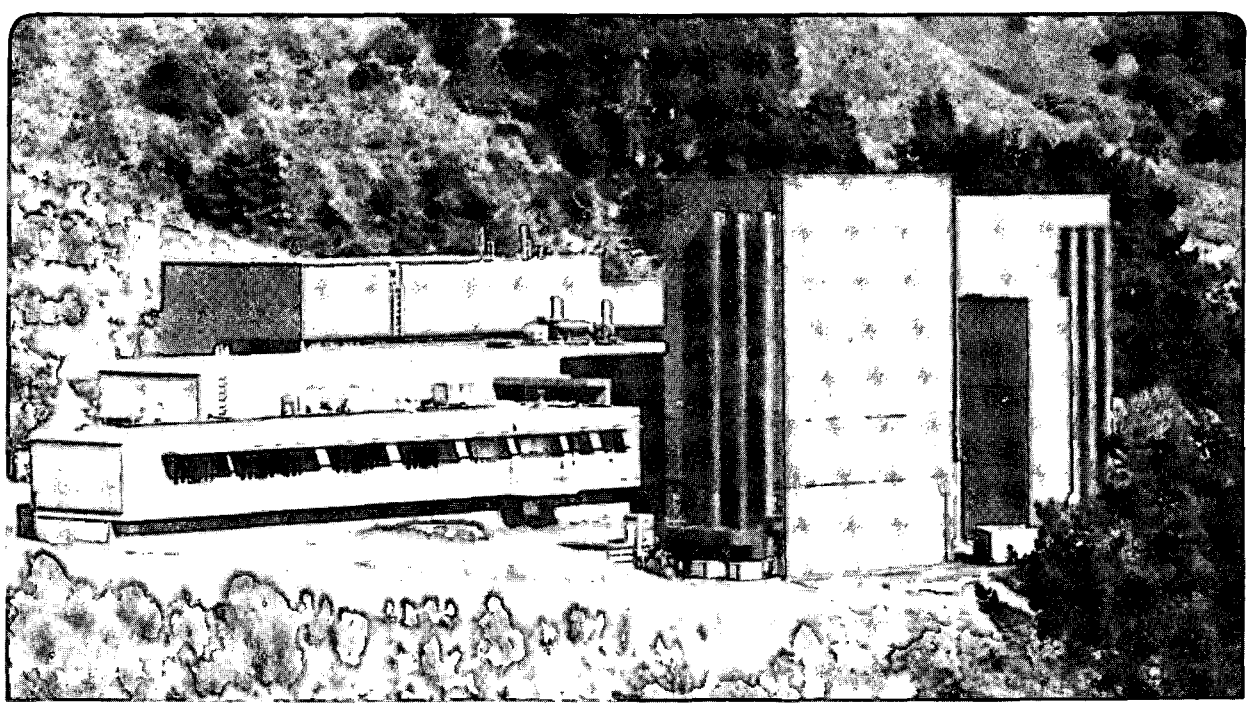

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Selected Area Polishing for Precision TEM Sample Preparation

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KEY WORDS TEM, Tripod polisher, Device failure analysis

ABSTRACT

A selected area mechanical polishing technique has been developed to improve the precision of cross-sectional TEM sample preparation, based upon the early work of Benedict *et al.* (1990). TEM samples were made from a pre-selected section through the middle of a 1 μm wide band of transistors extending laterally for more than 1 mm by precise control over the plane of polish with a corresponding reduction in sample preparation time. To illustrate the application of this technique, a uniformly-thin, electron transparent TEM sample of a single, specific, failed transistor is obtained from a 4 mm by 10 mm device array.

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INTRODUCTION

The rapid development of the semiconductor industry continues to demand device failure analysis with increasing spatial resolution. Scanning electron microscopy is still the most widely accepted technique for this application; however, the improved spatial resolution and image contrast of the transmission electron microscope (TEM) has compelled many laboratories to explore the use of this "research" instrument for both process development and failure analysis. To be successful, accurate TEM sample preparation is of paramount importance. For example, TEM cross sections may be required of a specific pre-determined feature of a single transistor that has failed. The difficulty of single-bit failure analysis obviously increases even more as submicron technology emerges as the standard in device fabrication. It is important, therefore, to have precise control over all aspects of the sample preparation process for future failure diagnostics.

During the past decade, there has been a surge of technical papers on TEM sample preparation for VLSI semiconductor device analyses. Klepeis *et al.* (1988) have pioneered the use of a Tripod Polisher[1] for accessing a pre-selected submicron area and mechanically reducing it to less than 60 nm thickness. The present work refines this method by incorporating dynamic observation of light interference fringes to monitor and control the polishing process at the 10nm level.

PRINCIPLES OF OPTICAL INTERFERENCE

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[1] The Tripod Polisher™ is manufactured and distributed by South Bay Technology, 1120 Via Callejon, San Clemente, CA 92672 (714) 492-2600.

The principle of light interference to monitor the flatness of the sample is illustrated schematically in Figure 1. A glass cover slip is placed into contact with the surface of the polished sample so that the air gap between the bottom surface of the glass and the top surface of the sample has dimensions on the order of the wavelength (λ) of visible light (about 550nm). Light reflected from these two specular surfaces interferes to produce patterns of constructive (light path difference of even times of $\lambda/2$) and destructive (light path difference of odd times of $\lambda/2$) interference that appear as fringes, which map the contours of the polished surface. Since each interference fringe corresponds to a path difference of one half wavelength of light, these contours can be measured quantitatively. For example, at fringe number n=0 the glass and sample are in contact where the air gap distance $\Delta t=0$; at fringe number n=1 the first dark fringe occurs because $2\Delta t=\lambda/2$ (the factor of two is used because the beam reflected from the top surface of the sample goes through the air gap twice); at fringe number n=2 the first bright fringe occurs because $2\Delta t=\lambda$; at fringe number n=3 the second dark fringe occurs because $2\Delta t=3\lambda/2$, etc. To calculate the air gap distance, simply number (n) all fringes (dark *and* bright) and apply the formula $2\Delta t = n\ (\lambda/2)$. The air gap distance ($\Delta t$) at the position of the fourth dark fringe (n=7) is therefore

$$\Delta t = 7\ (\lambda/2) = 7\ (550/2)/2 = 962.5\text{nm}$$

or approximately 1 μm. In practice, count only dark *or* bright fringes. The formula because $\Delta t=N(\lambda/2)$, where $N=n/2$. In fact, it is often the case that the fringes are only used to monitor the polishing process rather than calculate the absolute amount of unflatness.

This basic principle can be found in many optics text (see, for example, Meyer-Arendt (1984) or Moller (1983)).

SELECTED AREA POLISHING

The technique employed here for preparing a precision cross section TEM sample is based upon the procedure described originally by Benedict *et al.* (1990). To implement the above fringe observation method, the authors used a four inch diameter glass lapping plate supplied by Gatan Inc. for use with their Disc Grinder. In this way, the sample could be continuously monitored during polishing because the cover glass was sufficiently flat across the entire span of the Tripod Polisher feet. To carry out the "selected area polish," simply place the glass plate on top of the mounted sample assembly, beginning with a sample that has been lapped with at least 6 micron polish to provide a sufficiently specular surface. When the glass plate touches the micrometer feet and the sample, interference fringes from reflected room light can been seen emanating from all points of contact. It is best to look for these fringes in an orientation wherein a mirror image of the room lights can be seen reflecting from the glass.

The glass surface now represents the plane of polish. Adjustment of the Tripod Polisher micrometers adjusts the plane-of-polish which is visually monitored by watching the centers of the fringe patterns, representing those points of contact between the glass and the sample, as they move across the glass/sample interface. The idea is to position these optical fringes at the "high spots" in order that they can be removed during polishing. Additional precision can be obtained by viewing the fringes under a stereo microscope. Polishing is complete when the fringes disappear, indicating edge-to-edge surface flatness has been achieved.

During polishing of the second side, the sample is viewed under transmitted

light. The micrometers are now adjusted so that the centers of the interference fringes are positioned over the darker (thicker) regions of the sample, which are selectively removed during subsequent polishing. Using this method, the angle of a wedge-shaped (Benedict *et al.*, 1991) polish is also readily controlled.

In some instances it may help to purposely polish the sample so that it first achieves transparency at two opposite ends. This yields a conspicuous profile of fringes in the thicker center portion of the sample which can be used to eventually bring the entire section to uniform flatness safely. For silicon samples, color changes are an additional help in determining specimen thickness during the final critical steps of second side polishing.

These procedures are highlighted in the example shown in Figure 2. Light microscope images of a piece of silicon at certain stage of polishing. Figure 2 (a) shows the sample of nonuniform thickness with some scratch on its surface. By placing the glass in contact with the sample and adjusting the micrometers, the interference fringes can be seen and moved to the thicker part of the sample(b). After a few seconds polish, (c) shows the sample becoming more uniformly flat. For example the scratches visible in (a) and (b) are only removed in the thicker regions of the sample and the thinner portions are not disturbed. Note the (c) is still not flat enough, repeating of observation and polishing process is necessary until it becomes completely flat or with desired wedge angle.

With care, the results can be impressive. Figure 3 is a transmitted light image of an entire Intel® 80386 device (0.4 inches on a side) evenly thinned from the back side to total thickness of 5 microns using the procedures.

APPLICATIONS

To illustrate the application of this method for precision area selection during cross-sectional TEM sample preparation, an example isolating a single failed transistor was chosen and is presented in Figures 4 through 6. Figure 4 demonstrates the first stage of isolation, wherein a focused ion beam (FIB) was employed to outline the failed transistor so that it can be tracked during polishing process. Here it is seen in an FIB induced secondary electron image, and the failed transistor is the one in the center of the FIB-marked central box. This sample was mechanically polished along the horizontal plane containing the target transistor, as indicated by arrows, from both top and bottom, to a electron transparency. Figure 5 is an optical image of the TEM-ready sample. The FIB marks indicated by the arrows are the same FIB cuts visible in Figure 4. Because this image is taken in transmitted light, the contrast gradient of the silicon substrate indicates that the sample is wedge shaped, becoming gradually thicker towards the lower part of the micrograph. Figure 6 is low magnification TEM photograph of the failed transistor. The reference FIB marks are one transistor away on both sides. Note that a crack can be seen at the corner of the poly-Si structure labeled "poly 2." Such cracks are normally considered to be the result of thermal shock, induced by a leakage current. Where the leakage occurred is revealed in the higher magnification TEM image of Figure 7, recorded before final ion-milling to the thickness shown in Figure 6. This completes the failure diagnosis: the transistor clearly failed because of current leakage between two polysilicon layers (poly 1 and poly 2 in Fig. 7).

A useful variation of this method is that it can be used for one-sided (or "back-sided") polishing to produce precision cross-sections for SEM observation. In SEM x-ray microanalysis, backside polishing can reduce the volume of sample probed by the electron beam, increasing spatial resolution. Alternatively, an SEM can be used to determine very precisely the termination point of the first

side polishing of a TEM sample. Obviously, the technique can also be used for precision polishing of other types of samples. Specimens of 3mm X 5mm with a uniform thickness of 1-2 microns were made for backside interface profiling in SIMS by this same method.

DISCUSSION AND CONCLUSIONS

The selected area polishing technique described above offers the metallographer several distinct advantages. Because of the ability to conduct dynamic visual inspection, it is not necessary to calibrate or set to any specific value the micrometers on the Tripod Polisher. In fact, the reading of the micrometers can essentially be neglected. Even detaching and remounting the sample stub on the polisher does not slow down the process of sample preparation because the plane-of-polish can be easily re-established.

Another major advantage of this method is that more accurate depth control can be achieved. Every division of the micrometer is 10 microns while the corresponding distance between interference fringes is less than 1/4 micron. Assessing the height of the sample before and after adjusting the Tripod Polisher micrometers by focusing a depth-sensitive optical microscope is a tedious job, and becomes unnecessary with the interference fringe method. This advantage is particularly important when the original sample size is just large enough to be a 3mm TEM sample.

Unfortunately, there is a problem associated with TEM sample preparation for device failure analysis: in most instances, the thickness of the sample is significantly less than the size of a potential defect. For example, a 100nm thick TEM sample could conceivably miss a defect in an 800nm wide metal line. In the case of the transistor work presented in this paper, the current leakage could have occurred anywhere across the width of the polysilicon line shown in

Figure 7. Two possible solutions are suggested: one is to leave the work with thicker samples (say one micron) by conducting the TEM analysis in a high voltage TEM (~1MeV). The second is to gradually thin the sample with sequential ion thinning and examination in the TEM until the area of interest is just thin enough. There remains the possibility that the region of interest may inadvertently be sputtered away in this latter approach, but it represents the contemporary challenge of how to use TEM device failure analysis to improve semiconductor fabrication and processing.

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FIGURE CAPTIONS

Figure 1 Schematic illustrating the optical principles behind the use of interference fringes for precise control of thickness during selected area polishing.

Figure 2 Sequence during selected area polishing showing: (a) initial appearance of sample after contact with optical glass; (b) appearance of interference fringes after adjustment of Tripod Polisher micrometers; and (c) flattening of high points in sample following few seconds of polishing, indicated by disappearance of interference fringes.

Figure 3 Transmitted light image of complete Intel® 80386 chip polished from the backside to total thickness of 5 microns.

Figure 4 Transistor array and Focused Ion Beam (FIB) marked box to locate the site of a single failed transistor in a memory chip.

Figure 5 Light microscope image of the TEM ready sample with the FIB marks in the center. Note the gradual increase in background darkening of the image, indicating that it is wedge shaped.

Figure 6 Low magnification TEM image show failed transistor with the FIB marks.

Figure 7 Higher magnification TEM image revealing site of short circuit between poly1 and poly2 in thick sample.

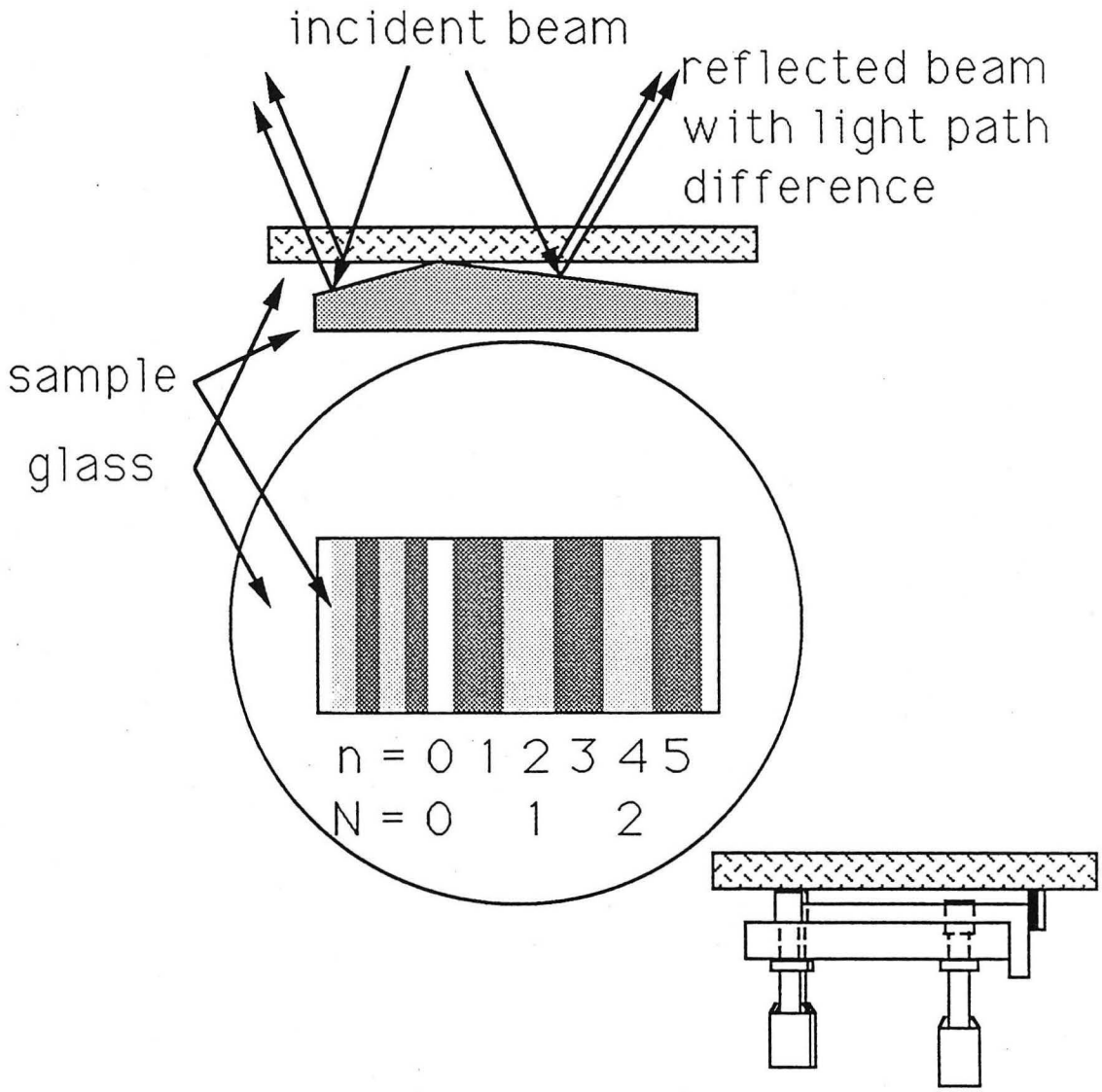

Fig.1 Optical principle of "selected area polish

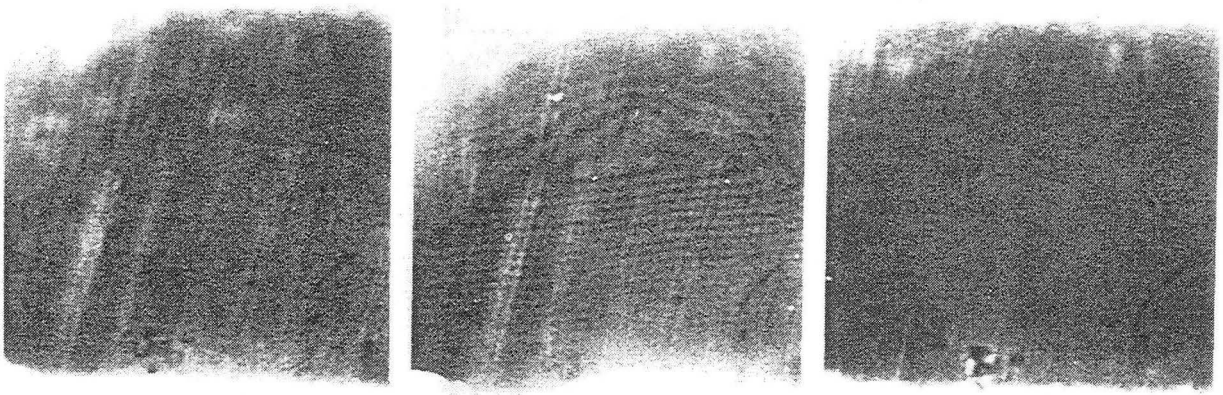

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Fig.2 The process of "selected area polish"

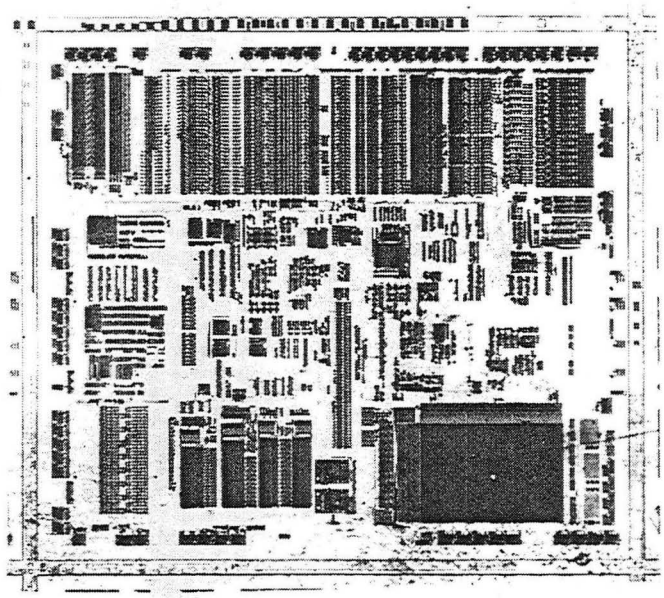

Figure 3 Transmitted light image of 80386 chip polished from the backside down to total thickness of 5 microns

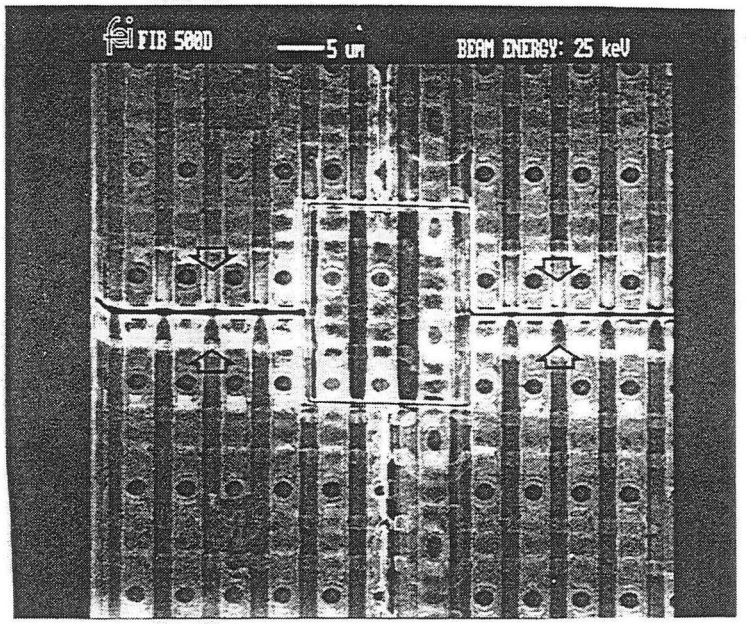

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Fig.4 FIB marked box to locate the failed transistor in a memory chip

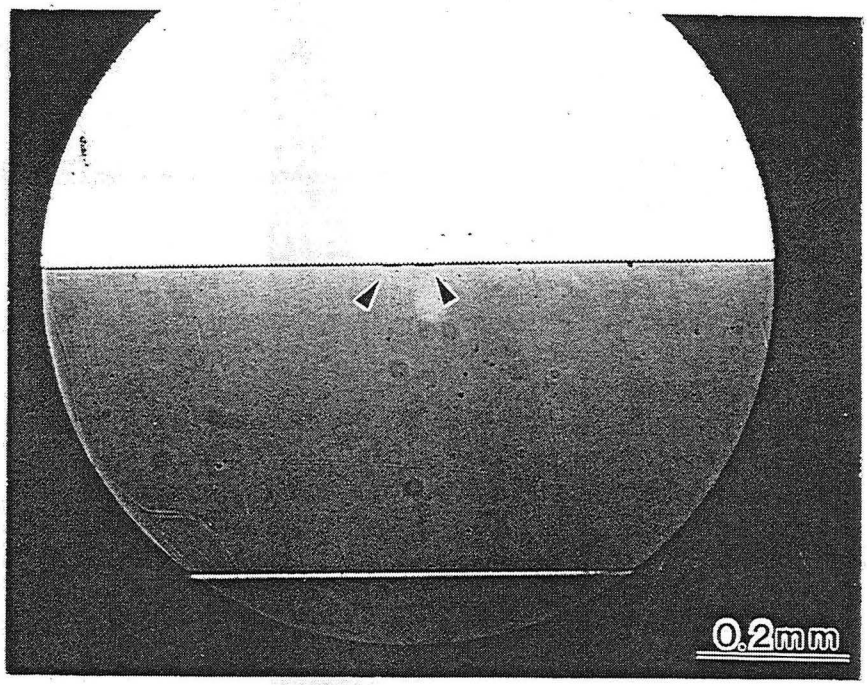

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Fig.5 Light microscope image of the TEM ready sample with the FIB marks in the center. Note the sample is "wedge shaped".

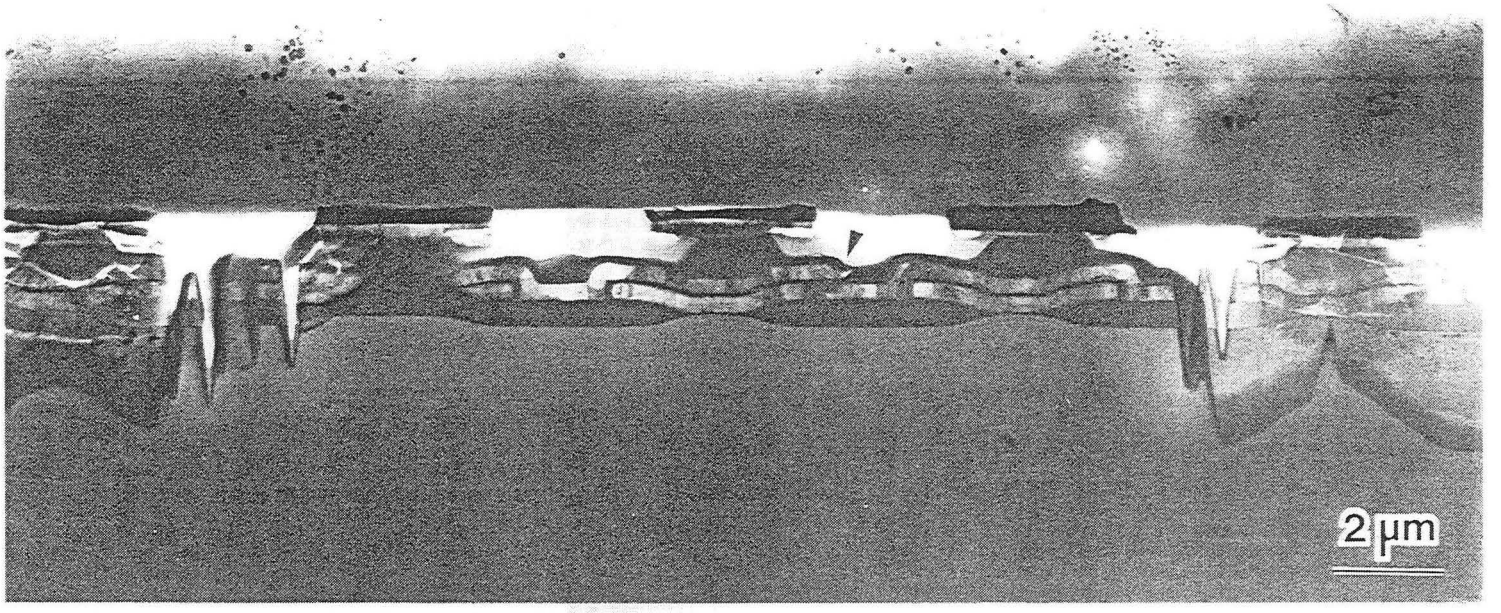

Figure 6 Low magnification TEM image show failed transistor with the FIB marks

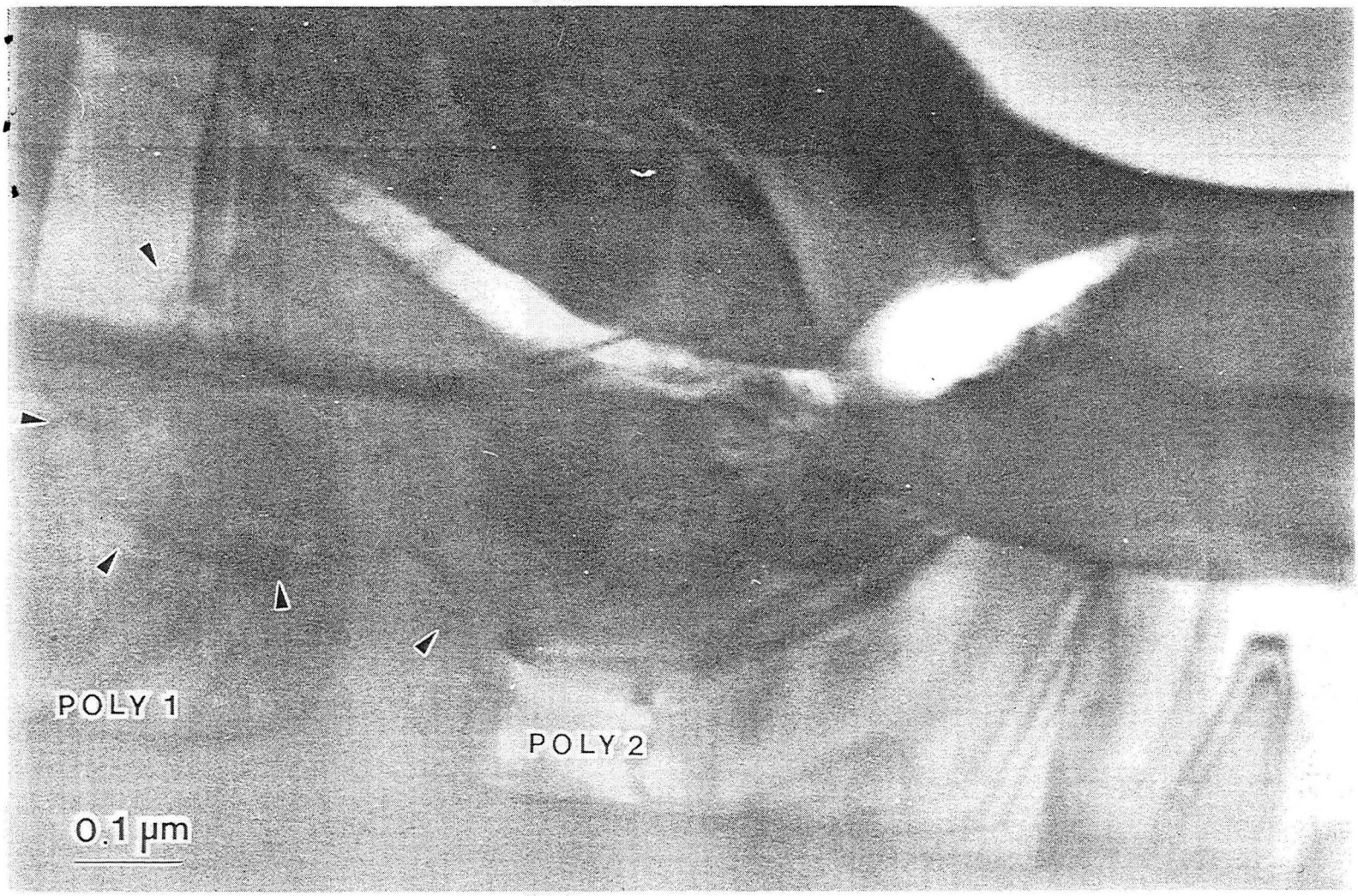

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Fig.7 Short circuit between poly1 and poly2 in the sample when it is thick, which is ion-milled off in Fig.6.

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