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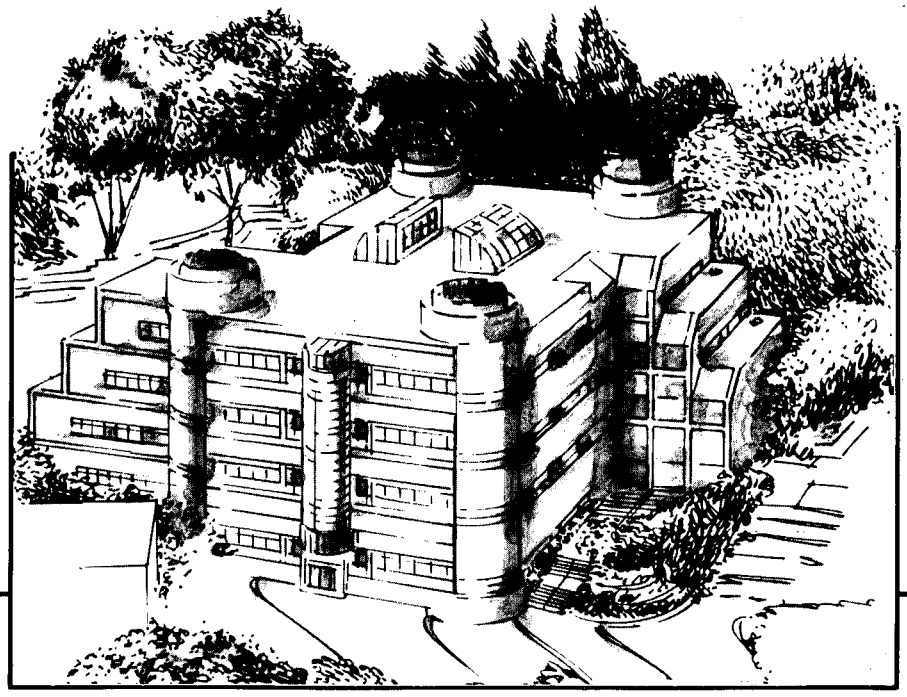

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Atomic Structure of Metal/GaAs Interfaces: The Role of Defects, Epitaxy, and Morphology

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Atomic Structure of Metal/GaAs Interfaces: The Role of Defects, Epitaxy, and Morphology

Zuzanna Liliental-Weber, Eicke R. Weber, and Nathan Newman

1.0 INTRODUCTION

One of the long-standing problems in electronic materials is the fundamental understanding of Schottky barrier formation. This problem has caused an extensive controversy in the literature for many years,[1] fueled by the fundamental interest in this question and the technological requirement of reliable and reproducible metal-semiconductor contacts as a prerequisite for the fabrication of electronic devices.

In the case of GaAs and other III-V compounds, two types of contacts are required: ohmic contacts, which connect the outside world to the active portion of the device; and rectifying contacts, which utilize the properties of the depletion region to achieve the device function, e.g., as gate contacts in field effect transistors, or for charge collection in detectors and solar cells. For some device fabrication sequences, the contacts must survive 800°C or higher temperatures during the anneals needed to activate implanted dopants.

Despite the widespread use of rectifying contacts to GaAs, two important issues remain to be resolved: the basic mechanism responsible for the observed Schottky barrier heights, and the reproducibility and stability of electrical performance during annealing and aging. An unstable interface invariably results in unpredictable contact resistance for ohmic contacts and barrier height changes and increased leakage currents for Schottky contacts. Although all these effects are known to be detrimental

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to device performance, the changes in barrier height that cause threshold voltage shifts in MESFET devices have been particularly troublesome.

Most experimental data agree that the barrier heights for metals deposited by evaporation or sputtering on GaAs fall within a few tenths of an eV in the midgap region, indicating a strong Fermi level pinning mechanism at the metal/GaAs interfaces. The measurements of barrier heights for many metals deposited in situ on ultrahigh-vacuum-cleaved GaAs (110), as determined, e.g., by Newman,[2]-[4] using I-V and C-V characteristics, seem to be very consistent. They show the same ideality factor n = 1.05 independent of the reactivity of the particular metal. The lowest barrier height found on n-GaAs was for Cr (Φ_b = 0.67 eV), and the highest was for Au (Φ_b = 0.92 eV). Generally, the sum of the barrier heights for the same metal deposited on n- and p-type substrates comes close to the GaAs bandgap, indicating that both n-type and p-type diodes have a common pinning position within the GaAs bandgap. Similar results have also been reported by McLean[5] and Waldrop.[6] To explain these results, several models have been proposed.[7]-[16] These models can be divided into two categories: those that include only the inherent properties of ideal metal/GaAs interfaces (frequently referred to as metal-induced gap states models[8]), and models that include the presence of lattice defects near the heterointerface. Currently popular defect models[1] propose either that native deep-level defects whose energy levels dominate Fermi level pinning are formed upon metal deposition,[11]-[16] e.g., due to the energy released during metal solidification, or that the effective work function differences between GaAs and microscopic near-interfacial anion-rich metallic inclusions determine the Schottky barrier height (the *Effective Work Function* model[9]-[10]).

In reality, most metal/semiconductor interfaces formed at room temperature are found to be non-ideal. In general, the near-surface region of the semiconductor is disrupted by the deposition of the metal. Annealing of metal films on compound semiconductor substrates at elevated temperatures can result in the dissolution of the compound semiconductor and the subsequent precipitation or regrowth of heavily doped or alloyed epitaxial layers. In each case (metal deposition or annealing), the metal/semiconductor interface is most affected by formation of defects such as protrusions, planar defects (stacking faults), line defects (dislocations), and point defects.

This chapter we will discuss the current knowledge of the structure of metal/GaAs interfaces and the influence of this parameter on technologi-

cally relevant issues such as the chemical stability and electrical behavior of the contacts. The metal/III-V contacts are considered to be model systems because the intrinsic surface states in these systems do not fall within the bandgap and are therefore not responsible for the pinning the Fermi-level in Schottky contacts. While this review covers the work on GaAs, other metal/III-V systems are found to have similar trends in properties to that on GaAs, although some quantitative differences are found. For example, Schottky barriers on InP are found to fall in a similarly narrow range of Fermi-level pinning position, as is found for GaAs, but with a position significantly higher in the bandgap. Similar reactions are found between a chosen metal and the cation and anion, although InP is in general more reactive than GaAs due its smaller heat of formation. In addition, the role of non-stoichiometric defects is believed to play an important role for all systems studied to date. Because of the similar nature of many of the metal/III-V systems, this review should be useful to investigators studying or using GaAs, as well as other semiconductor contacts.

We will describe possible defects formed at the metal/GaAs interface, giving several examples of non-reactive and reactive metals used for Schottky or ohmic contacts. The influence of particular defects on the Schottky barrier height and electronic properties of those contacts is also discussed in this chapter. The chapter is organized in the following way: first, detailed characteristics of the structure of several diodes are described, followed by stoichiometry and stability studies. Finally, we will show that the presence of antisite defects can be related to stoichiometry changes near the interface. These near-interfacial antisite defects are found to play an important role in Fermi-level pinning of the Schottky barriers.[14][17]

This review is mostly based on our own work in cooperation with the Stanford group. Structural studies were done using transmission electron microscopy, including high-resolution and analytical electron microscopy for studying interface abruptness, orientation relationship, new phases, and stoichiometry changes in the interfacial regions of the contacts. The Schottky barrier heights were measured using I-V and C-V characteristics. The aging of the diodes was obtained by applying current and voltage stress. The same diodes for which electrical parameters were measured were used for structural studies; therefore, it was possible to directly correlate the structural differences with the electrical properties.

2.0 INTERFACE FORMATION AND RESULTING MICROSTRUCTURE

Metal contacts on semiconductor surfaces generally show a flat interface after deposition. However, one technological requirement for a good metal contact is the preservation of interface flatness upon subsequent annealing during device processing, as otherwise the degradation of interface flatness can result in inhomogeneous electrical properties, leakage currents, and generally unpredictable electrical performance. As device dimensions decrease, deviations from flatness are particularly troublesome because protrusions can extend through the active portion of the device. Interface stability can be achieved either by uniform reaction at the interface or complete absence of reaction.

In this paragraph we will discuss several examples of metal contacts to GaAs in order to understand the fundamental mechanisms responsible for the formation of the Schottky barrier and the factors that may result in interface degradation. An effort was made to avoid the influence of impurities at the interface in order to eliminate any unnecessary variables that could influence the contact properties.[2] Almost all of the Schottky contacts in this study were prepared on GaAs (110) cleavage surfaces.[2][18]-[19] Cleavage in ultrahigh vacum (UHV) with in-situ metal deposition virtually guarantees the complete absence of impurities. (Henceforth, structures fabricated in this way will be referred to as *atomically clean* interfaces.) Comparison of such contacts with those deposited after cleavage in air allow for the direct investigation of the effects of interface contamination. (We will refer to these structures as *contaminated* interfaces.) It will be shown that the orientation relationship between the metal grains and the semiconductor found after annealing is influenced by impurities present at the semiconductor surface prior to metal deposition, as well as by growth conditions such as deposition rate and substrate temperature. A specific orientation relationship between the metal and semiconductor is found for the atomically clean interfaces; this orientation relationship can be vastly different from metals deposited on contaminated semiconductor surfaces. In some cases, we also studied the same metal (Au,[18]-[19] Au-Ni-Ge,[20] or Al-Ni-Ge[21]) deposited on chemically (industrially) prepared GaAs surfaces in order to observe similarities and differences in interface reactions.

Several classes of metals will be described. We will summarize this section starting with the least reactive overlayers and ending with the most reactive overlayers.

The first class of metal described is represented by Ag.[3][4][22]-[24] This

metal does not form compounds with GaAs even at elevated temperatures. Only for in-situ Ag depositions on UHV-cleaved GaAs does the interface and the Schottky barrier height remain stable and uniform at elevated temperature.[3] When contamination is present at the interface, large changes in the Schottky barrier height are found, and extended protrusions are formed upon annealing.[22] As can be seen, the presence of impurities at the interface influences the electrical and chemical stability of these contacts. TiN[25] and ZrN[26] are also found to be thermally stable contacts. Because these overlayers can react with and/or dissolve native GaAs oxides, contacts formed on air-exposed or chemically prepared surfaces are expected to be less susceptible to the effects of contamination. Contacts fabricated on chemically prepared surfaces are found to have flat interfaces even up to anneals at 500°C for TiN and 700°C for ZrN, with a stable Schottky barrier height to these temperatures. At 700°C and above, specific "pockets" are formed at the interface, suggesting out-diffusion of some substrate elements leading to large leakage currents in the Schottky contacts.

For slightly more reactive interfaces, such as Au on GaAs,[3][18][19][22] similar trends in the annealing-induced changes in the electrical properties are found for both atomically clean interfaces and contaminated interfaces. In both cases, if the effects of peripheral leakage currents are removed,[3] the contacts are found to have near-ideal, strongly rectifying behavior after annealing, with a barrier height reduction of ~0.15 eV.[3][22] However, morphologically large differences are found. After anneals in N_2 at 405°C, the atomically-clean interface is found to be flat. High-resolution electron microscopy did not detect a new crystallographic phase at the interface. However, energy dispersive x-ray (EDX) spectroscopy[18] and surface analysis by laser ionization (SALI)[30][31] detected a few percent (not more than 5%) of Ga in the Au layer and accumulation of As close to the interface. This indicates uniform out-diffusion of Ga from the GaAs interface, leaving As in the semiconductor beneath the metal. However, for the contaminated interface, the formation of protrusions resulted due to the selective reaction at voids and pinholes in the contamination layer.

While Au is known to react preferentially with Ga, Al is known to react with As. Al/GaAs systems, upon prolonged annealing times or extremely high annealing temperatures, form ternary (AlGa)As compounds. However, short annealing times (10 min) at lower temperatures (e.g., 400°C) lead only to reactions within a few monolayers of the interface, reactions that are not always possible to detect by transmission electron microscopy.

Nevertheless, under these annealing conditions a substantial increase in the barrier height is still found.[3] Under most circumstances, the Al/GaAs interfaces are found to be flat and are not greatly influenced by the presence of impurities.[19][24][32] Al is expected to reduce any native GaAs oxide and form oxides of Al (e.g., Al_2O_3).

Al, Ag, and Au have a cubic structure with similar lattice parameters (0.405 nm, 0.409 nm, and 0.408 nm, respectively). All three metals are found to form the same specific orientation relationship between the metal and GaAs in annealed contacts fabricated with atomically clean interfaces. The orientation relationships are found to be greatly different when the metals are deposited on air-exposed substrates.[19] In these cases the orientation relationship follows the expected epitaxy with γ-Ga_2O_3, which immediately forms upon air exposure.[33]

For ohmic contacts, this protrusion formation can be prevented even when impurities are present if Al is used with Ge and Ni, instead of the conventional use of Au. It will be shown in the case of ohmic contacts (Al-Ni-Ge) that even when the flatness of the interface is reached, the lack of appropriate dopant (Ge) at the interface does not lead to a low resistivity ohmic contact.[22] Only specific layer deposition sequences that allow diffusion of selected dopant elements to the interface can fulfill the ohmic device requirements: interface flatness and doping of the semiconductor beneath the metal.

Cr is a metal that is known to react with both Ga and As, as well as with the native GaAs oxides. Differences in the interface properties due to the presence of impurities are observed for Cr.[22][34][35] For atomically clean interfaces, the Schottky barrier height is found to be stable upon annealing.[22] For contaminated interfaces, the Schottky barrier height is found to increase substantially upon annealing.[22] For the atomically clean and air-exposed contact, the interface remains flat up to anneals at 370°C, with no new large-scale reaction products formed. Annealing at higher temperatures leads to substantial reactions at the interface, and the resulting diodes contain large amounts of leakage currents.

Very reactive metals, such as Ti[36]-[38] and Pd,[39]-[41] comprise the next class of metal/GaAs interfaces. These metals are known to react at room temperature forming ternary compounds. Flat interfaces are formed with Ti, and undulating interfaces are formed with Pd case. New reaction products are formed upon annealing at elevated temperatures. Annealing also leads to substantial changes in barrier heights for both the air-exposed and clean interfaces.

2.1 Ag/GaAs Morphology [4][23]-[24]

Ag is an example of a metal that is nonreactive with GaAs. Both thermodynamic bulk data and data from surface science studies for submonolayer to several-monolayer coverages of metal show no evidence for Ag-GaAs reaction products. Upon deposition, Ag forms grains with twins, but the interface is flat for both the samples deposited in-situ in UHV on cleaved (110) GaAs surfaces and the samples deposited on air-exposed cleaved (110) GaAs. The grain size was observed to be larger and less defective for atomically clean interfaces. This is shown in Figs. 1 a, b. The oxide layer was easily detected for the contaminated interfaces, while in the atomically clean interfaces, the Ag was in intimate contact with the substrate (Figs. 2 a, b).

Figure 1. Cross-section micrographs of Ag/GaAs interfaces. (*a*) Ag deposited in-situ on UHV-cleaved (110)GaAs. Note the very large Ag grain size; (*b*) Ag deposited on air-exposed cleaved (110)GaAs, showing a high density of twins.

Figure 2. High resolution images of Ag samples deposited on (*a*) UHV-cleaved GaAs surface and on (*b*) air exposed surface. Note thick layer of oxide present at the contaminated interface.

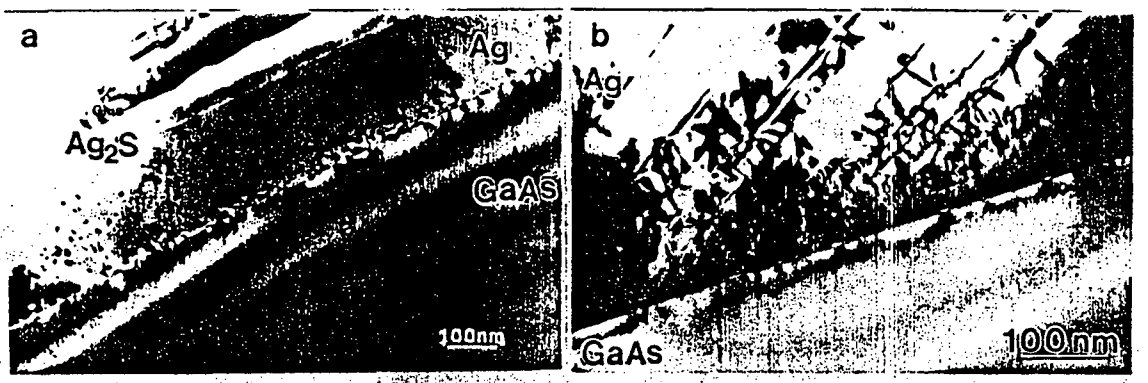

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Fig.1

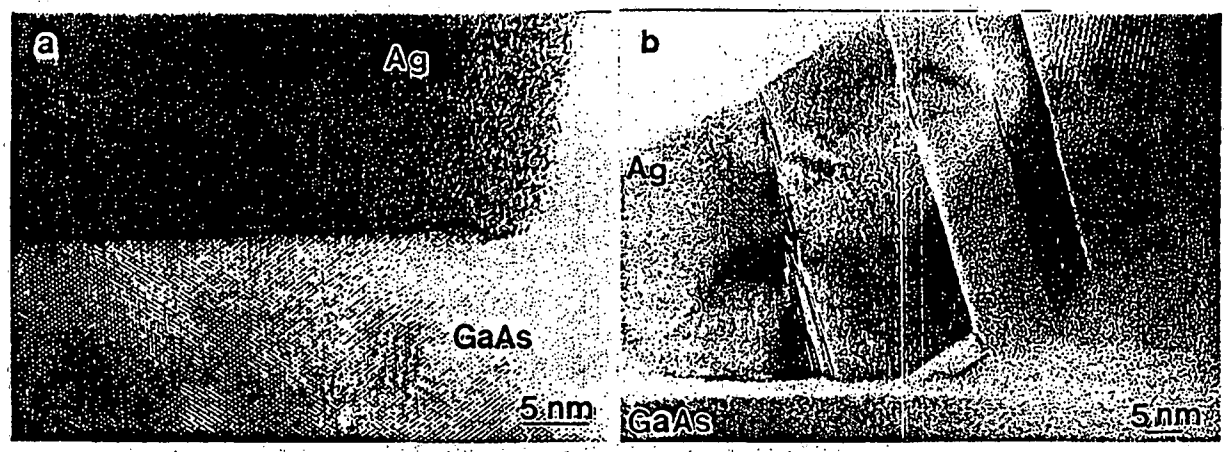

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Fig.2

contaminated interfaces. The as-deposited Au layer was found to be polycrystalline, with grain diameters in the 10 - 50 nm range. The largest grain size was found in UHV-deposited Au samples on cleaved in situ (110) GaAs surfaces. Such unannealed Au layers observed in cross section show atomically flat interfaces with GaAs. Some of these grains, particularly in UHV-cleaved samples, were epitaxial, with their (211) or (011) orientation parallel to the (011)GaAs substrate orientation; but generally the grains were randomly oriented, resulting in diffraction patterns with textured rings.

Significant differences between these air-exposed samples and UHV-deposited samples occur after annealing in N_2 at 405°C for 10 min (Figs. 4, 5). For the UHV-cleaved samples, the interface remains flat and abrupt despite the annealing process (Fig. 4a). The entire Au layer is almost monocrystalline, with the smallest grain size ~500 nm. Both a specific semiconductor surface reconstruction beneath the metal and the formation of misfit dislocations were found at this interface (Fig. 5), similar to those observed for the annealed Ag layers.

Figure 4. The Au/GaAs interface abruptness after annealing for 10 min at 405°C; (*a*) Au deposited in situ on a UHV cleaved GaAs surface; (*b*) Au deposited on the GaAs surface cleaved in air. Note protrusion formation at the contaminated interface.

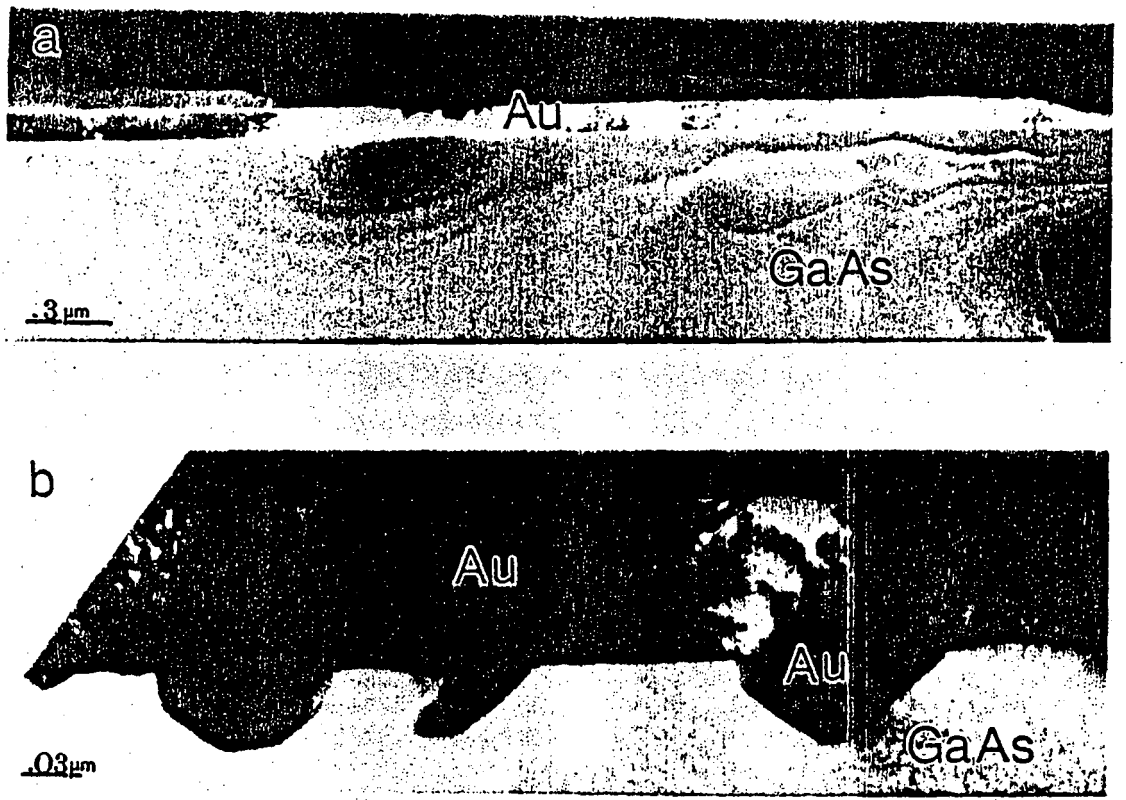

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Fig. 4

Figure 5. High resolution micrograph of the Au/GaAs (011) interface annealed at 405°C for 10 min in N_2 atmosphere. Note the lattice distortion in the interfacial area and the twisting of all Au planes toward the GaAs planes. A 10° angle was measured between the $(11\bar{1})$Au (shown on the micrograph with weak contrast) and $(11\bar{1})$GaAs planes. Note that six $(\bar{1}1\bar{1})$Au planes coincide with five $(200)_{GaAs}$ planes.

The same annealing treatment for Au samples deposited on GaAs cleaved in air resulted in the formation of voids and metallic protrusions at the interface (Fig. 4b). Many small grains, highly twinned and dislocated and with irregular shapes, were observed in a plan view of these annealed contaminated interfaces. The oxide layer was still detected at the interface even after annealing. The Au layer above the oxide layer has many defects, and its grain size is much smaller than found for annealed atomically clean Au interfaces. The orientation relationship for grains at the contaminated interface was (011)Au || (011)GaAs. Au diffusion through pinholes in the oxide layer lead to protrusion formation at the interface. These protrusions are single grains of Au. For the contaminated interfaces, the volume of the remaining overlayer plus that of the protrusions is found to be equal to the volume of the Au overlayer in the as-deposited samples.

In cross section, two different shapes of protrusions extending into the GaAs were found (Fig. 4b): (*i*) triangular protrusions, whose sides are delineated by GaAs {111} planes, and (*ii*) multifaceted protrusions delineated by GaAs {111}, {110}, and {100} planes. Similar protrusions were observed in annealed Au/GaAs samples formed on chemically prepared GaAs(100) surfaces (Fig. 6a). The Au layer was separated from the GaAs substrate by a thin oxide band (Fig. 6b). The presence of oxygen at the interface was confirmed by energy-dispersive x-ray spectroscopy.

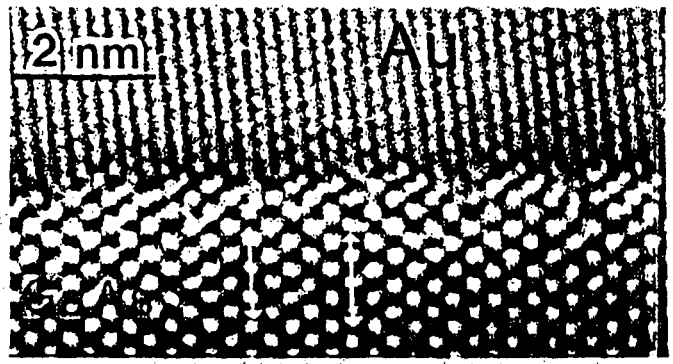

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Fig.5

Figure 6. (*a*) Au deposited on a chemically cleaned (100)GaAs surface after annealing; note the Au island beneath the oxide layer *(white band marked by arrow).* *(b)* High resolution image of the same interface showing layer of oxide and the lattice image of Au protrusion formed below the oxide layer.

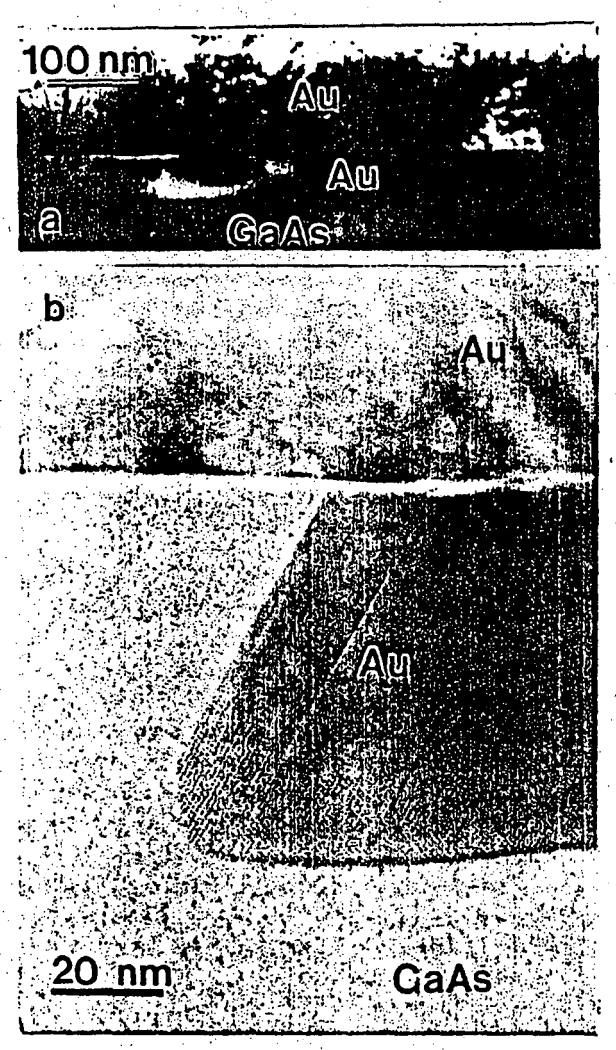

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Fig. 6

The formation of protrusions at Au/GaAs and Au-based ohmic contacts on GaAs interfaces has been observed by several independent researchers, and it was concluded that elevated temperatures are a sufficient condition for their formation. Our own study[18] shows that the morphology of the interface is strongly influenced by the surface preparation prior to Au deposition. Impurities at the interface can promote different reactions at the interface, causing non-uniform out-diffusion of substrate elements and subsequent protrusion formation at the interface. This result demonstrates that the formation of protrusions is not the result of annealing at elevated temperatures alone but is clearly affected by the semiconductor surface preparation prior to metal deposition.

Generally, if a reactive elemental metal on GaAs undergoes prolonged annealing, different phases can be formed at the interface. For Au, according to the phase diagram, Au + GaAs reactions should not take place if annealing is performed in a closed system.[42] New phases were not found after annealing atomically clean interfaces for 10 min in N_2 at 400°C. Ga was detected by x-ray dispersive spectroscopy and SALI in the Au grains, with a Ga concentration smaller than 5%. This concentration is not sufficient to form of a new crystallographic phase, although it does indicate the formation of a weak alloy with Ga and the subsequent release of As near the interface. In an open system, a Au-Ga phase should be formed, leaving excess As behind. The formation of the $AuGa_2$ phase was indeed observed when annealing was performed in vacuum for 10 min in N_2 at 400°C.[19] The resulting system is found to follow the expected epitaxy of the near perfect lattice match between GaAs and $AuGa_2$ and between $AuGa_2$ and Au.

In order to avoid any semiconductor surface disruption at the interface during metal solidification a novel technique has been developed that makes it possible to bring preformed metal clusters into contact with clean semiconductor surfaces.[43]-[45] Protective layers of ~3 nm Xe were first condensed on GaAs (110) cleaved in UHV at 60 K. A metal was then deposited by evaporation onto the solid xenon layer. As a result of this deposition, metal clusters formed in and on the xenon layer. The clusters were buffered from the semiconductor surface. The Xe buffer layers were sublimed upon warming to room temperature so that the metal clusters were brought into contact with the undisrupted GaAs surface (Fig. 7). In this way, atom deposition, cluster nucleation, and growth occurred in the overlayer before any direct substrate contact, eliminating complications from the release of energy by metal solidification. Au clusters deposited in this way are found to have an abrupt unreacted interface. High-resolution transmis-

sion electron microscopy and analytical electron microscopy show direct evidence of a defect-free interface produced by in situ cluster deposition. In contrast to interfaces produced by atom-by-atom deposition, no specific interface reconstruction or orientation relationship was observed near the interface.

Figure 7. (*a*) Plan-view micrograph of Au clusters deposited on the UHV-cleaved (110)GaAs surface; (*b*) cross-section of the interface between Au clusters and the GaAs substrate.

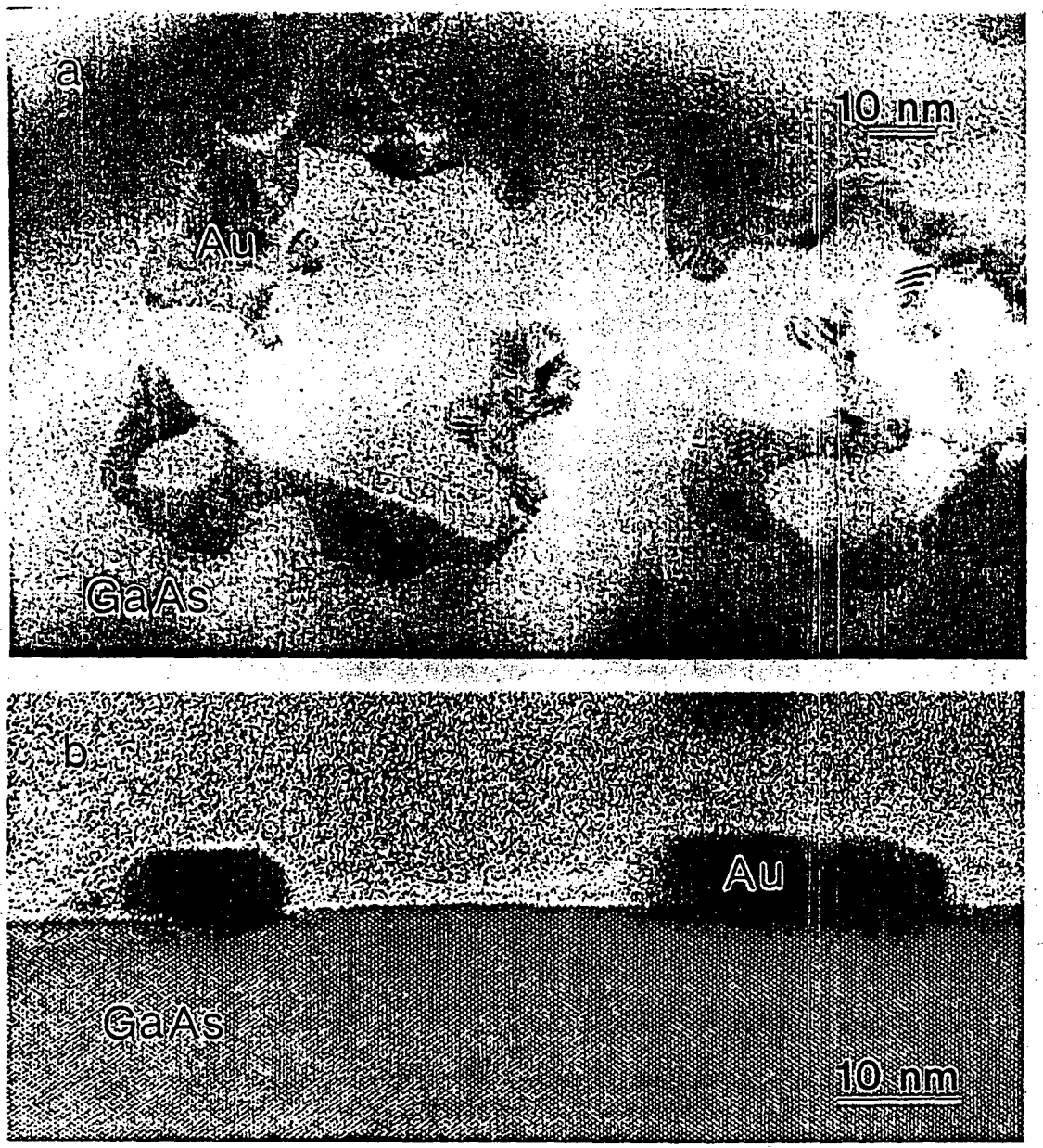

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Fig. 7

2.3 Al/GaAs Morphology[24][32]

For Al grown on UHV cleaved (110) GaAs surfaces, a typical grain size of 100 - 300 nm was observed (Fig. 8a). The interface with GaAs remains flat and Al(111) planes form a 10° angle with (111)GaAs planes (Fig. 8b). This angle remains constant even for grains with different orientations. When Al react with GaAs, it is known to preferentially form Al-As bonds and release free Ga. Upon annealing at 375°C in N_2 for 10 min, the interface remained flat and the grain size did not increase. In some areas a very thin layer of AlGaAs was formed. The formation of AlGaAs did not occur uniformly. There were large areas where this phase was not detected.

Figure 8. TEM micrograph of cross sections of Al/GaAs interfaces (*a*) from the sample prepared on UHV-cleaved substrate; (*b*) high resolution image of the same sample annealed at 405°C for 10 min in N_2; (*c*) from the Al sample prepared on air-exposed GaAs; high resolution image of the air-exposed sample annealed under the same conditions as in *(b)*. Note amorphous layer at the interface.

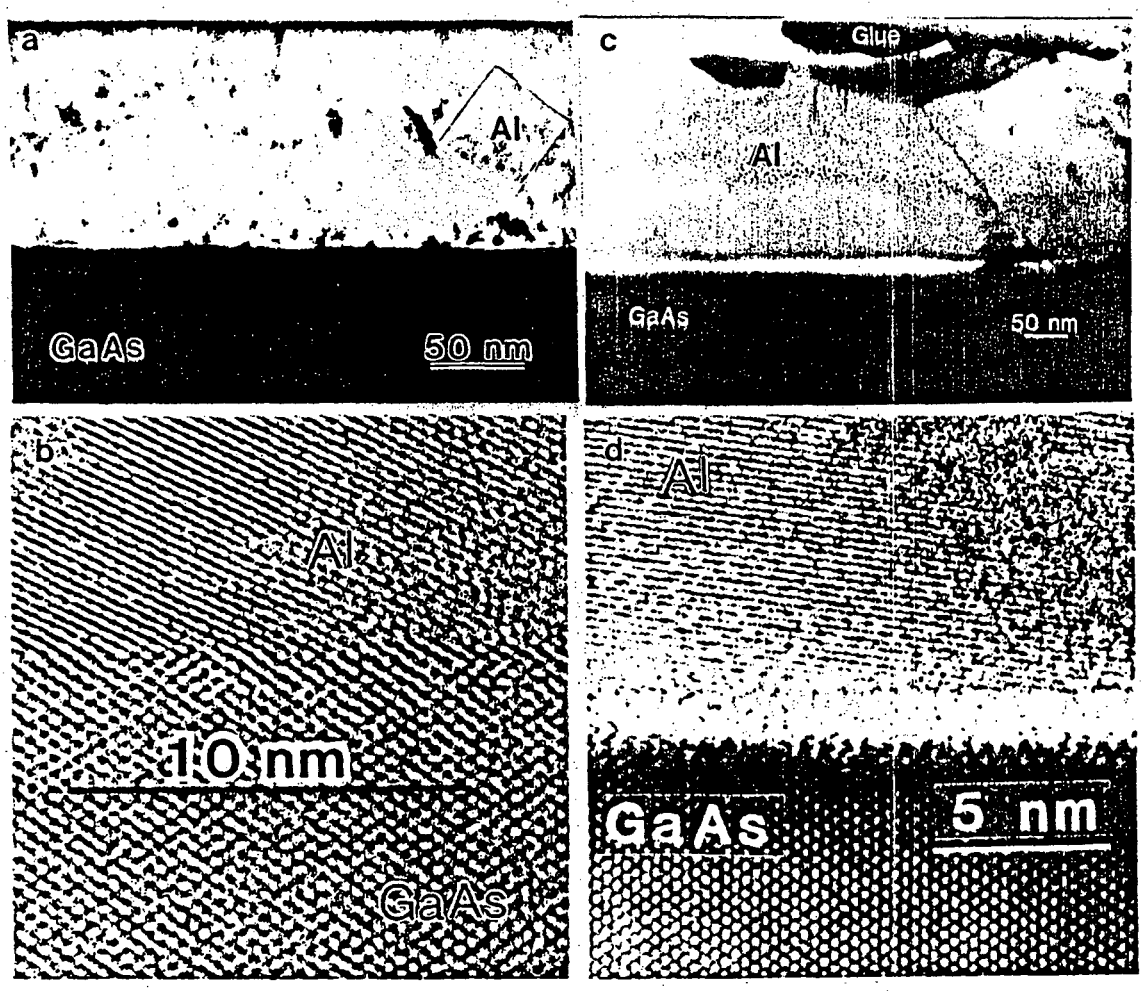

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Fig. 8

For the samples cleaved in air, the interface remained flat before and after annealing, but a significant smaller Al grain size was observed in these samples, compared to samples deposited in UHV (Fig. 8c). Only in some areas of the annealed air-exposed samples was an amorphous oxide layer detected at the interface (Fig. 8d). Above these oxide layers, the orientation of the Al was different from that found in the areas where the oxide was not detected. For Al metallization, in contrast to the other metals (Au and Ag), protrusions at the interface were not observed, even for annealed air-exposed samples. This probably can be explained by the possibility of thin oxide dispersion by Al or formation of an AlGaAs phase in intimate contact with GaAs and no As out-diffusion from the system. Void formation was not observed in as-deposited samples or annealed samples.

2.4. Ag, Au, and Al/GaAs Epitaxial Relationships[19]

As mentioned before, the metal/GaAs orientation relationship can be influenced by the impurities present at the substrate surface. The influence of these impurities is most visible in annealed samples. Upon deposition, the Au layer was found to be polycrystalline, independent of the surface preparation of GaAs. Large differences between these samples were observed after annealing. For atomically clean Au interfaces which annealed for 10 min at 405°C in a N_2 atmosphere, most of the grains were elongated along the [011]GaAs. Their orientation relationship towards the substrate was (522)Au parallel to (011)GaAs. A 10° angle was measured between the (111)Au and (111)GaAs planes. Near perfect coincidence was observed at each fifth {200}GaAs plane and each sixth {111}Au plane (Fig. 5). The existence of this orientation relationship for Au deposited in situ on UHV-cleaved GaAs was confirmed by scanning tunneling microscopy.[46] A similar orientation relationship and correlation between the {111} planes of the metal and the substrate was observed for Ag and Al.[19]

Two completely different types of orientation relationships for large grains were observed for the annealed (110) air-exposed samples and for the (100) chemically prepared samples, after subsequent annealing in the same conditions as the UHV-prepared samples: (011)Au || (011)GaAs (type I) and $(\bar{4}11)$Au || (011)GaAs (type II). The type II orientation relationship is related to the type I relationship by twinning along the (111) planes. This twinning provides a better lattice match to the substrate and releases the existing stress.

The type I orientation relationship was observed for all diodes deposited on air-exposed surfaces [Au and Ag on GaAs (110) and Au on GaAs

(100)] after annealing. This type of orientation relation was explained for Au by Yoshiie and Bauer[47] as the epitaxial relationship to the newly formed Au-Ga phase, e.g., $(0\bar{1}1)$GaAs || $(1\bar{1}0)$AuGa || $(01\bar{1})$Au with $[01\bar{1}]$GaAs || [001]AuGa || [011]Au. However, the formation of a Au-Ga phase is not necessary to achieve this orientation relationship. This orientation relationship exists in annealed Au even when a Au-Ga phase is not formed and exists for other metals, such as Ag, as well. The mechanism for this epitaxy is obviously more general than for just the case when $AuGa_2$ is formed at the interface.

A possible explanation for the type I orientation relationship is that γ-Ga_2O_3 grows epitaxially on GaAs in a type I orientation relationship: (011) γ-Ga_2O_3 || (011)GaAs with [100] γ-Ga_2O_3 || [100]GaAs.[19][33] This oxide provides an excellent lattice match to Au: $d_{400}(\gamma\text{-}Ga_2O_3) = 0.205$ nm, as compared to d_{200} (Au) = 0.203 nm (and very similar spacings for Ag), and d_{044} (γ-Ga_2O_3) = 0.145 nm, compared to d_{022} (Au) = 0.149 nm. This observation suggests that GaAs surfaces exposed to air form epitaxial γ-Ga_2O_3, and the deposited metal relates epitaxially to the oxide already existing on the surface. The γ-Ga_2O_3 oxide is not a continuous layer. In pinholes, twinning gives a better match at the interface, which can explain the observed type II orientation relationship.

The clear difference in the orientation relationship between air-exposed and UHV-prepared samples of the same metal (e.g., Au) provides an additional tool to distinguish between metal layers deposited on clean and on contaminated semiconductor surfaces. Surface contamination before metal deposition influences not only the orientation relationship but also the stability of metal contacts, as discussed in detail in Sec. 3 of this contribution.

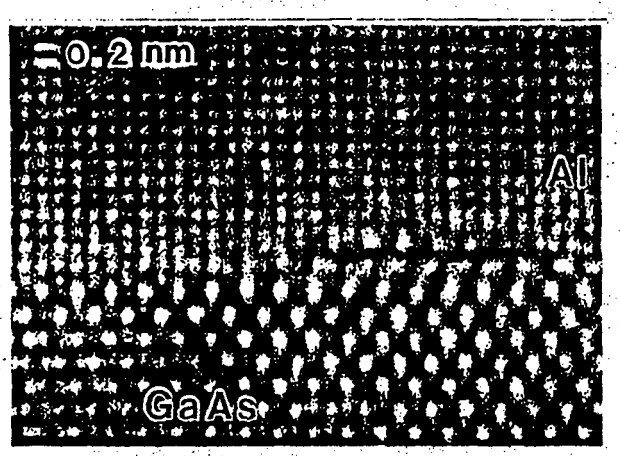
For Al deposited at low substrate temperatures (<0°C) in situ in an MBE chamber on in situ grown GaAs, the Al layer is epitaxially regrown on the (001)GaAs surface, with Al(001) || GaAs(001), Al[100] || GaAs[110], and [010]Al || $[1\bar{1}0]$ GaAs. This is the most stable and expected Al arrangement on (001)GaAs, showing fourfold symmetry because of a good lattice match between the $GaAs_{220}$ (0.1991 nm) and Al_{200} (0.2034 nm) on two perpendicular axes.[32][48]-[49]

When the substrate temperature was raised to 25°C during metal deposition, some of the grains showed the (110) orientation, with [002]Al || $[2\bar{2}0]$ GaAs. The lattice image showed monoatomic steps (2 - 4 Å high) along the interface (Fig. 9). No exchange reaction was discovered by dark-field electron microscopy imaging. For the As-stabilized surface, c(2x8), at a substrate temperature of 150°C, triangular faceted islands with (110)Al

(three-dimensional growth) orientation were observed along the interface with GaAs, with [002]Al || $[\bar{2}\bar{2}0]$GaAs (Fig. 10). Those islands were imbedded in strips of Al parallel to the interface where the $[\bar{2}\bar{2}0]$Al axis was inclined to the same axis in the triangular islands. A layer of AlGaAs was found at the GaAs interface. This AlGaAs layer was significantly larger in thickness for the samples fabricated with a substrate temperature of 400°C during Al deposition. In most cases, the Al layer adjacent to AlGaAs had a (110) orientation parallel to the (001)GaAs. Formation of triangular islands was characteristic of higher growth temperatures.

Figure 9. High resolution image of the Al/GaAs (100) interface grown in an MBE chamber with 25°C substrate temperature.

Figure 10. Al islands formed on the interface with GaAs for deposition in MBE chamber at the substrate temperature of 150°C. The thin layer of GaAlAs was observed by dark field imaging in these samples.



100%

70%

Fig. 10

2.5 AuNiGe/GaAs Morphology[20]

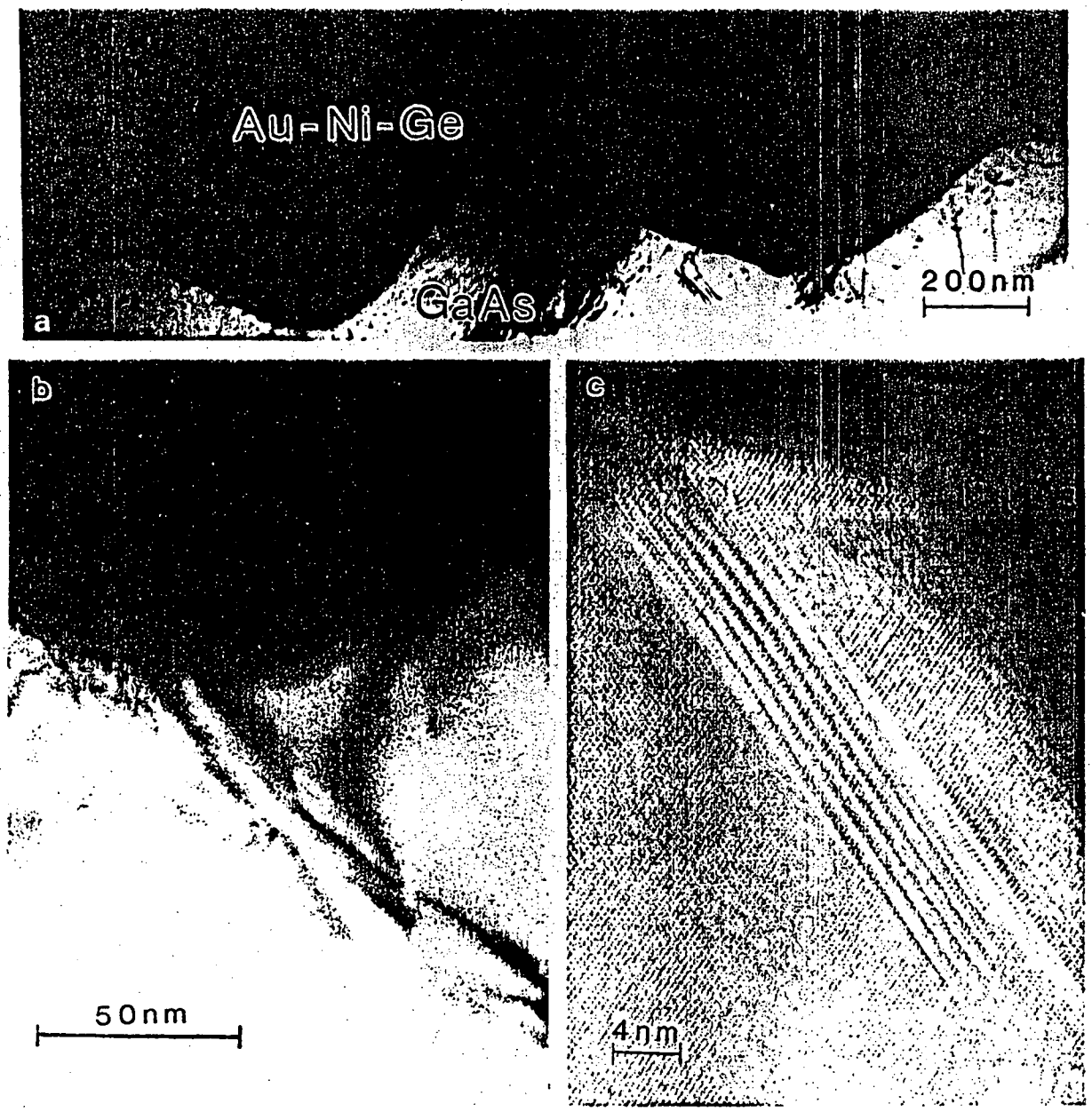
Protrusion formation at the interface is detrimental to both ohmic and Schottky contacts. For Au-Ni-Ge contacts, formation of protrusions of different composition was observed at the interface. For ohmic contacts, these protrusions determine the electrical properties of the contact. Braslau[50] proposed that Ge accumulation surrounds such protrusions and forms an n^+ layer beneath the metal. It has been predicted that the tunneling current flow is controlled by the field enhancement at these penetrating points. The resulting current was predicted to be dominated by the spreading resistance, which is known to be proportional to the doping concentration: Such protrusions contain Au-Ga grains of varying compositions that can produce strain at the interface (Fig. 11a). This strain leads to formation of various defects near the interface, such as dislocations and stacking faults (Fig. 11b). All dislocations were found on the apexes of the triangular protrusions. It appears that short circuit "pipe" diffusion of the alloying elements takes place along the dislocation lines. The metal diffusion coefficient is about two orders of magnitude higher than for the fastest bulk impurity diffusion coefficients reported for GaAs.[20][51] Stacking faults were found in the corners between the triangular protrusions and the flat interface (Fig. 11c). Formation of such defects can lead to device degradation, especially when these defects propagate through the active area of the devices.

2.6 AlNiGe/GaAs Morphology[21]

When Al was substituted for Au in ohmic contacts (e.g., Al-Ni-Ge contacts), annealing of these contacts did not introduce any protrusions at the interface. However, the metal layer sequence during deposition was found to be a critical factor in determining the electrical contact properties. This property was associated with the dispersal of an oxide layer on the semiconductor surface after chemical cleaning. Deposition of Ni as the first layer (Ni/Al-Ge/Ni/Al) instead of Ge (Ge/Ni/Al) did not disperse the impurity layer present at the semiconductor surface even after annealing (Fig. 12a), and layers with such metal layer sequences did not produce ohmic contacts. In this case a Ge layer is formed that is separated from GaAs by an amorphous impurity layer (Fig. 12 b, c). Since low contact resistance was ascribed to Ge dopants in GaAs forming an n^+ layer beneath the metal, it is possible that an amorphous impurity layer at the interface did not allow Ge to penetrate. When the Ge layer is deposited directly on the semiconductor surface, then annealing leads to the formation of two phases: Ge_3Ni

(Fig. 12c) and Al_3Ni. The interface remained flat (Fig. 13b) despite annealing and formation of different phases. In addition Ge was found by SIMS and EDX in the semiconductor beneath the newly formed phases. The contact resistance after annealing at 500°C for 1 min was 1.4×10^{-6} A cm^{-2} and it was expected that a Ge doped n^+ layer was formed in the semiconductor and was responsible for low contact resistance.

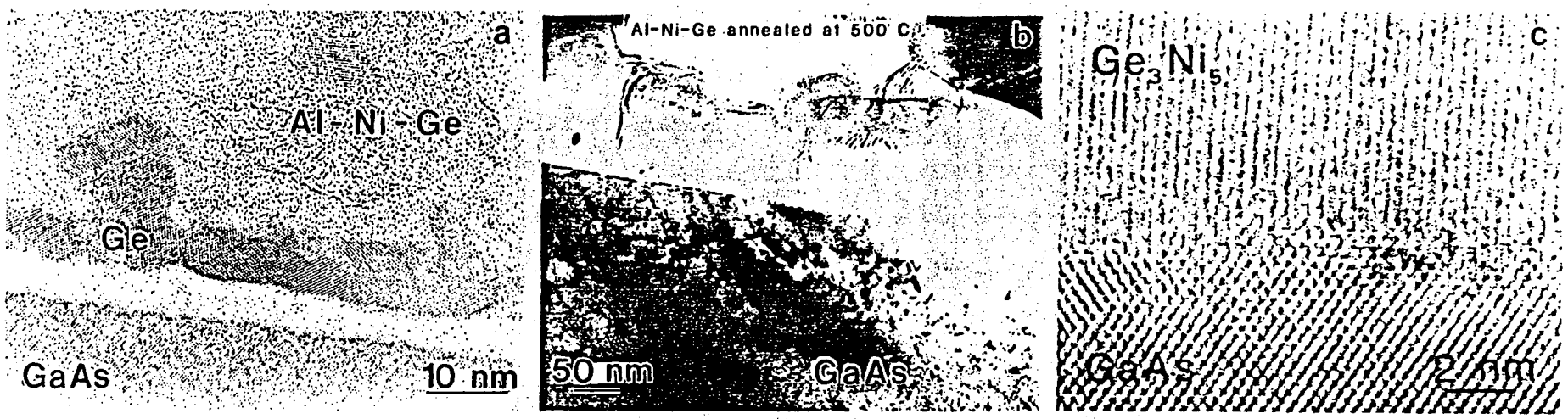
Figure 11. Defects formed after annealing at 450°C at the Au-Ni-Ge/GaAs interface; (*a*) protrusion formation; *(b)* a dislocation at the apex of triangular protrusion; (*c*) microtwins at the intersection of the flat interface and the protrusion.



70%

Fig. 11

Figure 12. TEM micrographs of cross-section of Al-Ni-Ge contacts after annealing at 500°C for 1 min; (*a*) for the contact with Ni layer deposited directly on the GaAs. Note the amorphous oxide layer on the interface with GaAs and the Ge layer formed above it; (*b*) from the contact with Ge layer deposited directly on the GaAs showing flat interface; (*c*) high-resolution micrograph of the same interface, showing formation of Ge_3Ni_5 compound.



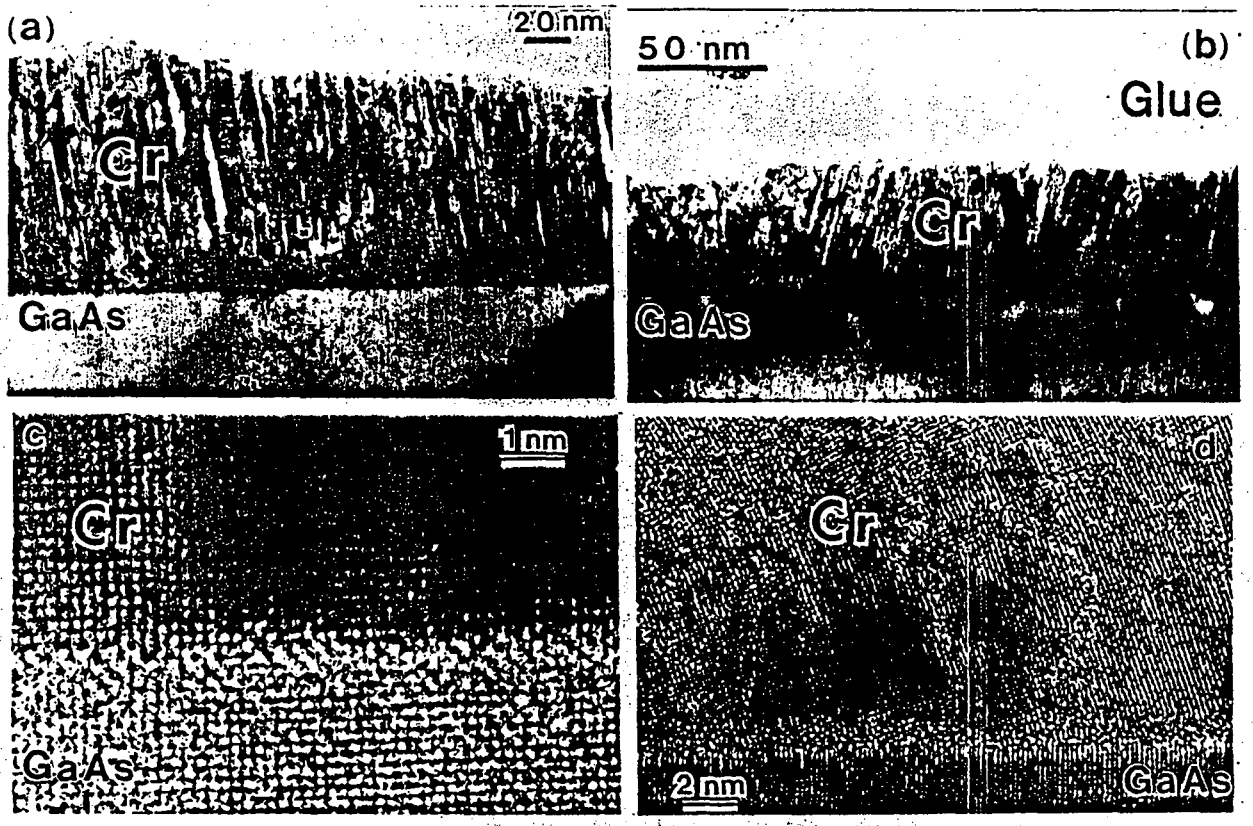
Landscape

Fig. 12

Figure 13. TEM micrographs from Cr/GaAs interface. (*a*) As-deposited UHV sample showing the columnar structure of Cr with voids between columns. Note that columns are almost parallel to each other and inclined ~80° toward the interface with GaAs. (*b*) Air-exposed sample showing a columnar structure of Cr with columns inclined in different directions to the substrate; (*c*) high-resolution micrograph of annealed samples deposited in UHV; (*d*) High-resolution image of annealed air-exposed samples. Note thick layer of oxide at the interface and increased buckling of lattice planes toward the top of the layer.

2.7 Cr/GaAs Morphology and Epitaxial Relationships[34]-[35][52]

Deposition of Cr on either UHV or air-exposed GaAs surfaces leads to the formation of flat interfaces in both cases (Fig. 13 a, b, c, d). Columnar grains of Cr are formed that are separated from each other by voids. However, for air-exposed samples the Cr columns are randomly oriented, and their size was 2 - 4 times smaller than the samples deposited in-situ in UHV. Diffraction patterns show ring patterns typical of polycrystalline Cr material with body-centered cubic (bcc) structure and no texture. The Cr layers deposited in UHV on clean-cleaved surfaces were primarily bcc, however, in some areas face-centered cubic (fcc) Cr with a lattice constant of a = 0.35 nm, was detected. The orientation relationship between the GaAs substrate and the Cr layer was {100}Cr || {100}GaAs with [100]Cr || [022]GaAs. Cr matches almost perfectly to GaAs, because the Cr lattice



70%

Fig. 13

parameter (a = 0.288 nm) is almost exactly half of that of the GaAs lattice parameter (a = 0.565 nm).

Annealing of these samples for 10 min at 370°C in N_2 did not cause the formation of a new phase in the atomically clean and contaminated interfaces. This ~~effect~~ experiment shows that the structure and interface abruptness remained stable after annealing at the described conditions. High-resolution TEM shows a specific contrast, independent of the defocus value, suggesting presence of specific atoms at the interface. Annealing at higher temperatures (630°C for 10 min) leads to the formation of rough interfaces, with grains protruding up to 100 nm into the GaAs (Fig. 14a). Two kinds of grains were found at this interface: $CrAs_2$ and Ga_4Cr_3.[53] Only where the interface is flat, as is found for $CrAs_2$ grains (Fig. 14b), is a consistent epitaxial relationship observed [$(32\bar{2})$ $CrAs_2$ || (200) GaAs and $4\,d_{32\bar{2}} = 2d_{200}$)]. In the areas where the interface is undulated, no specific epitaxial relationship is consistently found.

AQ NOT A SENTENCE.

new paragraph

Figure 14. Cross-section of the UHV deposited Cr/GaAs interface after annealing at 630°C. (*a*) Note formation of protrusions at the interface and unreacted Cr layer at the top of the layer. (*b*) High-resolution image of the $CrAs_2$ lattice matched to the GaAs substrate forming flat interface with the substrate and Ga_4Cr_3 forming protrusion at the interface.

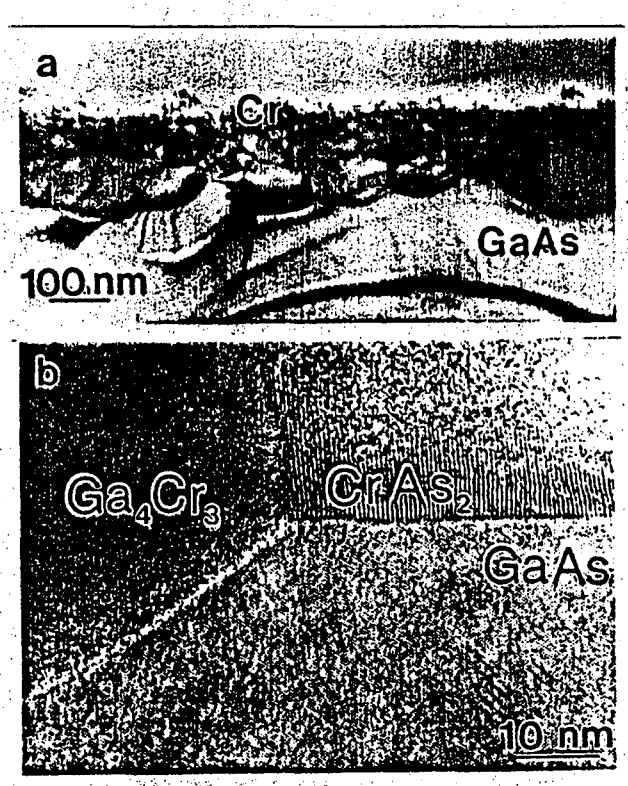


Fig. 14

2.8 Ti/GaAs Morphology and Epitaxial Relationships[38][45]

An example of a metal that reacts with GaAs at room temperature is Ti. Even when GaAs was protected against disruption by solid Xe using cluster deposition on GaAs cleaved in UHV (see Sec. 2.2 for a description of the deposition method), Ti is found to react with GaAs, forming a ~2.5 nm-thick amorphous layer as soon as the Xe layer disperses during warming to room temperature (Fig. 15a).[45] Amorphous layers of approximately the same thickness were also observed when Ti was directly deposited on UHV-cleaved or air-exposed GaAs.[38] The interface with this amorphous layer is atomically flat, indicating that the room-temperature reaction between Ti and GaAs is very uniform. The composition of this layer is not known, since its thickness is not sufficient for EDX studies. XPS studies show the formation of Ti-As bonds,[45] which may be evidence for the initial stages of TiAs phase formation. Unreacted Ti with $(10\bar{1}0)$ planes ($d_{Ti(10\bar{1}0)}$ = 0.255 nm) parallel to the (110) GaAs planes were observed above this amorphous layer. For 100 nm of Ti deposited on UHV-cleaved GaAs and annealed for 20 min at 450°C, the interface is found to be rough. The resulting structure was found to consist of three layers with different compositions (Fig. 15 b, c). The first layer adjacent to the GaAs is the TiAs layer, followed by a Ga_3Ti_2 layer, and then an unreacted Ti layer on the top. The TiAs layer consists of large grains (~ 500 nm) that are twinned to each other with $(\bar{1}012)$ twinning planes (Fig. 15d). Formation of particular twins allows for the best lattice match to the substrate. The main orientation relationship can be described as $[1\bar{2}10]$ TiAs || [110]GaAs with $(\bar{1}010)$ TiAs || $(\bar{1}10)$ GaAs.

$(10\bar{1}0)$

$d_{Ti(10\bar{1}0)}$

$(\bar{1}012)$

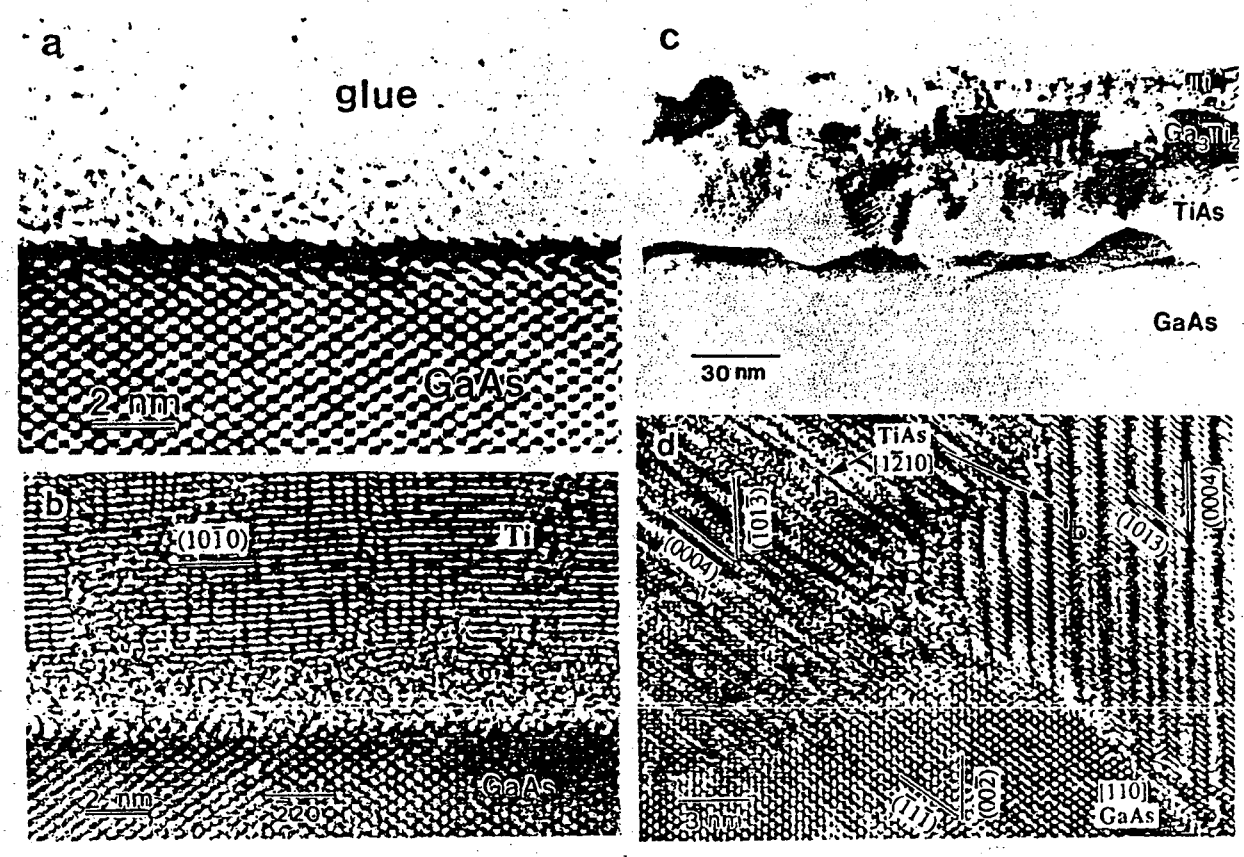
2.9 Pd/GaAs Morphology and Epitaxial Relationships[39]-[41]

Another metal that is highly reactive with GaAs is Pd. Palladium is found to diffuse through the oxide layer, forming a hexagonal ternary phase with the grains connected to each other by low-angle boundaries (Fig. 16). Their major orientation relationship is <0001>||<011>GaAs and $\{\bar{2}110\}$|| {100}GaAs; however, the grains were only parallel to one set of (011) planes. This phase is found to increase in thickness to ~20 nm for samples annealed at 200 - 250°C. Many voids are found in the Pd film since Pd is a diffusing species. When samples are annealed at more than 250°C, another hexagonal ternary PdGaAs phase nucleates at grain boundaries of the first phase. At longer annealing times, this phase penetrates deeply into the substrate, forming many protrusions at the interface. At annealing temperatures higher than 350°C, the first phase disperses, leaving only the

second phase in the layer and possibly some Pd-Ga phases on the top. The first phase, formed at room temperature, is slightly more As-rich than the phase formed at higher annealing temperatures. As described by Sands,[39][40] formation of the second phase and its composition is related to the amount of Pd unconsumed after the first phase is formed. The dependence of the formation of the different ternary phases on annealing temperature and the amount of Pd deposited on the GaAs surface makes this metal/substrate interface highly unstable. However, the fact that Pd can disperse the existing native oxide at the interface is considered a very desirable property of an ohmic contact.[53]

Figure 15. Cross-section of Ti/GaAs interface: (*a*) an amorphous layer formed for cluster Ti deposition on cleaved (110) GaAs buffered by Xe layer; (*b*) formation of the same amorphous layer for Ti deposited directly on the UHV-cleaved (110)GaAs substrate; (*c*) the layers of TiAs, Ga_3Ti_2, and Ti formed after annealing for 20 min at 450°C. Note undulated interface with TiAs; (*d*) high-resolution image of the interface shown in *(c)*. Note twinning of TiAs at the interface with GaAs.

Fig 15

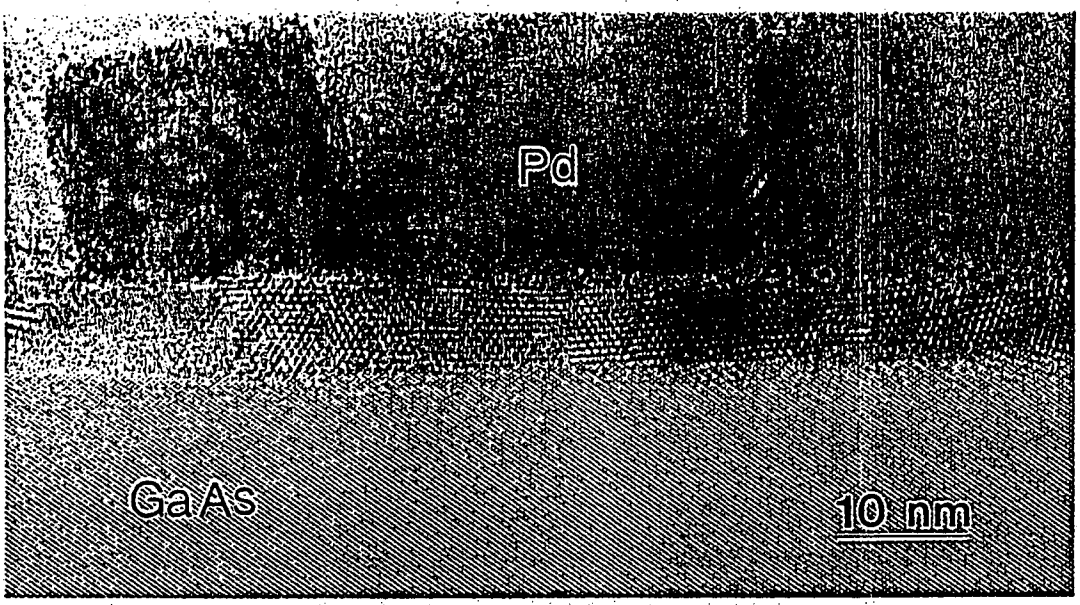

a
glue
GaAs
2 nm
b
(10$\bar{1}$0)
Ti
GaAs
2 nm
220
c
Ti
Ga_3Ti_2
TiAs
GaAs
30 nm
d
TiAs
[1$\bar{2}$10]
(10$\bar{1}$3)
(0004)
(10$\bar{1}$3)
(0004)
(11$\bar{1}$)
(002)
[110]
GaAs
3 nm

70%

Figure 16. Formation of ternary Pd-Ga-As phase after Pd deposition on the UHV-cleaved (110)GaAs substrate.

2.10 TiN/GaAs Morphology[25]

The last type of contact we will discuss is one formed using high-melting metals. Thermally stable Schottky contacts are important in the self-aligned gate MESFET technology because both the gate material and ion-implanted GaAs substrate are subjected to high-temperature annealing (~800°C). Metal-nitrides are considered to be a suitable material for such contacts. The highest barrier height has been measured for ZrN[26] and TiN[25] contacts. For ZrN contacts, the interface remains flat and no degradation in the electrical properties are found up to anneals at 700°C. At higher temperatures amorphous pockets are found at the interface (Fig. 17). For TiN, amorphous pockets have been observed at temperatures as low as 500°C. The average depth of these pockets into the GaAs substrate was about 4 nm. Annealing at higher temperatures increased slightly the depth of penetration of those pockets and decreased the average spacing between pockets. The mechanism of pocket formation is not clear. It is believed that no chemical reaction should occur at the TiN/GaAs interface, but the pocket formation might be related to the coalescence of residual impurities such as oxides at the interface.



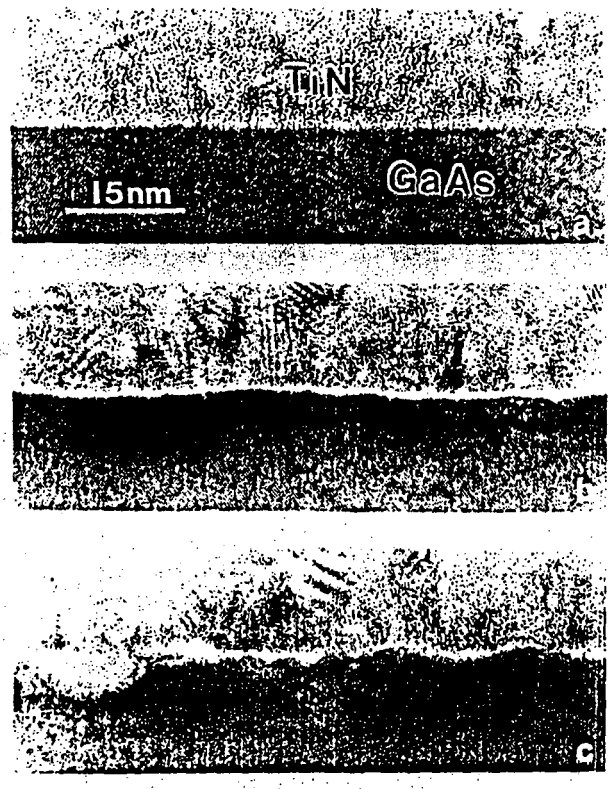
75%

Fig. 16

Figure 17. High-resolution cross-section TEM images of the TiN/GaAs (*a*) as-deposited sample, and (*b*) annealed at 500°C, and (*c*) sample annealed at 800°C. Note the "pocket" formation at the GaAs interface after annealing at the highest temperature.

It can be expected that, even though TiN thin films have been used widely as diffusion barriers in Si technology,[54]-[55] volatile arsenic atoms from the GaAs substrate may be able to escape through weak points and pinholes in the thin intervening layer at the interface. These atoms would then diffuse out through the columnar boundary structure of the thin film and the TiN grain boundaries during anneals at high temperatures. This extensive out-diffusion of arsenic atoms would leave excess gallium atoms at the interface near these weak points, which might form GaN within the pocket. However, this crystalline phase was not detected in our study.[25]

An alternative explanation for this pocket formation is that the fast diffusion paths provided by the columnar boundary structure of the thin film (relative to lattice diffusion) may permit a certain degree of out-diffusion of



100%

Fig. 17

both Ga and As atoms from the substrate, resulting in pocket formation below the interface. These void-like defects would be expected to be detrimental to contact properties. It has recently been found that the number of these pockets at the interface can be related to the substrate preparation before nitride deposition.[56] These findings are consistent with the fact that impurities at the interface can influence interfacial morphology, and the defects present (protrusions, pockets, dislocations and stacking faults) can determine contact properties. Both the defects and the contamination at the interface are expected to greatly influence the kinetics of the resulting interfacial chemical reactions.

3.0 CONTACT STABILITY[3][22]-[24][35]

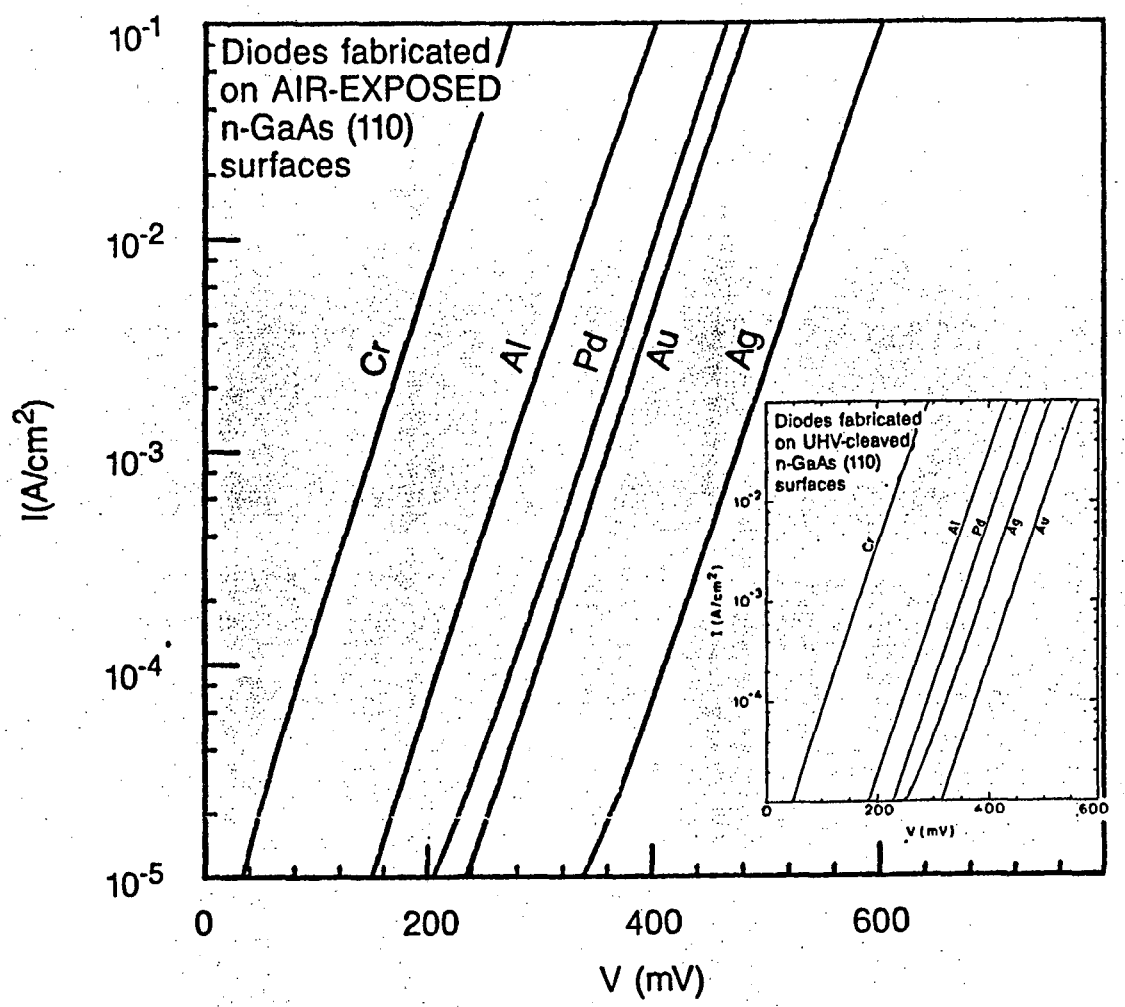
The stability of Schottky contacts deposited on UHV-cleaved and air-exposed GaAs (110) was studied by thermal annealing and electrical aging under reverse bias conditions.[22][23] The results are summarized in Table 1 and Figs.18 and 19.

Table 1. Results of I-V and C-V Electrical Measurements

	Diodes formed on Air-Exposed GaAs(110)			Diodes formed on Clean UHV-cleaved GaAs(110)		
	ϕ_{bo} I-V (eV) ±0.02	n	ϕ_b C-V (eV) ±0.05	ϕ_{bo} I-V (eV) ±0.02	n	ϕ_b C-V (eV) ±0.05
Al						
Unannealed	0.76	1.07	0.84	0.83	1.06	0.87
370°C Anneal	0.83	1.07	0.90	0.90	1.05	0.92
Ag						
Unannealed	0.95	1.07	1.06	0.89	1.06	0.94-0.97
370°C Anneal	0.79	1.06	0.85	0.91	1.07	0.92-0.99
Au						
Unannealed	0.83	1.08	0.94	0.92	1.05	1.00
370°C Anneal	0.65	1.06	0.72	0.80[a]	1.06[a]	0.88[a]
Cr						
Unannealed	0.68	1.06	0.79	0.66	1.06	0.74
370°C Anneal	0.76	1.08	0.88	0.67	1.06	0.74

[a] The data in this table for Au diodes formed on the clean UHV-cleaved GaAs is from a 430°C anneal.

Figure 18. A comparison of typical forward-bias I-V data from a number of metal/n-type GaAs diodes which were fabricated on air-exposed and UHV-cleaved *(insert)* diodes. The exponential dependence with a near unity ideality factor can be seen. For current densities less than 5×10^{-15} A/cm^2, non-linearities due to the effects of leakage currents can be seen in the electrical measurements of the Ag (UHV-cleaved and air-exposed) and Pd (air-exposed) diodes.

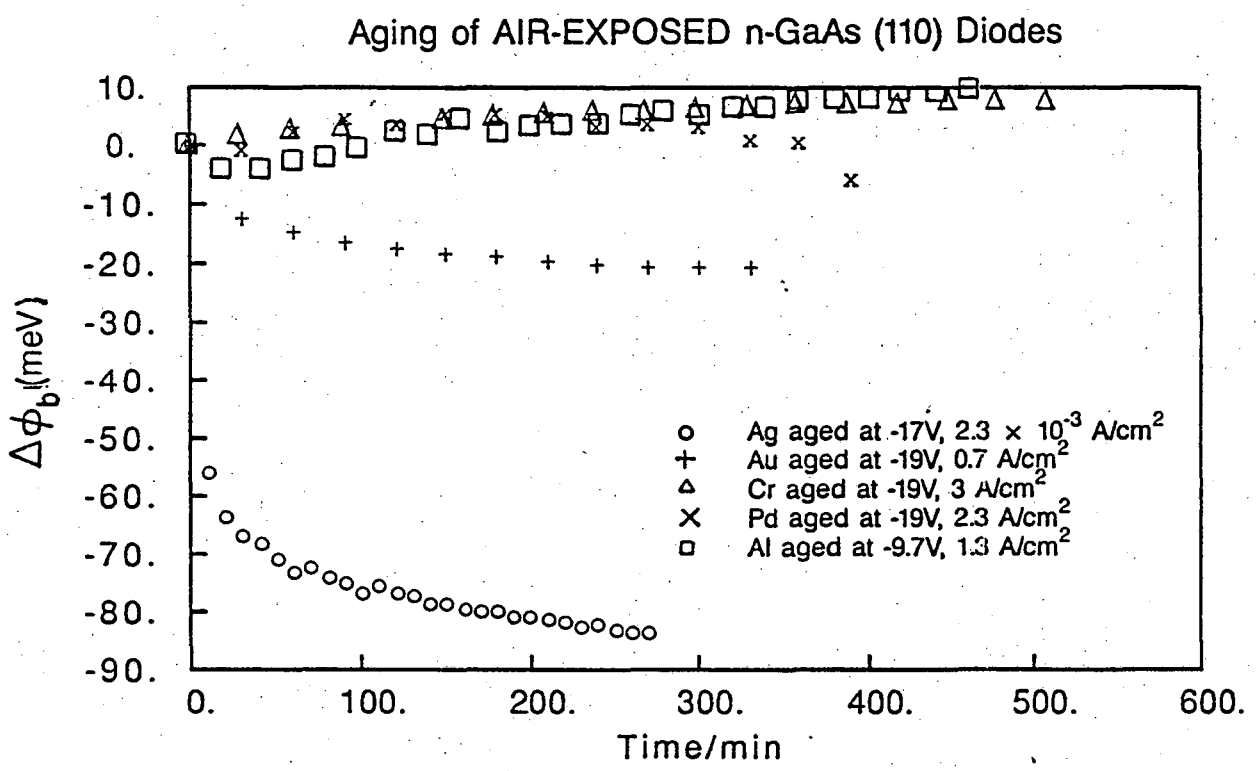

Diodes fabricated on AIR-EXPOSED n-GaAs (110) surfaces
Cr
Al
Pd
Au
Ag
I(A/cm²)
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
0
200
400
600
V (mV)
Diodes fabricated on UHV-cleaved n-GaAs (110) surfaces
Cr
Al
Pd
Ag
Au
I (A/cm²)
V (mV)

75%

18

Figure 19. This figure illustrates typical results of electrical aging for diodes formed on cleaved air-exposed GaAs (110) surfaces. The change in barrier height is plotted as a function of the length of time which the diodes were exposed to electrical aging. The electrical aging conditions for each diode are given in the figure's key.

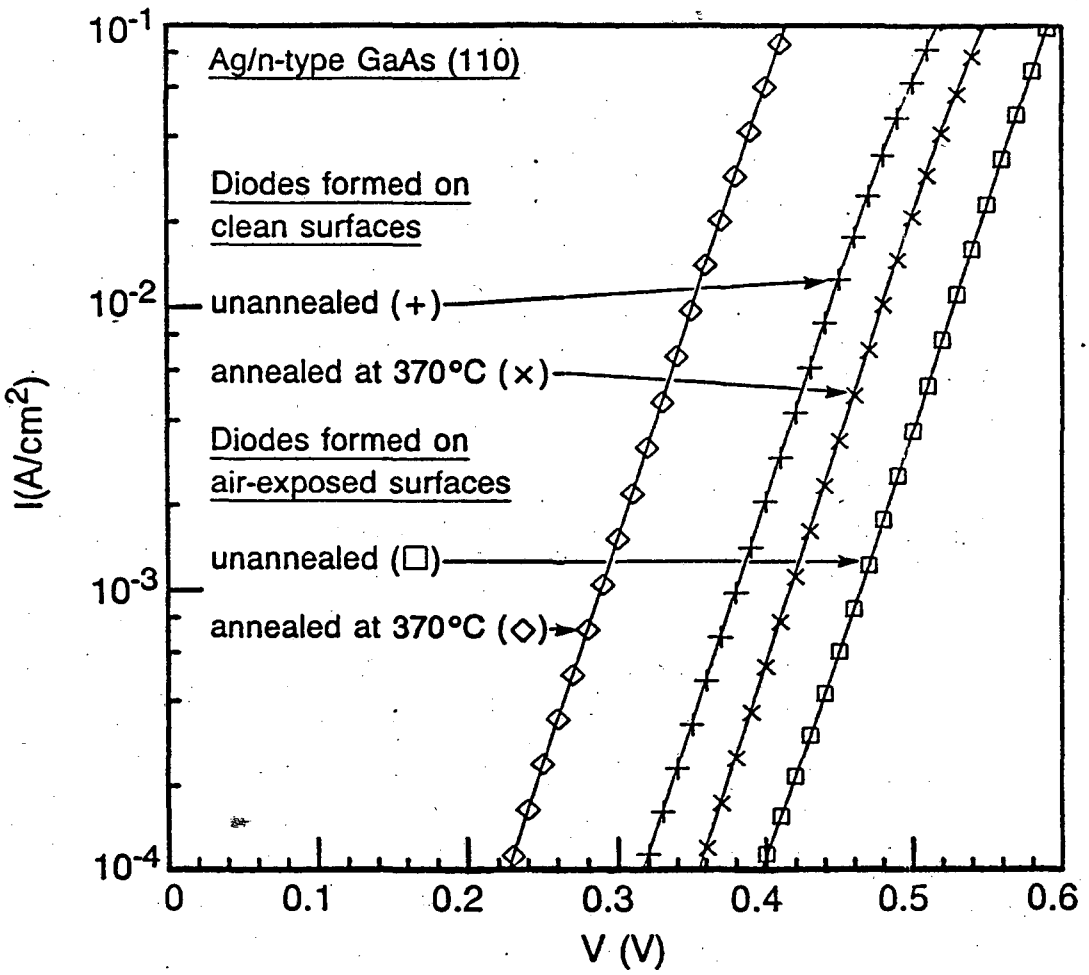
The most important observation is the unexpected stability of contacts deposited in situ on cleaved GaAs (110) under UHV conditions. In contrast, contacts deposited on air-exposed cleaved GaAs (110) show clearly inferior stability upon electrical and thermal stressing. This is especially evident for Ag/GaAs contacts, as shown in Fig. 20 and Fig. 21. The barrier height of these unannealed Ag diodes (obtained from I/V measurements) formed on air-exposed substrates is 0.96 eV. A significant decrease of more than 80 meV was found after 100 min of electrical aging using 2.3×10^{-3} A/cm^2 current density at -17 V reverse bias voltage (Fig. 21). In contrast, the barrier height of Ag diodes formed on UHV-cleaved substrates was 0.89 eV and was stable even upon stressing with 1.4 A/cm^2 for 400 min. Similarly, upon annealing for 10 min at 370°C, the barrier heights of air-exposed diodes decreased by 160 meV, whereas the barrier height of the UHV-deposited Ag diode remained constant to the accuracy of the measurement.


Aging of AIR-EXPOSED n-GaAs (110) Diodes
10.
0.
-10.
-20.
-30.
-40.
-50.
-60.
-70.
-80.
-90.
$\Delta\phi_b$(meV)
0.
100.
200.
300.
400.
500.
600.
Time/min
Ag aged at -17V, 2.3 × 10^{-3} A/cm^2
Au aged at -19V, 0.7 A/cm^2
Cr aged at -19V, 3 A/cm^2
Pd aged at -19V, 2.3 A/cm^2
Al aged at -9.7V, 1.3 A/cm^2

-10%

19

Figure 20. Typical current-voltage (I-V) measurements for diodes formed on clean n-type GaAs (110) surfaces prepared by cleavage in ultra-high vacuum (UHV) and on air-exposed surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours.

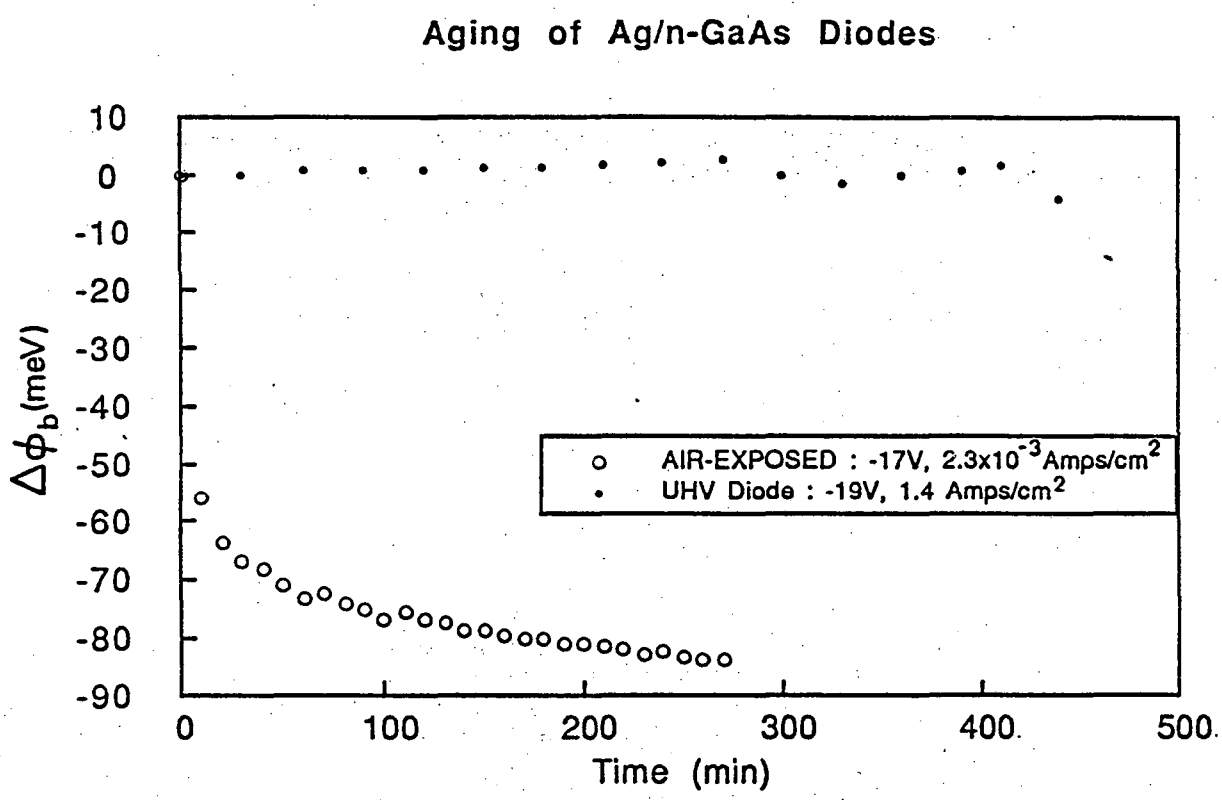

Ag/n-type GaAs (110)
Diodes formed on clean surfaces
unannealed (+)
annealed at 370°C (×)
Diodes formed on air-exposed surfaces
unannealed (□)
annealed at 370°C (◇)
I(A/cm²)
10⁻¹
10⁻²
10⁻³
10⁻⁴
0
0.1
0.2
0.3
0.4
0.5
0.6
V (V)

80%

20

Figure 21. This figure illustrates typical results of electrical aging for Ag/n-type GaAs (110) diodes formed on air-exposed and UHV-cleaved GaAs (110) surfaces. The change in barrier height is plotted as a function of the length of time which the diodes were exposed to electrical aging. The electrical aging conditions for each diode are given in the figure's key.

In Sec. 2.1 significant differences in the structure of the two kinds of Ag contacts were briefly discussed. An oxide layer of 4 nm thickness was present at the interface of as-deposited air-exposed samples, but it was not present in UHV-prepared samples. The air-exposed diodes contained a higher density of twins and much smaller Ag grains compared to samples deposited in situ under UHV conditions. Current stressing did not result in any structural changes of UHV-cleaved diodes (Fig. 22a). However, structural degradation of the air-exposed samples was found with current stressing (Fig. 22b). After current stressing, a significant decrease in Ag grain size, voids separating those grains, and enhanced electromigration of Ag were observed. Thermal annealing of UHV-deposited samples did not degrade the interface flatness; however, annealed air-exposed diodes showed a high density of protrusions similar to that shown in Fig. 3b.

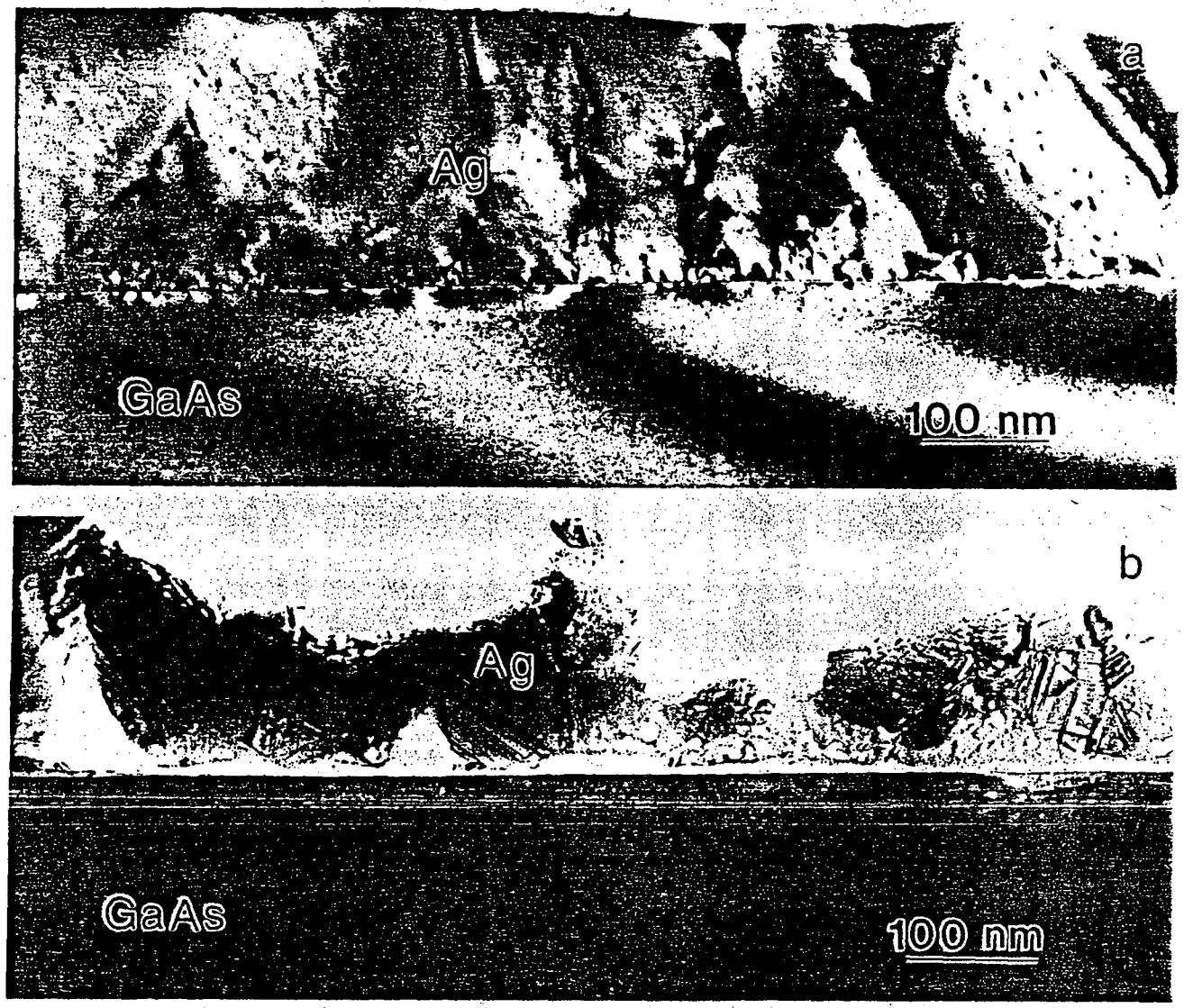

Aging of Ag/n-GaAs Diodes
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
$\Delta\phi_b$(meV)
0
100
200
300
400
500
Time (min)
AIR-EXPOSED : -17V, 2.3x10^{-3}Amps/cm^2
UHV Diode : -19V, 1.4 Amps/cm^2

70%

21

Figure 22. TEM micrographs of Ag/GaAs interfaces after current and voltage aging; (*a*) Ag deposited on UHV-cleaved GaAs aged for 7 hrs, -19 V, 1.4 A/cm2. (*b*) Ag deposited on air-exposed GaAs aged for 50 min, -14 V, 4.3 x 10^{-3} A/cm^2. Note smaller grain size than before aging and void formation.

For Al/GaAs contacts, a very small increase of 9 meV in the barrier height was observed for air-exposed diodes upon electrical stressing for more than 400 min at -9.7 V with a current density of 1.3 A/cm^2. Thermal annealing of UHV-deposited Al contacts resulted in an increase in the Schottky barrier height from 0.83 eV to 0.90 eV. A similar increase of 70 meV was found for the samples deposited on air-exposed substrates, where the barrier height increased from 0.76 to 0.83 eV (Table 1). Although it is tempting to ascribe this increase in barrier height to the formation of near-interfacial AlGaAs with a larger bandgap than GaAs, a careful comparison of the annealing induced changes in the electrical properties of UHV-deposited Al/GaAs and Al/InP revealed that the barrier height of the



65%

contacts on p-type semiconductors had an equal and opposite change to that observed for n-type, i.e., the barrier heights before and after annealing added up to the GaAs bandgap.[3] This indicates that the changes in the barrier height upon annealing of the Al diodes can be attributed to shifts in the interface Fermi-level position within the GaAs bandgap, rather than to the formation of a larger-bandgap semiconductor (i.e., AlGaAs, AlInP).

The influence of interfacial impurities has been observed in admittance measurements of Al contacts deposited by MBE on n-GaAs (100) buffer layers.[57] For Al deposited by molecular beam epitaxy on n+ GaAs wafers, ideal current-voltage characteristics were measured. When Al was deposited using inferior vacuum conditions, nonidealities in the current-voltage characteristics and excess capacitances were seen. The onset of excess capacitances was attributed to the change in surface properties.

The I-V characteristics of Au/n-GaAs (110) diodes showed a considerable difference in barrier height for the Au diodes deposited in situ on UHV-cleaved GaAs (0.92 eV) and deposited on the samples cleaved in air (0.83 eV). After annealing at 370°C for 10 min, the barrier height decreases by 120 meV for the UHV-deposited samples and by 180 meV for air-exposed diodes (Fig. 18). It should be noted that the data for annealed Au/GaAs diodes could only be established after removing the peripheral leakage current.[3] This can be accomplished by the use of a chemical "mesa" etch.[3] The excess current is due to thin Au "fingers" formed at the thin boundary region of the Au contact. Surface recombination at these peripheral structures was shown to cause the Au/GaAs diode degradation upon annealing in the 400°C range.[58]

On air-exposed Au/GaAs (110) samples, which were air-exposed Au deposition, electrical aging was performed using -19 V reverse bias at a current density of 0.7 A/cm^2 for 200 min. A decrease in the barrier height of over 20 meV was found (Fig. 23). With atomically clean Au interfaces, similar instabilities were observed upon electrical aging at -19 V reverse bias at a current density of 4.2 A/cm^2 for 200 min. A decrease in the barrier height of over 15 meV was found.

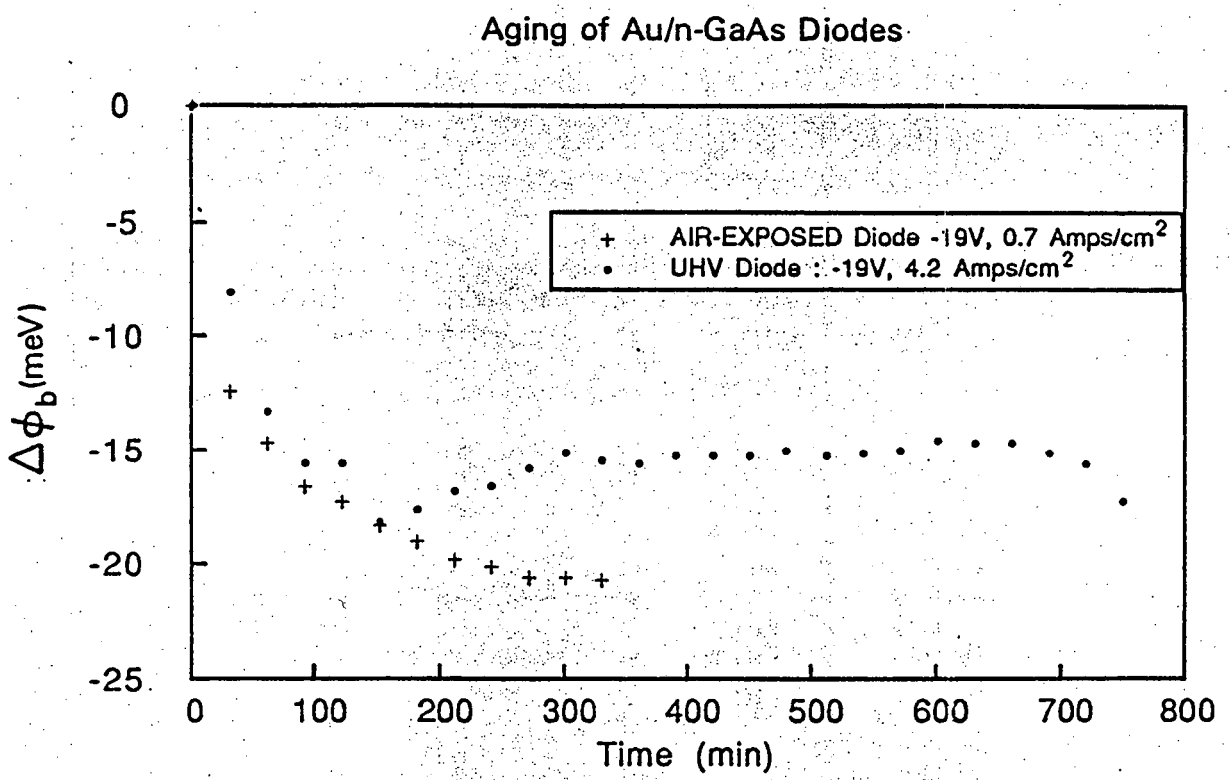
The microstructure of the Au/GaAs (110) diodes is described in detail in Sec. 2.2. It showed similarities to Ag/GaAs: Annealing of UHV-deposited samples revealed preservation of a flat interface accompanied by an increase in grain size, whereas for air-exposed diodes, the formation of faceted protrusions at the interface was observed upon annealing. No significant change of the microstructure was found after electrical stressing.[59]

Figure 23. This figure illustrates typical results of electrical aging for Au/n-type GaAs (110) diodes formed on air-exposed and UHV-cleaved GaAs (110) surfaces. The change in barrier height is plotted as a function of the length of time which the diodes were exposed to electrical aging.

Electrical aging of Cr/GaAs (110) diodes at -19 V for more than 6 hr with a reverse current flow of 3 A/cm2 did not change the barrier height by more than 6 meV (within experimental error) for contaminated interfaces. However, annealing of contaminated Cr interfaces up to 370°C induced an 80 meV increase in barrier height (from 0.68 to 0.76eV), while the same thermal treatment did not lead to any significant changes in the barrier height of atomically clean interfaces (Fig. 24). The change in the barrier height for the contaminated interfaces is correlated with the smaller Cr column size found in these samples, as compared with atomically clean interfaces (Fig. 13). The high number of voids between small, randomly oriented columns may allow As to escape during annealing. Because the column size in the annealed UHV samples is larger, the number of voids is fewer, and the out-diffusion of As might be suppressed in these samples.

3 A/cm^2

These observations show that surface preparation of a semiconductor before metal deposition, and impurities present during deposition, can be detrimental to metal contact performance in that they can influence the stability of the electrical properties. Moreover, the observed differences in changes of barrier height upon annealing revealed some interesting correlations with the near-interfacial stoichiometry. This topic is discussed in the next section.

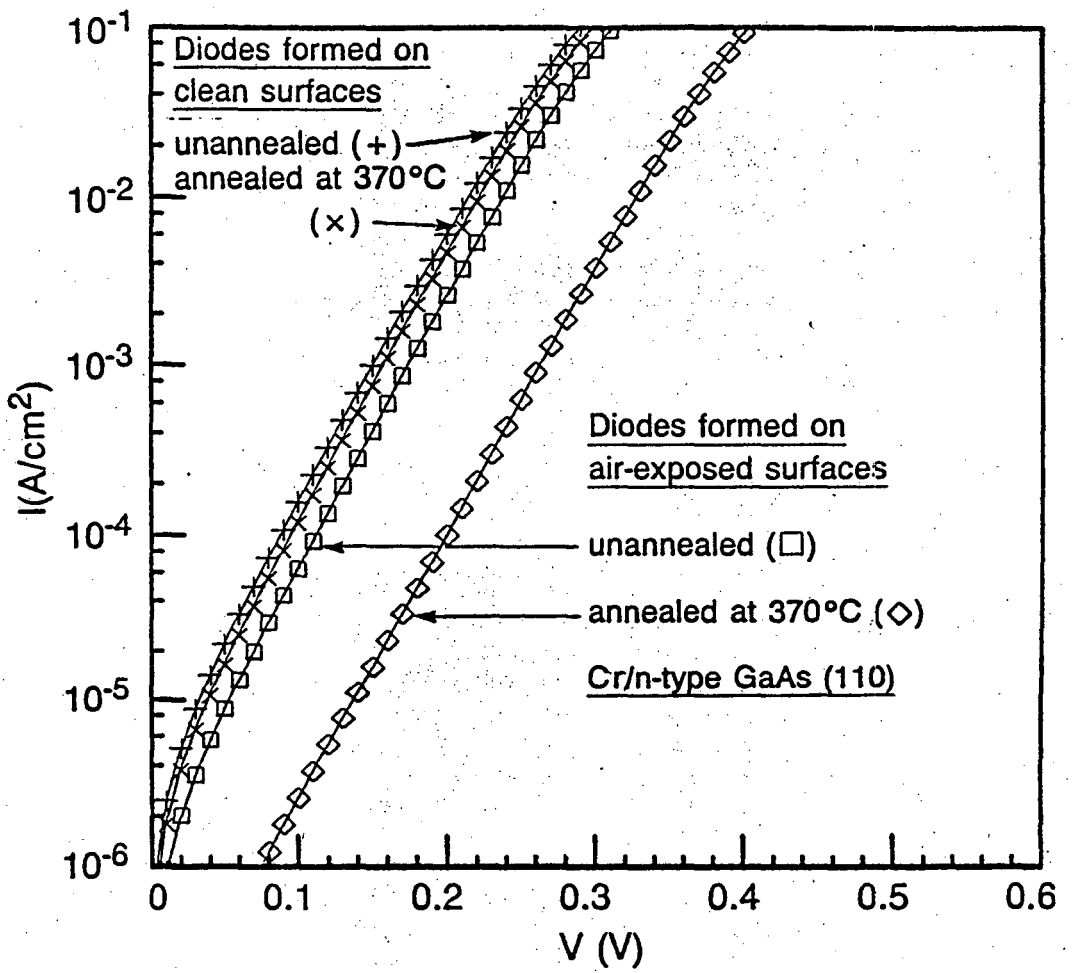

Aging of Au/n-GaAs Diodes
AIR-EXPOSED Diode -19V, 0.7 Amps/cm2
UHV Diode : -19V, 4.2 Amps/cm2
Δφb(meV)
0
-5
-10
-15
-20
-25
0
100
200
300
400
500
600
700
800
Time (min)

55%

Figure 24. Typical current-voltage (I-V) measurements for Cr diodes formed on clean n-type (110)GaAs surfaces prepared by cleavage in UHV and on air-exposed surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours. Note a change in the barrier height after annealing for the contaminated interfaces.

4.0 NEAR-INTERFACIAL STOICHIOMETRY

The metal/n-GaAs (110) Schottky barrier of in situ UHV-prepared samples was found to exhibit near-ideal electrical characteristics. The lowest barrier height was found for Cr (Φ_b = 0.67 eV) and the highest for Au (Φ_b = 0.92 eV).[2] Cross-sectional samples of these contacts were studied by conventional and analytical transmission electron microscopy. The characteristic x-ray emission (EDX) spectra consistently show a deviation in stoichiometry for the region within ~10 nm of the GaAs beneath the metal contact, as compared with the GaAs far from the interface (Fig. 25). The

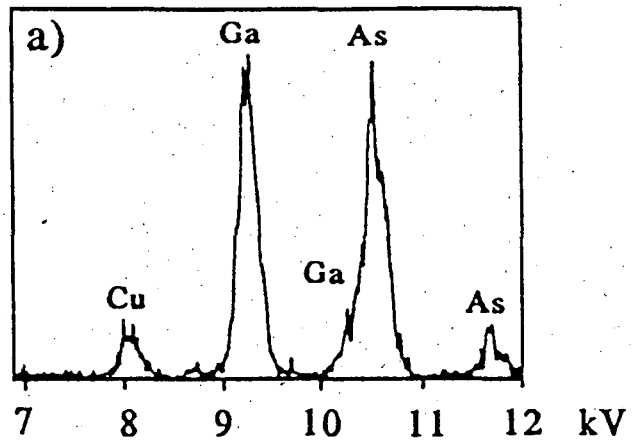

Diodes formed on
clean surfaces
unannealed (+)
annealed at 370°C
(×)
Diodes formed on
air-exposed surfaces
unannealed (□)
annealed at 370°C (◇)
Cr/n-type GaAs (110)
I(A/cm²)
V (V)
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
0
0.1
0.2
0.3
0.4
0.5
0.6

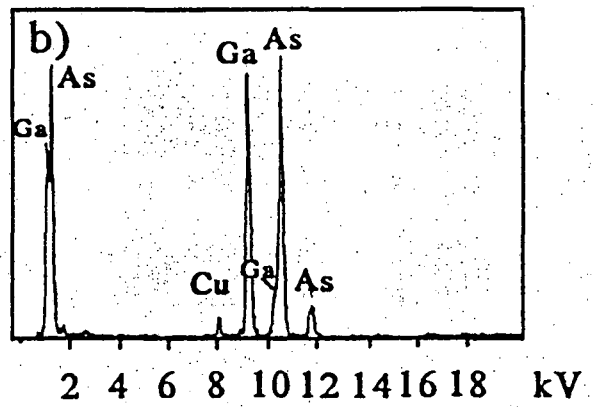
80%

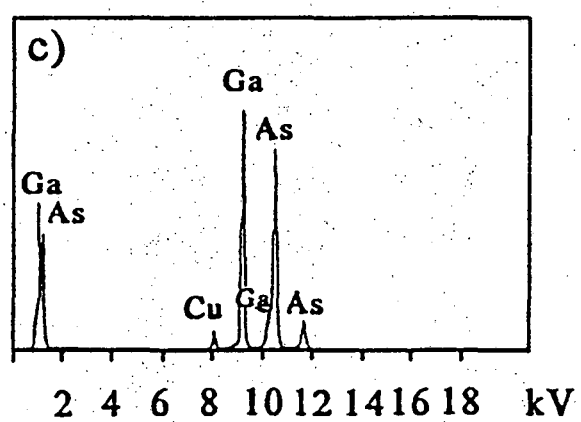
24

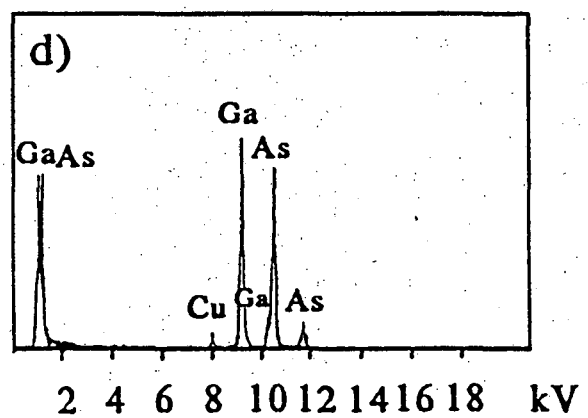
deviation is always As-rich when compared quantitatively to bulk GaAs. These measurements of the crystal stoichiometry are very difficult, as the excess As is volatile under the electron beam. Even when an electron beam is directed onto an As precipitate, the stronger As-K_α peak relative to the Ga-K_α peak can be observed only for a short time. Therefore, to obtain statistically reliable results at a given distance from the interface, the electron beam was scanned to several equivalent positions along the interface so that reliable data could be obtained.

Figure 25. EDX spectra taken in the GaAs substrate; (*a*) below the annealed Au layer deposited on the UHV-cleaved (110)GaAs surface; (*b*) below the Cr layer deposited in the same way; (*c*) below Au cluster deposited on the UHV-cleaved (110)GaAs surface buffered by Xe; *(d)* far from the interface. The As/Ga ratio in *(c)* and *(d)* is typical for bulk GaAs.In *(a)* and *(b)* case As/Ga ratio is much higher indicating As rich interfaces.


a)
Ga
As
Cu
Ga
As
7 8 9 10 11 12 kV


b)
As
Ga
Ga
As
Cu
Ga
As
2 4 6 8 10 12 14 16 18 kV


c)
Ga
As
Ga
As
Cu
Ga
As
2 4 6 8 10 12 14 16 18 kV

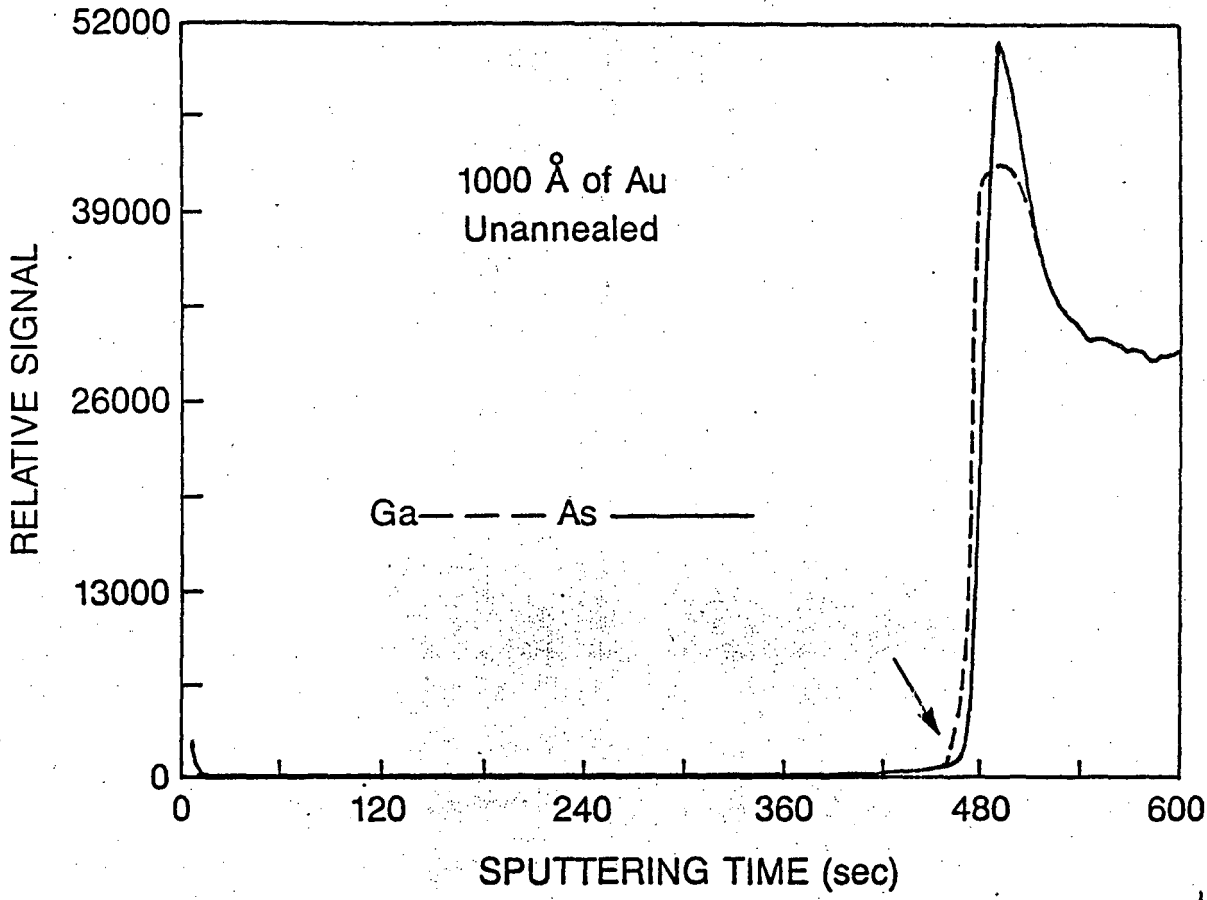

d)
Ga
As
GaAs
Cu
Ga
As
2 4 6 8 10 12 14 16 18 kV

50%

Fig. 25

This As instability under the electron beam was further confirmed by studying As-rich GaAs grown by MBE at low temperature (~200°C). These layers are known from conventional x-ray and PIXE analysis to contain up to 1.5% of excess As.[60]-[61] Studying cross sectional samples of low-temperature (LT)-GaAs by EDX showed a very similar time dependence: the x-ray signal from excess As can be seen only for a certain time. Comparison of the near-interfacial regions of metal/GaAs contacts for interfaces that are known to be As-rich (such as Cr/GaAs) to that of As-rich LT GaAs leads to the conclusion that the (average) deviation from stoichiometry in a 10 nm-deep region from the metal/GaAs interface must be on the order of 1%. The increase in As concentration (Fig. 26) near the metal interface was confirmed independently by SALI.[30]-[31]

Figure 26. SALI depth profiles of UHV prepared Au (100 nm thick) on GaAs. A 5 keV Ar^+ beam was used with ~ 30 mm diameter and a DC current of ~ 100 mm.


52000
39000
26000
13000
0
RELATIVE SIGNAL
1000 Å of Au
Unannealed
Ga— — — As ———
0
120
240
360
480
600
SPUTTERING TIME (sec)

45%

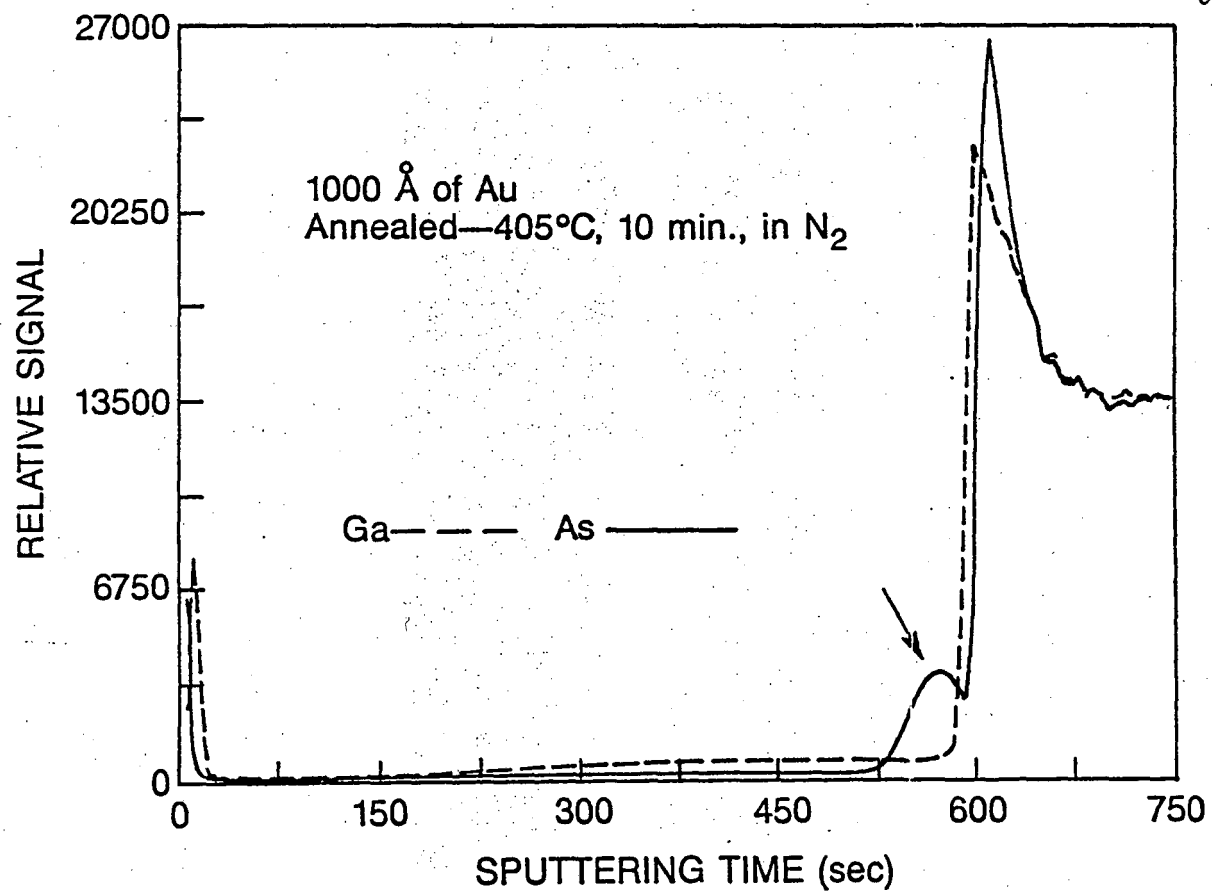

27000
20250
13500
6750
0
RELATIVE SIGNAL
1000 Å of Au
Annealed—405°C, 10 min., in N_2
Ga— — — As ———
0
150
300
450
600
750
SPUTTERING TIME (sec)

Fig. 2b

Comparison of the EDX spectra of different metal/GaAs contacts gives evidence that the amount of additional As found in this near-interfacial region depends on the metal used and the thermal history of the sample. For as-deposited metals, the largest deviation from stoichiometry was found for Cr, and the smallest was found for Au. After annealing above 370°C, the Au barrier height *decreased* by 120 and 180 meV for UHV-deposited and air-exposed samples, respectively.[3][22] In contrast, the Cr barrier height was stable upon thermal annealing for UHV-deposited samples but *increased* by 80 meV to 0.76 eV for air-exposed samples.[22] Air-exposed annealed Cr/GaAs samples showed less excess As than the as-deposited structures; the excess concentration was comparable to Au/GaAs in magnitude. Indeed, the barrier height of annealed Au/GaAs samples (0.80 eV) is also comparable to annealed air-exposed Cr/GaAs samples (0.78 eV).[3][22] The excess As found near the Al/GaAs interfaces was less than that found for Cr/GaAs, and showed a similar decrease upon annealing.

Nevertheless, all the Schottky barrier heights found in the course of this work[2][3][22][36] correspond to Fermi-level pinning positions between 0.75 eV and 0.5 eV above the valence band maximum. In addition, changes in barrier height upon annealing were found to correlate~~d~~ with changes in the near-interfacial stoichiometry. An increase in the barrier height of n-GaAs such as the one found for Cr on air-exposed GaAs (110) and for Au on UHV and air-exposed GaAs (110), is correlated with As-rich interfaces in both cases. However, the amount of excess As near the interface in the first case is much larger than in the second case. The changes in As concentration at the interface after annealing for Al, Ag, Au, and Cr contacts are generally found to follow this relationship: an increase (decrease) in As concentration results in a decrease (increase) in barrier height. This relation and the change in As concentration is especially noticeably for Au and Al. In the first case, higher As concentration is observed after annealing compared to as-deposited samples. In contrast, for Al, the As concentration is lower in annealed samples compared to as-deposited samples.

The observed changes in stoichiometry and near-interfacial reconstruction are typical for atom-by-atom deposition methods such as evaporation or sputtering in vacuum onto substrates kept near room temperature. During such a deposition, the metal atoms condense from the gas phase to the solid phase, which releases the heat of sublimation and may result in disruption of the semiconductor surface. In addition, a significant amount of energy can also be released when metal atoms combine on the surface to form clusters. This is particularly important for the less-reactive metals such as Ag. This surface disruption might be avoided by cluster deposition,

described in Sec. 2.2. The energetics of such a deposition are dramatically different from atom-by-atom deposition, making it possible to minimize surface disruption. Analytical electron microscopy performed in the semiconductor below the clusters (Fig. 25) did not show any deviation from stoichiometry of the sort observed for cases such as the Au atom-by-atom deposition onto the GaAs surface.[45] This shows that metal/semiconductor interfaces free of bulk defects can be formed. Photoemission measurements gave evidence for Fermi-level pinning of cluster-deposited Schottky contacts outside the usually observed range of energies.[44]-[45]

5.0 NEAR-INTERFACIAL ELECTRICALLY ACTIVE DEFECTS

In Sec. 2 - 4 of this chapter, a detailed structural analysis of metal/GaAs contacts is summarized. In all cases investigated, the interfaces were far from ideal: for in-situ UHV deposition, a distinct deviation from perfect stoichiometry was found; for diodes deposited onto air-exposed GaAs (110) surfaces, an interfacial oxide layer can also be detected that influences both the chemistry and orientation relationship of the metal grains to the substrate. Moreover, evidence for distinct changes of the near-interfacial stoichiometry upon annealing of the diodes was found.

It is difficult to reconcile these experimental results with models that ascribe the narrow range of Fermi-level pinning positions to the extra states in the semiconductor band gap induced by the metal contact.[8] The dependence of the pinning position on the near-interfacial stoichiometry strongly suggests the influence of near-interfacial electrically active defects.

Two defect-related models currently receive the greatest level of acceptance: (*i*) the effective work-function model that ascribes the Fermi level pinning to the work function of As-rich metal compounds that are hypothesized to be formed at the metal/semiconductor interface,[9]-[10] and (*ii*) the antisite defect model,[14][17][63] which was based originally only on the experimental determination of the energy levels of As_{Ga} antisite defects at E_c -0.75 eV and E_v +0.52 eV.

The structural studies summarized in this chapter do not support the effective workfunction model.[9]-[10] For the model to be applicable, the presence of anion-rich clusters or anion-rich near-interfacial phases is required for all the Schottky contacts studied here. The limit of detection is the resolution limit of high-resolution electron microscopy, which can easily detect clusters above 2 nm diameter or thin-film phases above one

monolayer in thickness. It is worth noting that the situation is completely different for low-temperature grown GaAs, in which *after annealing above 500°C*, a high density of As precipitates is found.[64]-[65] It has been suggested that these As precipitates are responsible for the Fermi-level pinning in these semi-insulating layers.[66]

It is worth considering in detail whether the antisite defect model finds support in this and other recent studies. This model assumes that the surface disruption upon metal sublimation from the gas phase onto the GaAs surface releases enough energy to displace atoms in the first few monolayers of the crystal, so that a certain fraction of these distorted atoms comes to rest in the wrong sites, effectively forming a high concentration of antisite defects of both kinds, As_{Ga} and Ga_{As}. If the near-interfacial region is anion-rich, as experimentally observed, it is expected that As_{Ga} will dominate, partly compensated by Ga_{As}. This situation of a high As_{Ga} concentration partly compensated by other native defects is found as well after heavy n-irradiation of bulk GaAs[17] or in as-grown MBE layers of GaAs grown at low temperatures (LT-GaAs).[59]-[60]

The range of Fermi-level pinning positions determined electrically with well-defined contacts on GaAs correspond very well to the two donor levels of the anion antisite defect at $E_v + 0.52$eV and $E_c - 0.75$eV.[17]

Changes of near-interfacial stoichiometry are predicted in this model to result in characteristic changes in the Fermi level pinning position. More As-rich interfaces with little compensation should be dominated more by the upper, near midgap donor level of As_{Ga}, corresponding to lower barrier heights for n-GaAs; while less excess of As at the interface should result in stronger compensation and thus stronger domination of the second donor level at $E_v + 0.5$ eV, i.e., in larger barrier heights on n-GaAs. This prediction of the antisite defect model is without exception supported by the experimental observations of correlated changes of barrier height and near-interfacial stoichiometry described in the previous section. Additional examples of correlations between interfacial stoichiometries and barrier heights are discussed in detail by Spicer.[63]

Direct evidence for the creation of deep-level defects upon metal deposition on GaAs was found by cathodoluminescence experiments of Chang et al.[67]-[68] These authors detected the evolution of an emission peaking near 0.85 eV upon Au, Cu, and Al deposition on (100)GaAs grown by MBE, together with other emissions that were more typical of the respective metals. It is worth noting that this 0.85 eV emission corresponds quite well to near-midgap electronic energies, although a direct correlation with an emission known from bulk GaAs defects is not yet possible.

If the Fermi level pinning position were indeed dominated by deep-level defects, then application of hydrostatic pressure should result in similar changes in the barrier height and the defect ionization energy. Shan et al.,[69] studied the pressure dependence of the Pt/n-GaAs(100) Schottky barrier height and found a parabolic behavior according to:

$$e\Phi_b(P) = 0.703\,[\mathrm{eV}] + 11\,[\mathrm{meV/GPa}]\,P - 2.6\,[\mathrm{meV/GPa^2}]\,P^2$$

For the midgap level of EL2 (which is generally accepted to be essentially an As_{Ga} antisite defect) a distinctly different pressure dependence was found by DLTS:[70]

$$(EL2)^{0/+} = 0.703\,[\mathrm{eV}] + 44\,[\mathrm{meV/GPa}]\,P - 1.1\,[\mathrm{meV/GPa^2}]\,P^2$$

However, DLTS measures the electron emission barrier, which is the sum of the true thermal ionization energy (E) plus the barrier against free carrier capture E^{cap}.[71] Therefore, the capture barrier has to be taken into account for a correct evaluation of the EL2 pressure dependence. Baj and Dreszer[72] recently measured the pressure dependence of the capture barrier as:

$$\partial E^{cap}/\partial P = (-49 \pm 5)\ \mathrm{meV/GPa}$$

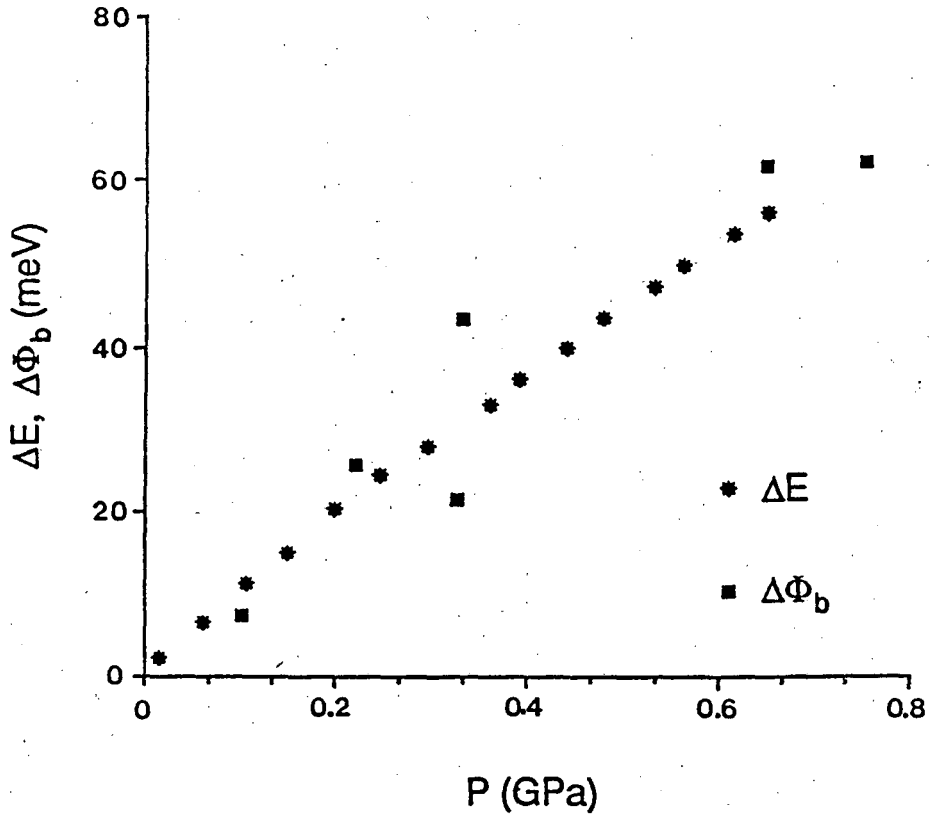
Therefore, the pressure dependence of the EL2 ionization energy is:

$$E = 0.703\,[\mathrm{eV}] + 93\,[\mathrm{meV/GPa}]\,P - 1.1\,[\mathrm{meV/GPa^2}]\,P^2$$

Figure 27 presents experimentally determined values of the pressure dependence of the Schottky barrier height[69] and pressure-induced energy level changes of the $EL2^{0/+}$, ΔE,[70] corrected by the pressure dependence of the capture barrier.[72] It is clear that *the pressure dependence of* $\Delta E(P)$ *cannot be distinguished within the accuracy of the experimental data from the pressure dependence of the Schottky barrier* $\Delta\Phi_b(P)$ *of Pt/n-GaAs*. This conclusion is in direct contradiction to the original conclusion of Ref. 69, whose analysis neglected the pressure dependence of the capture barrier. Although this extraordinary agreement is not unique, as some other deep-level defects have similar pressure coefficients, it can be regarded as a very strong argument in favor of the antisite defect model.

Figure 27. Pressure-induced change of the Schottky barrier height $\Delta\Phi_b(P)$ according to Shan et al[69] and experimental data of thermal ionization energy of the $EL2^{0/+}$ level, $\Delta E(P)$ obtained as a sum of an activation energy of the emission rate after Dobaczewski and Sienkiewicz[70] and the pressure derivative of capture barrier energy.[68] Note the excellent agreement between these two sets of data.

Moreover, the dominance of antisite defects in the Fermi level pinning process could be avoided if defect formation could be suppressed altogether, or influenced by modification of the interfacial stoichiometry. For MBE-grown metal/GaAs (100) interfaces, conflicting results were published: Viturro et al.[73] report photoemission results indicating a very strong dependence of the barrier heights on work function for low-temperature deposited contacts of Ag, Al, Au, Cu, In, and Yb, whereas Wilks et al.[74] reported I/V measurements of similar diodes (In, Al, and Au) that revealed only the well-known "canonical" pinning positions near and slightly below midgap. This difference, e.g., in the case of Al between a barrier height near 0.2 eV[73] and 0.79 eV[74] might be due to either the methods used (photoemission vs. electrical measurements) or to the different approach: whereas Wilks et al.[74] deposited the metallization in situ on UHV-clean, freshly grown GaAs (100) surfaces, Vitturo et al.[73] utilized GaAs wafers grown ex situ that were capped with As that had to be thermally desorbed before the metal deposition. As it is unlikely that this large a discrepancy can be due to artifacts such as surface photovoltaic effects,[75] the different surface stoichiometry due to the As-capping might play a decisive role.



55%

Fig. 27

Similarly, distinct changes in the barrier height (determined by photoemission) were found for off-axis substrates with a high step density,[67] which might again be related to different interfacial stoichiometry. However, a detailed study of the effective stoichiometry present at the MBE-grown interfaces has not yet been performed.

A different approach which avoid the formation of interfacial defects, has been described in Sec. 2.3. Photoemission measurements of diodes prepared by cluster deposition rather than by the disruptive atom-by-atom deposition indicate Fermi level pinning positions outside the commonly observed range.[43] In this case, analytical electron microscopy of cross-sectional samples did not find evidence for the As-rich near interfacial layer typical of contacts prepared by the more disruptive atom-by-atom deposition.

Finally, recent self-consistent local density calculations of several metal/GaAs structures have revealed that the Fermi-level pinning positions for "ideal" unreconstructed interfaces in the absence of defects should range throughout the band gap, depending on the metal and the interfacial geometry, effectively refuting the notion that metal-induced gap states should result in a universal pinning position near the experimentally observed values.[76] Moreover, it was directly demonstrated that defects present near the interface can indeed result in pinning at the bulk-like levels of the defects.[77] This study thus provides a "missing link" between the extensive experimental evidence for the role of deep-level defects in Fermi-level pinning and state-of-the-art theory of the electronic properties of heterostructures.

6.0 CONCLUSIONS

This study allows us to conclude that interface morphology, grain size and orientation of metal layers on GaAs depend strongly on the surface preparation of the substrate before metal deposition. The metals investigated (Au and Ag, with similar lattice parameters), deposited in situ on a UHV-cleaved GaAs surface, show very similar orientation relationships with GaAs upon annealing. This relationship changes when GaAs is exposed to air before metal deposition. All metals investigated, when deposited on UHV-cleaved GaAs, are stable upon annealing. For Cr, an almost perfect lattice match to GaAs was observed for UHV-deposited samples, but random orientations were observed for air-exposed samples. A pronounced correlation between changes in barrier height and near-

interfacial stoichiometry was found. This correlation has important implications for the fundamental understanding of the mechanism of Fermi-level pinning. High-resolution electron microscopy showed evidence of lattice reconstruction and defect formation in the interfacial area, supporting defect models of Schottky barrier formation.

Among the defect models for Fermi-level pinning, the antisite defect model seems to be especially attractive, as it directly relates to the experimentally determined barrier heights and the observed deviation from stoichiometry. Besides the agreement with a large number of well-known experimental results,[62] this model received additional support through the new observation that the pressure dependence of a typical Schottky barrier (Pt with Φ_b = 0.70 eV) corresponds within the measurement error to the pressure dependence of EL2, which is composed of an As antisite defect. On the other hand, a defect model requires the possiblity of avoiding or modifying the defect formation, and this is indeed the case, as the examples of MBE-deposition and cluster-deposited contacts seem to indicate.

Therefore, a realistic model of the metal/semiconductor interface has to take into account intrinsic and extrinsic interfacial processes: intrinsic effects such as metal-induced gap states and interfacial dipoles can be dominating if defect formation is effectively suppressed, but we conclude that extrinsic effects take over in most metal/GaAs rectifying contacts of practical relevance that show the well-known small range of Fermi-level pinning positions.

Despite the large body of circumstantial evidence in favor of the defect model that was discussed in detail in Sec. 5, further experiments are required to finally directly *identify* the defects that are involved in the Fermi-level pinning process. As we are reaching the limits even of high-resolution electron microscopy, this final clarification might come from scanning tunneling microscopy, a technique that should allow us to directly image individual point defects.

ACKNOWLEDGMENT

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